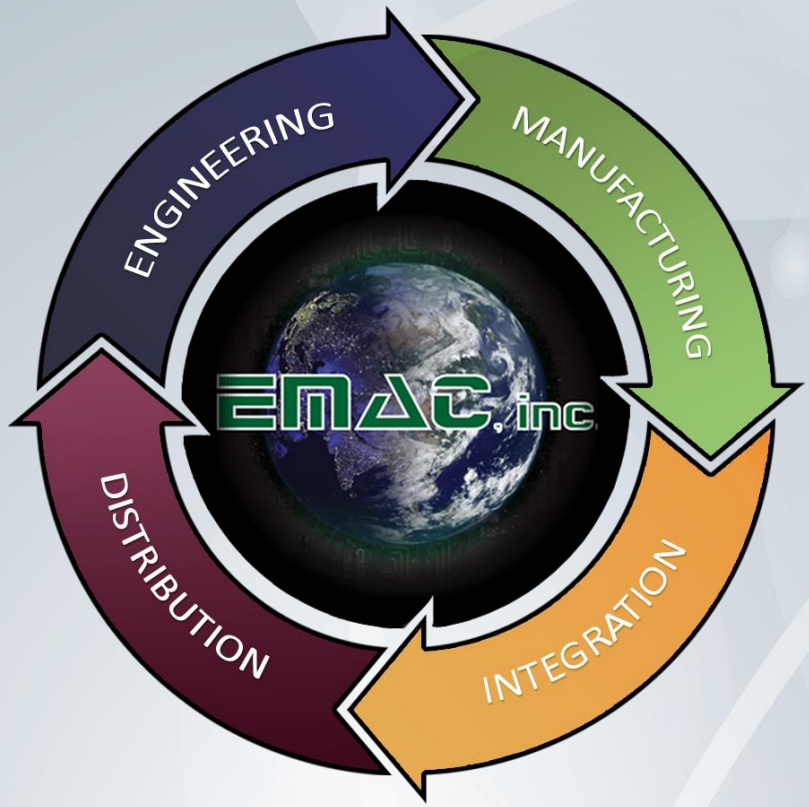
Equipment Monitor And Control



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Design for Accuracy, Manufacturability & Test

Presented by Eric Rossi Engineering Manager
& Members of the EMAC Engineering Team

EMAC, Inc.

Seminar Overview

This seminar will cover the best practices to producing a Printed Circuit Board Assembly (PCBA) that can be efficiently manufactured and tested, as well as a discussion of Test-Sets for testing of PCBAs. The seminar will explore best practices in achieving an error free design (addressing most common mistakes), Design for Manufacturing (DFM) and Design For Test (DFT). Further discussion will briefly cover the various ways an Assembled Board can be tested (AOI, ICT & FCT), constructing Test-Sets, Test Software and Test Data Logging & Reporting. Time will be set aside for Q&A after the presentation.

EMAC, inc.
EQUIPMENT MONITOR AND CONTROL

EMAC, Inc Overview

- **Sale of Off-The Shelf SBCs, SOMs, PPCs, Servers**
- **Engineering Services both Software & Hardware, including Design of Test-Sets**
- **Integration Services (Box Builds, Wiring Panels, etc.)**
- **Manufacturer of Electronic Assemblies**

- **EMAC Contract Manufacturing (CM)**
  - **What makes us different**
    - **We are an Engineering company that does Manufacturing**
    - **Closed Loop Process**
    - **We feed design issues back to the Client for them to fix or EMAC can perform the changes**
    - **As an Engineering Company we can make Smart recommendations on Part & Design for Manufacturing Issues**
    - **We are very good with Complex boards**
    - **We have designed a number of Custom Tools to assure High Quality & Customer Satisfaction**

Design For Accuracy (DFA)

DFA consists of the Best Practices for Designing a circuit that is electrically correct and creating a PCBA that is functional. Note, meeting the above does not mean that this PCBA can be Assembled & Tested efficiently or at all.

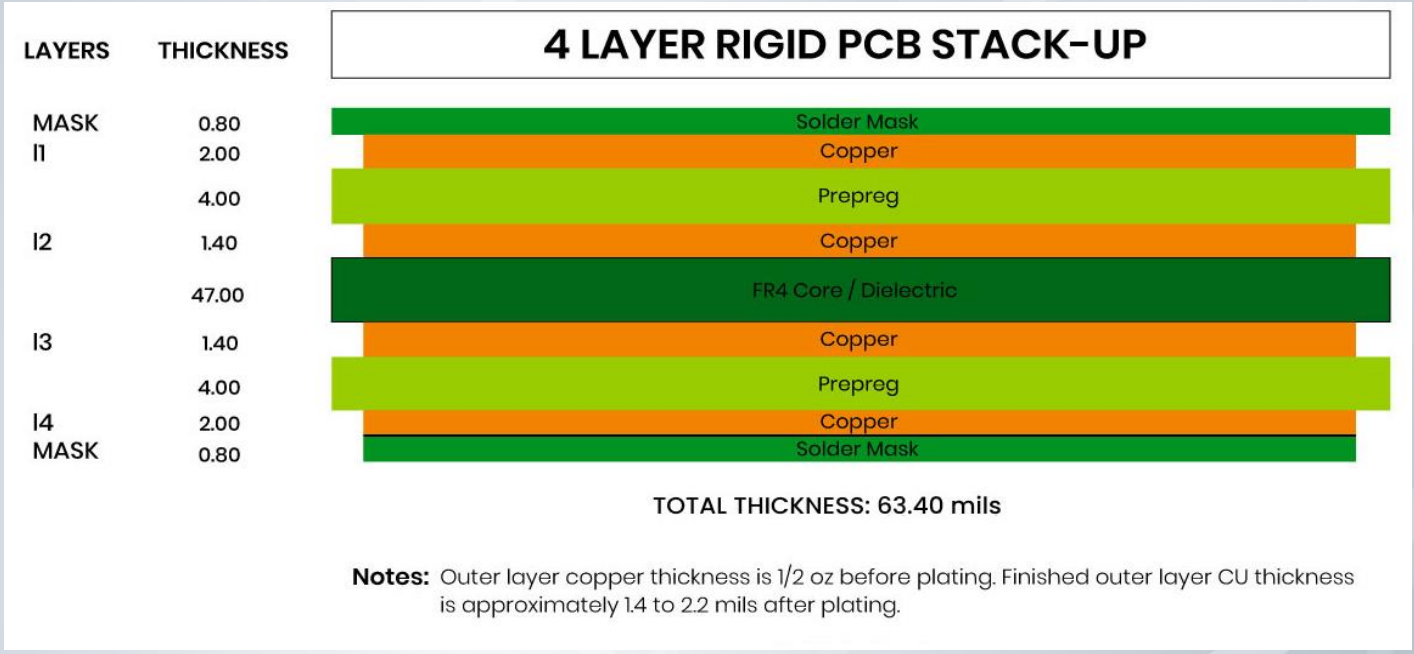
Schematic

- **Reuse proven circuitry whenever possible**
- **Always review Symbols and Land Patterns (proper rotations & centroid positions)**
- **Determine Test Requirements prior to routing**
- **Perform a Comprehensive Schematic Design Review**

Design For Accuracy (continued)

PCB

- Review Assembly House Design Guidelines prior to routing (discuss with Assembly house)
- Determine Layer Stack prior to routing (discuss with Board house)



Design For Accuracy (continued)

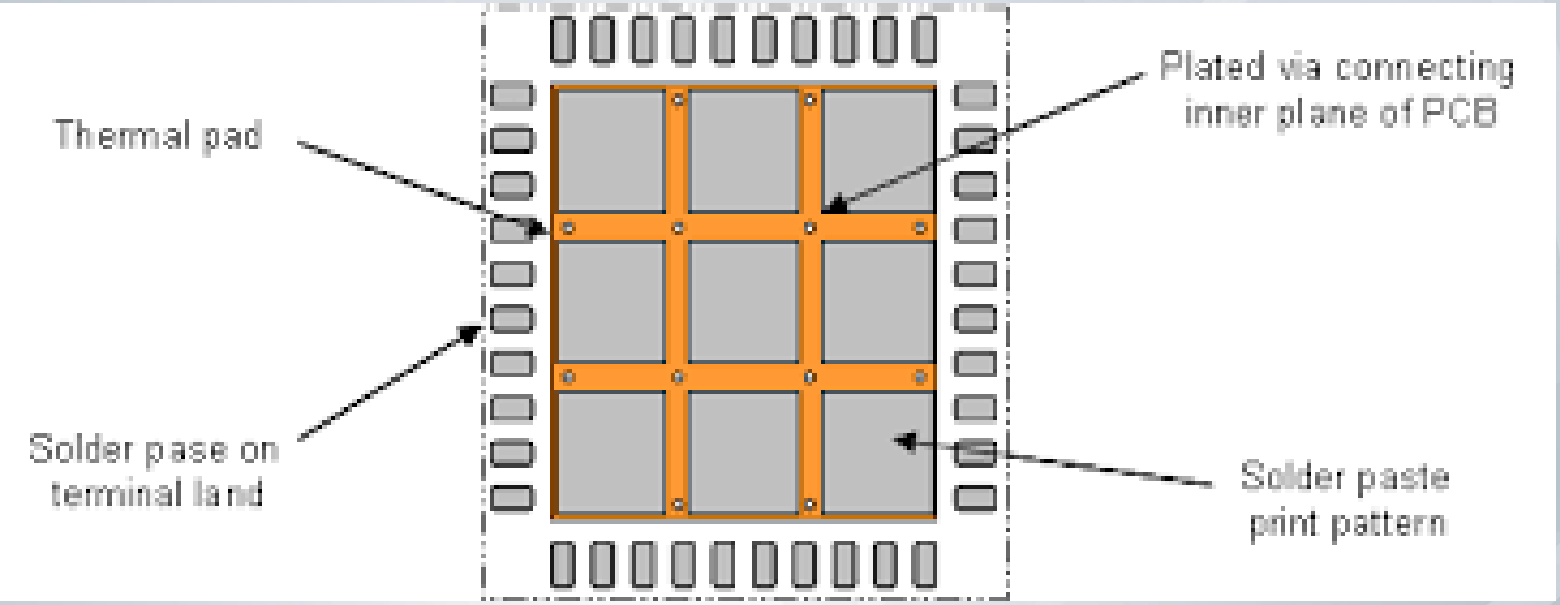
PCB

- Maintaining a balanced layup in relation to the Z-axis median of the board will assure minimum bow and twist. This balance includes the following:
  - Dielectric thickness of layer
  - Copper weight/thickness of layers
  - Sequence/order of the plane vs. signal layers
  - Consider Copper Pours on signal layers which balances the individual layer & reduces the amount of etching of the PCB

Design For Accuracy (continued)

PCB

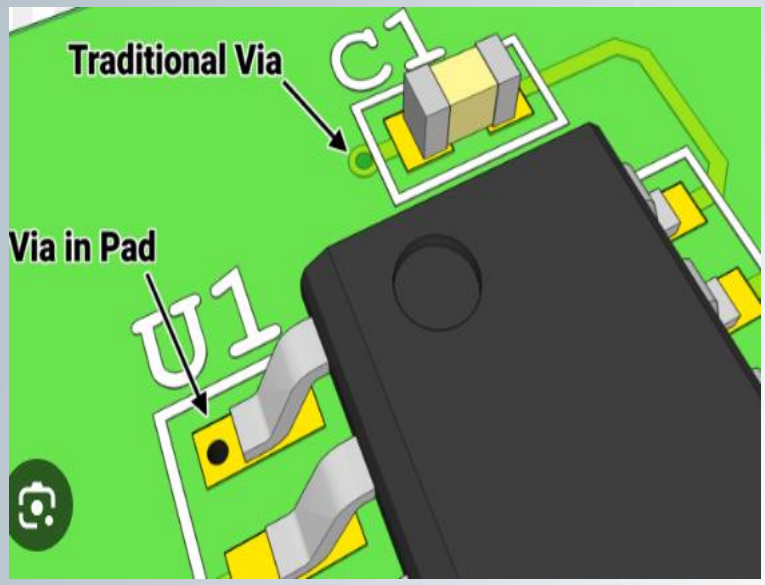
- **Thermal requirements – Bottom Terminated (Exposed) Pads and Thermal Vias; Window Panes; Tenting; Paste Migration considerations**

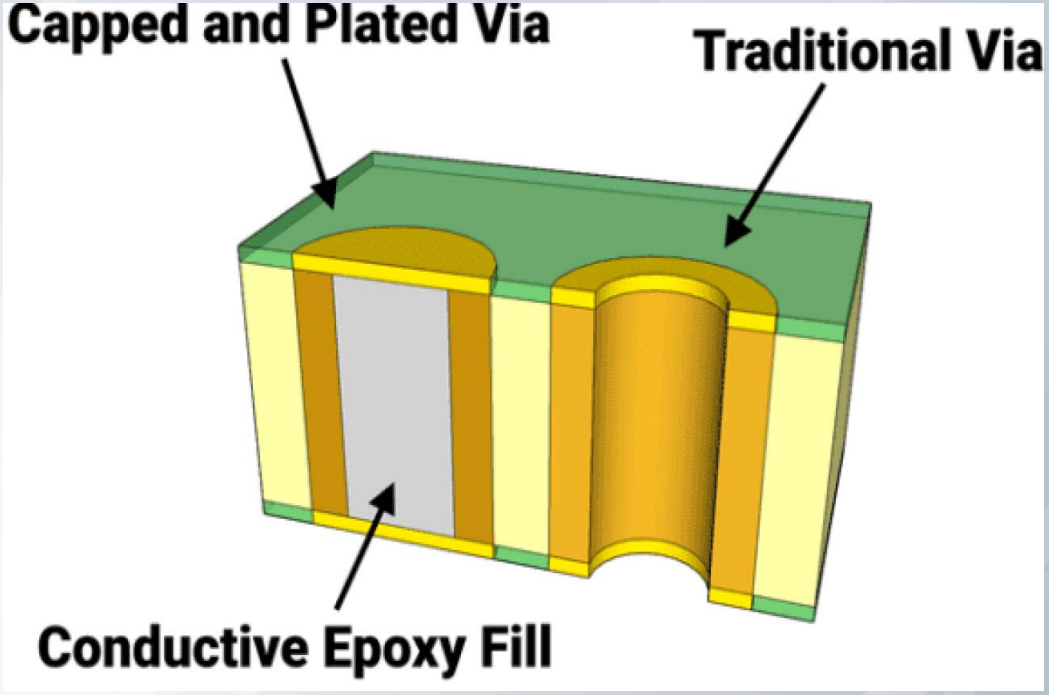


Design For Accuracy (continued)

PCB

- **Avoid Via in pad when possible (plug and plate, cost, etc.)**

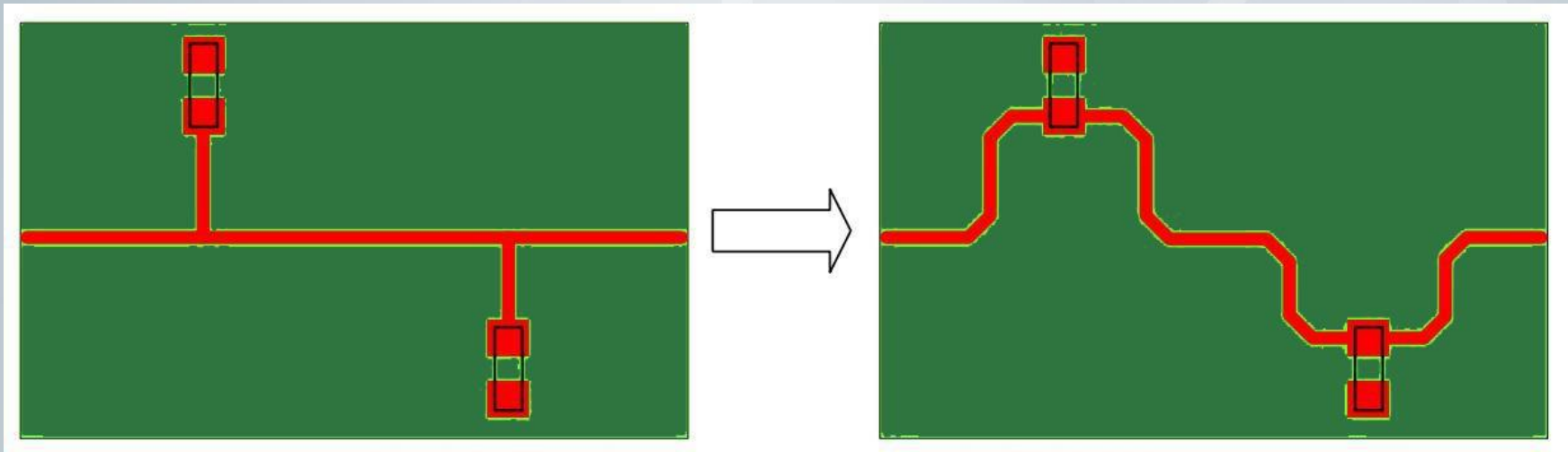




Design For Accuracy (continued)

PCB

- **Limit Stubs and be aware of controlled impedances**
- **Avoid 90-degree angles to minimize reflection**



Design For Accuracy (continued)

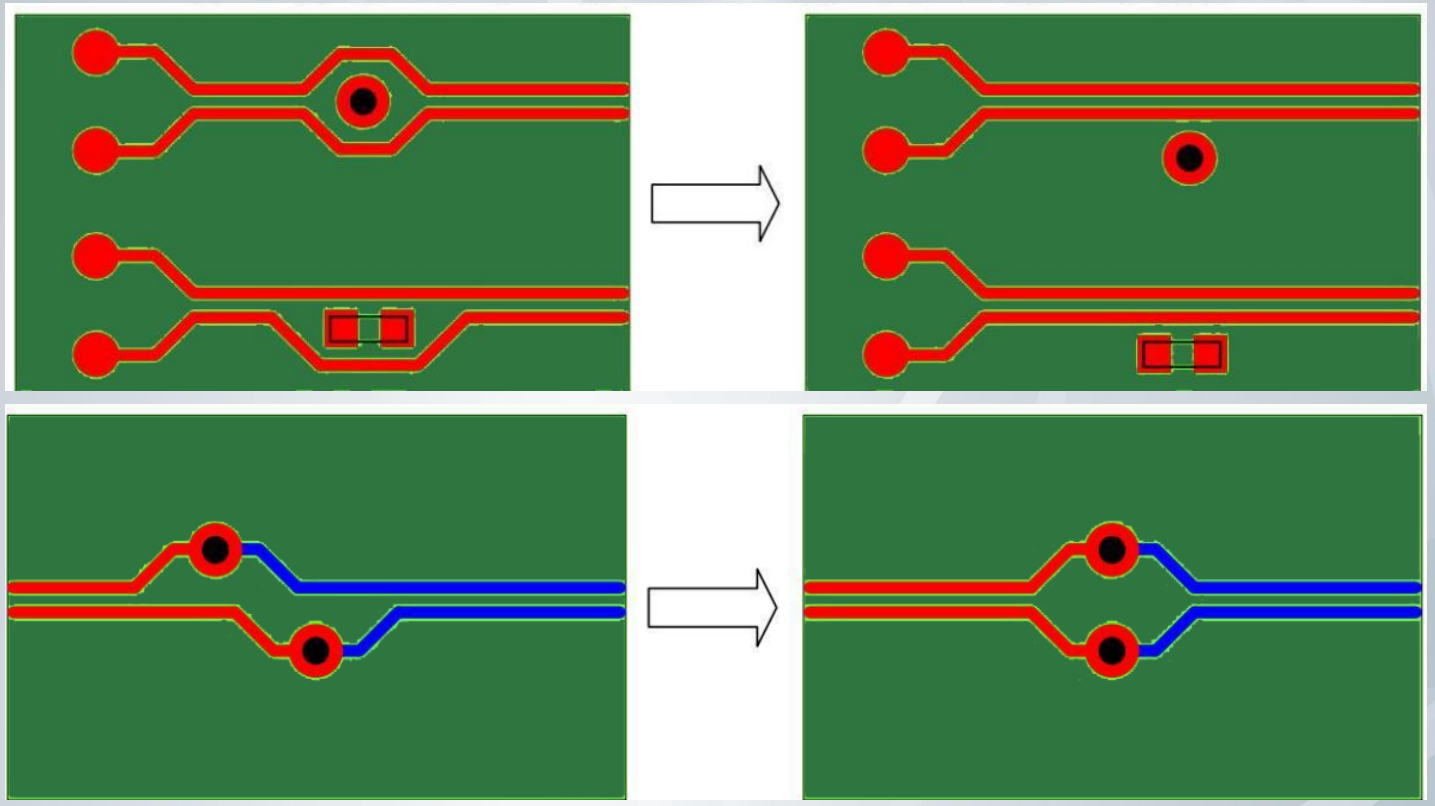
PCB Standard Recommendations:

- **Preferred trace/space: 0.004"/0.004" (0.102 mm)**
- **Minimum trace/space: 0.003"/0.003" (0.076 mm)**
- **Inner signal layers must have a positive polarity**
- **No thieving smaller than a 0.030" (0.762 mm)**
- **Relieve all copper internal to part from route paths by at least 0.010" (0.254 mm)**
- **Provide thieving inside all open and breakaway areas, if possible**
- **Use Tear-Dropping with small pad diameters (<0.02”)**

Design For Accuracy (continued)

PCB

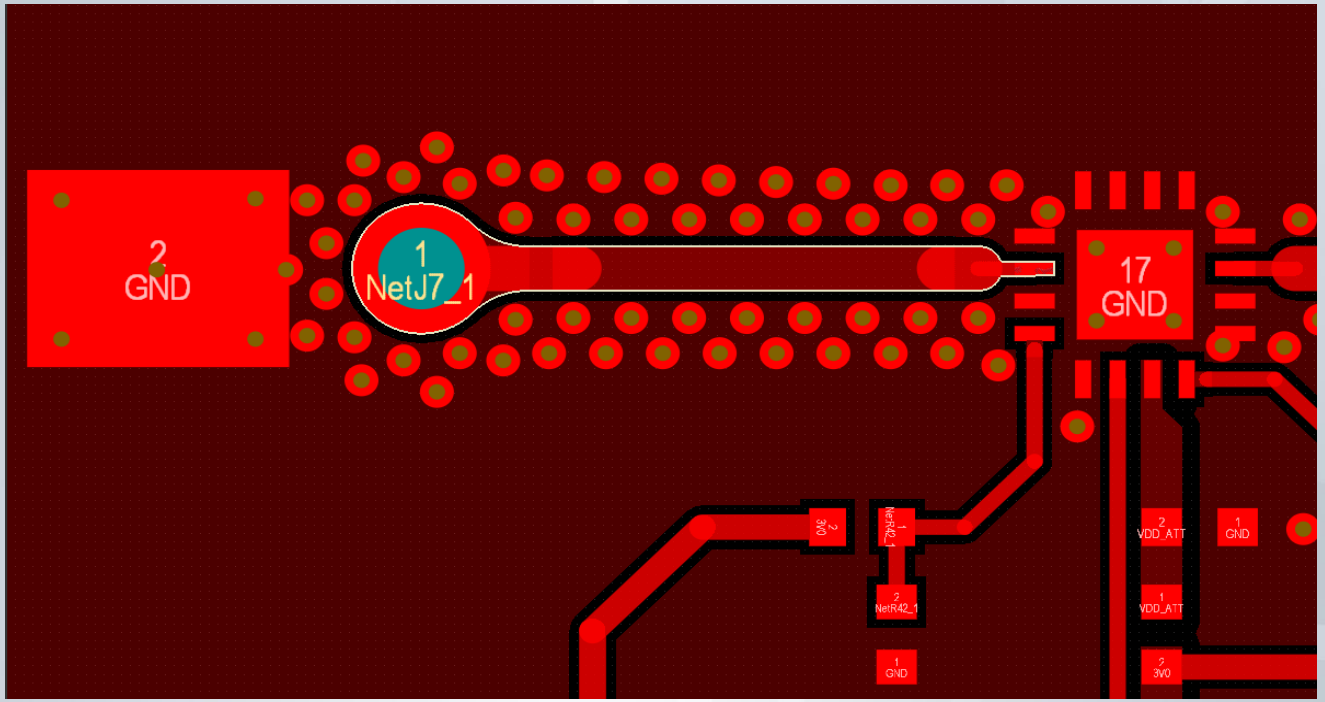
- **Do not place any components or vias between differential pairs (route on same layer if possible)**



Design For Accuracy (continued)

PCB

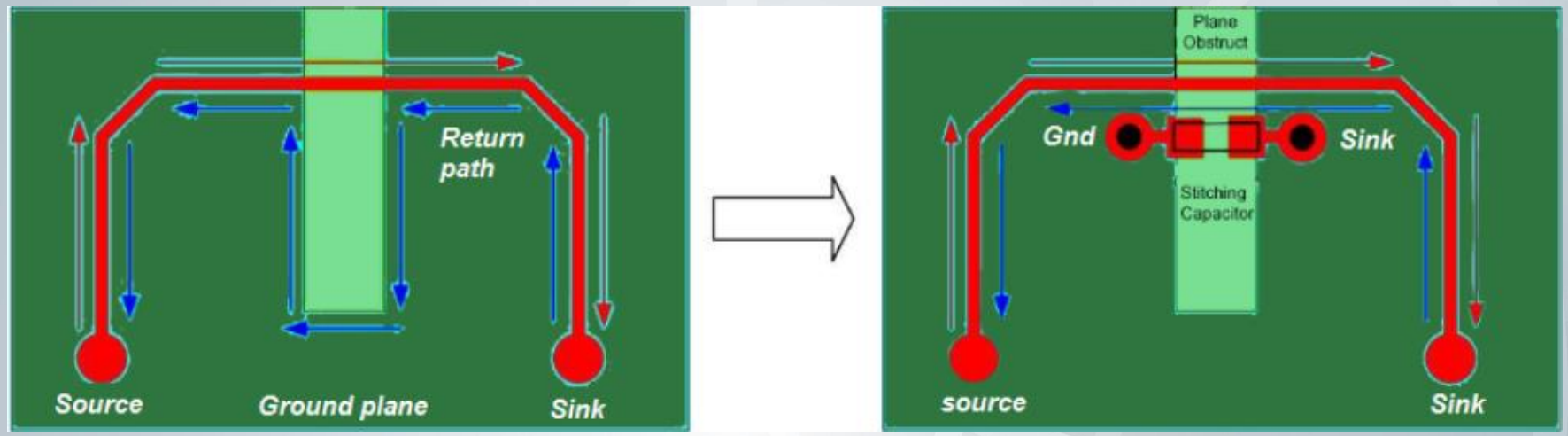
- **Use Via Stitching to enhance ground planes and reduce EMI**



Design For Accuracy (continued)

PCB

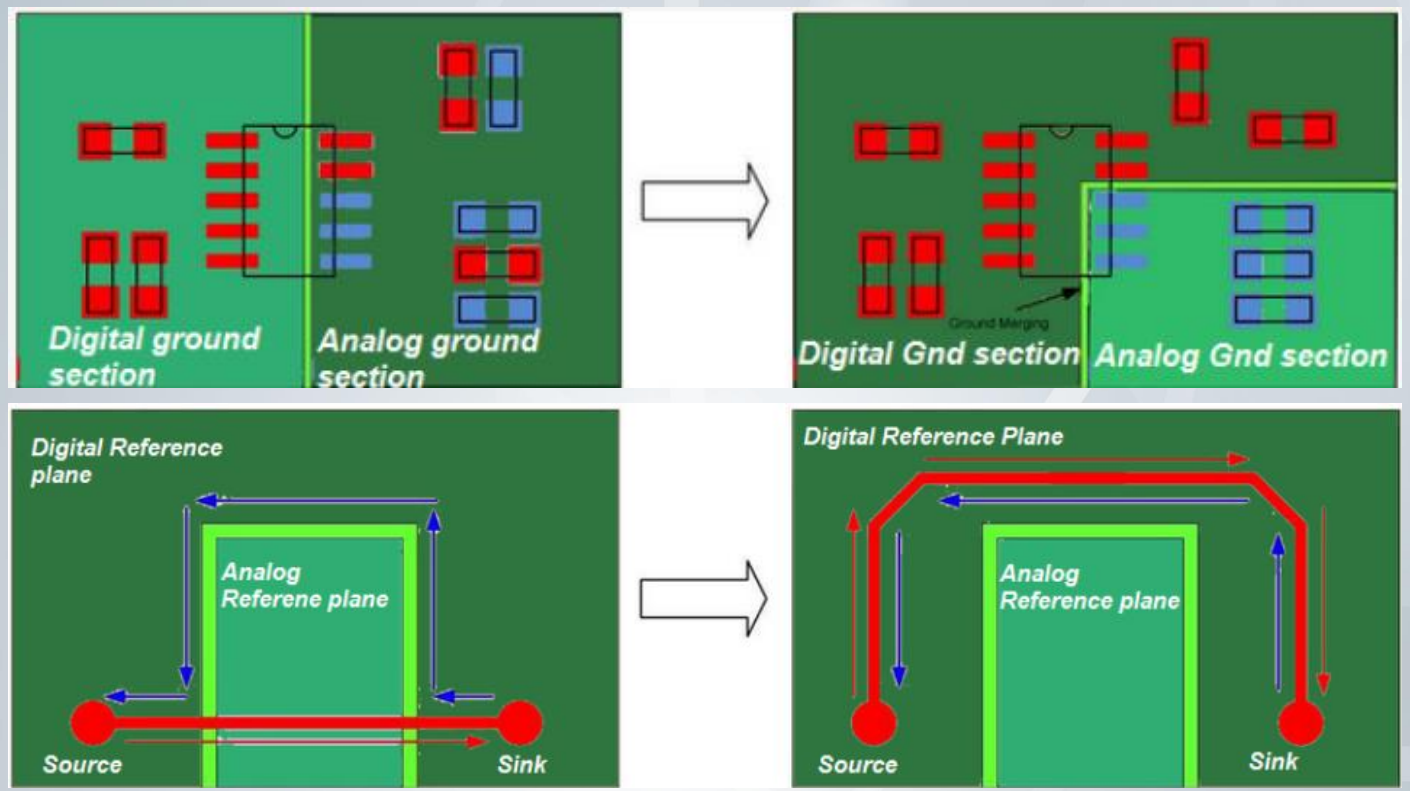
- Do not route signals over a split plane (stitching caps)
- Keep Traces short as possible



Design For Accuracy (continued)

PCB

- **Separate Analog & Digital ground planes**



Design For Accuracy (continued)

PCB

- Perform a Component Layout Drawing Review
- Perform a Thorough Routed PCB Review
- Perform a Gerber Review
- Provide a Clear & Comprehensive Fabrication Package
  - Fabrication Notes
  - Fiducial Drawing
  - Gerber Files
- Provide a Comprehensive Production Package
  - Bill Of Materials (BOM) with Ref Des & MFGPNs
  - Pick & Place File
  - Assembly Drawing(s)
  - Gerber Files

Design For Accuracy (continued)

PCB (Data Output Formats)

- The preferred formats at are IPC-2581 & ODB++ because they provide a unified/consistent data format for all data layers, drill, netlist, etc.
- Gerber RS-274X is the preferred file format versus Gerber RS-274D because it has embedded apertures and formatting within its file, which reduces translation / Interpretation errors.
- Refer to IPC-D-325 and IPC-2610 for the requirements of different drawings.

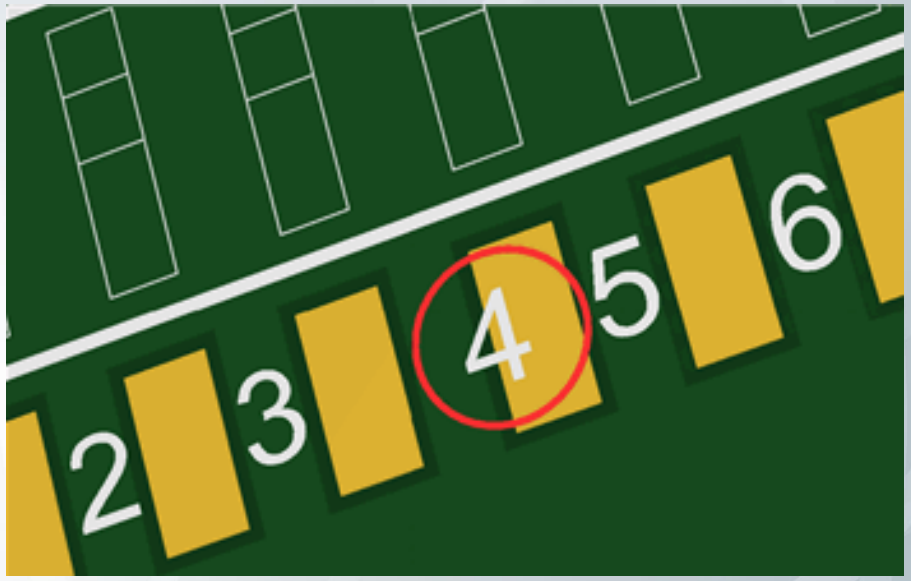
Design For Manufacturability (DFM)

DFM consists of the Best Practices for Designing a PCBA that can be manufactured efficiently. Note, meeting the above does not mean that this PCBA will be Functional or be able to be Tested efficiently.

- **Be aware of wash restrictions (Speakers, solder in batteries, etc. will require no-wash type assembly)**
- **Choose the correct/best PCB plating option for your design (ENIG)**
- **Try to limit MSL of <=3 (MSL 1 is ideal)**
- **Make sure to have Reference Designators for all components**

Design For Manufacturability (continued)

- Avoid Via in pad
- Avoid Silk on pad/solder mask apertures
- Include visible Pin-1 indicators for all components and Polarity Indicators for polarized components



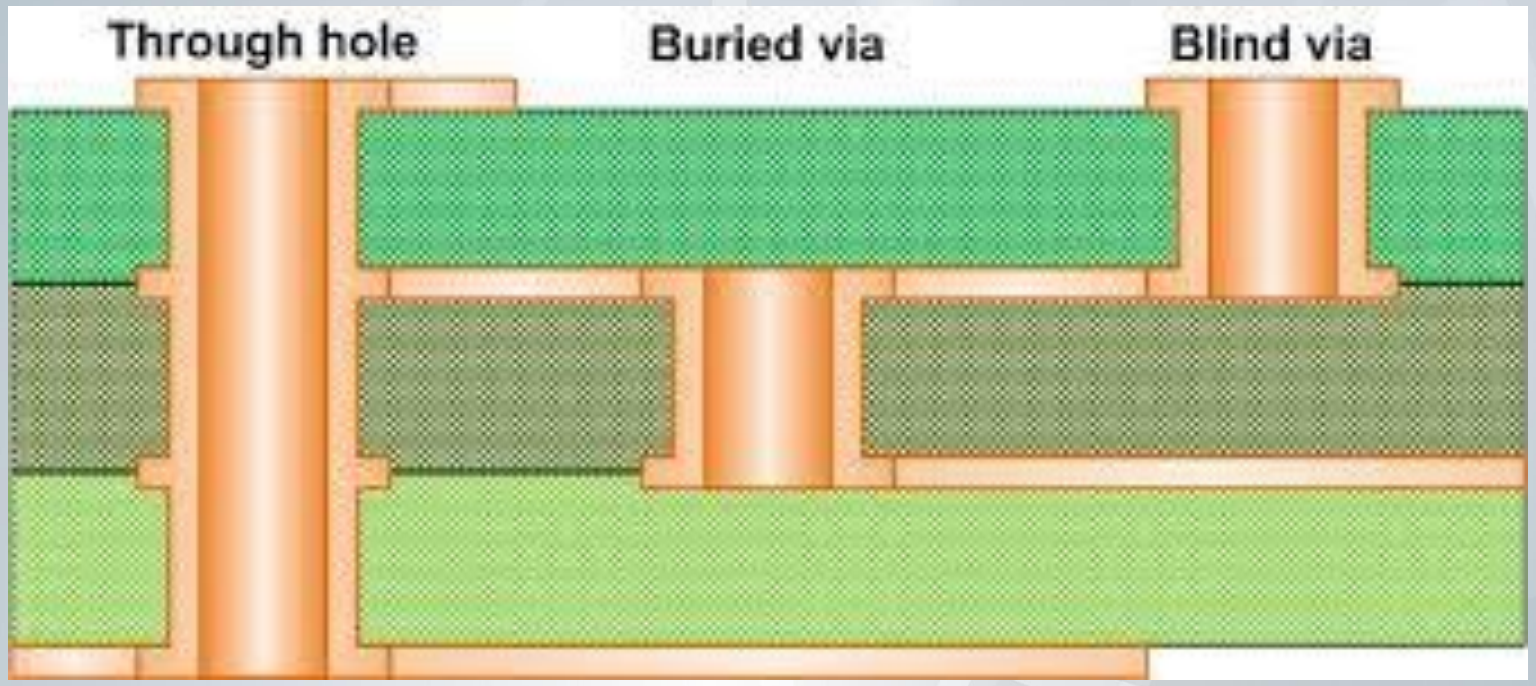
Design For Manufacturability (continued)

PCB

- **Do not place Silk Text over Vias or Pads**
- **To ensure all letters, numbers, and figures are legible on the finished board, height-to-width ratios need to be considered (e.g. character line widths should be greater than 0.006" (0.152 mm) & at least 0.030" (0.762 mm) high).**
- **Space letters at least 0.008" (0.203 mm) apart so they don’t bleed together.**

Design For Manufacturability (continued)

- If possible, limit the number of Blind & Buried Vias

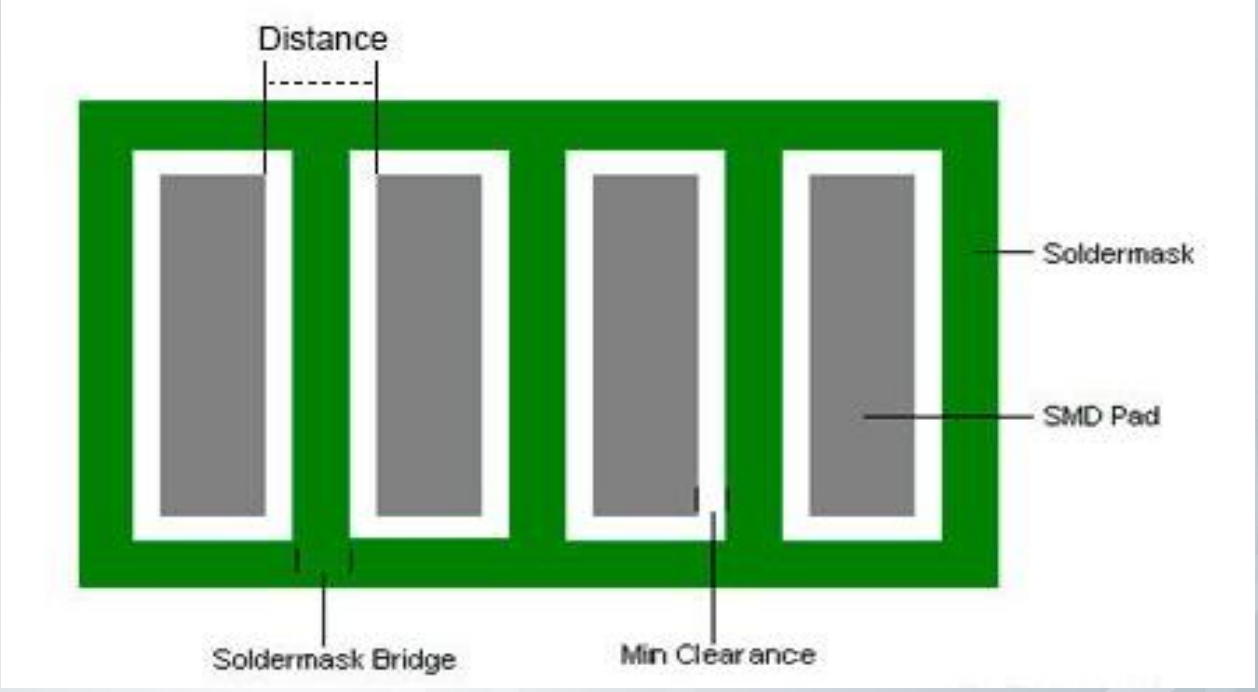


Design For Manufacturability (continued)

- Attempt to place all components on once side of the PCB
- Minimize the number of PCB Layers
- Attempt to have all Through Hole components soldered on the same side of the PCB
- Use standard components with crosses when possible
- Component package type preferences (reel vs. tray vs. tube)

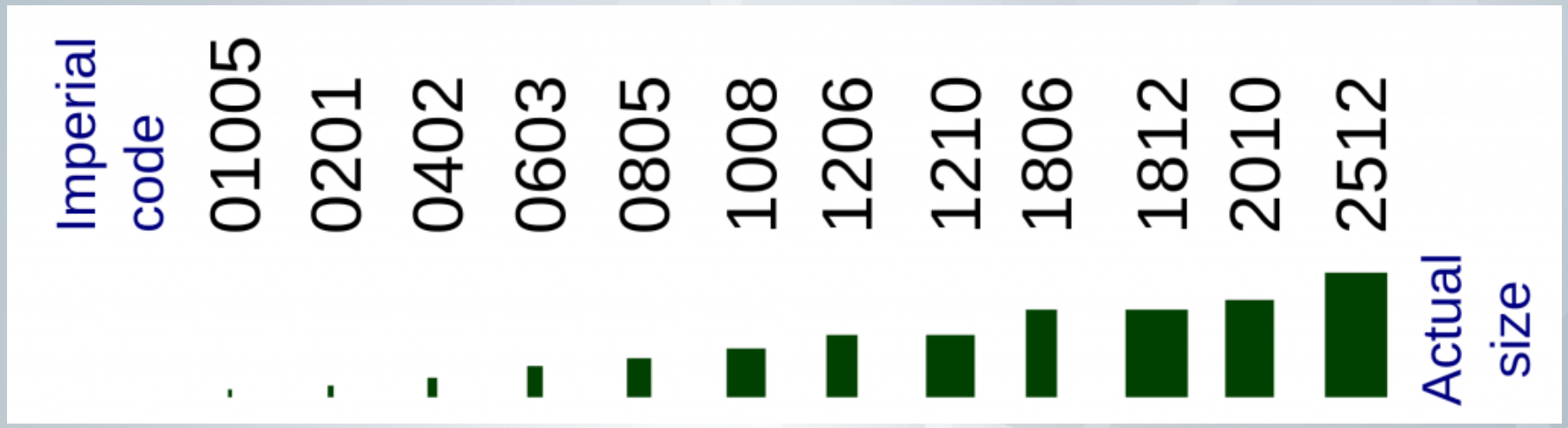
Design For Manufacturability (continued)

- Try to reduce the use of Through Hole components
- Use Solder Mask between pins when possible
- Try to use a Solder Mask with good contrast (not white)



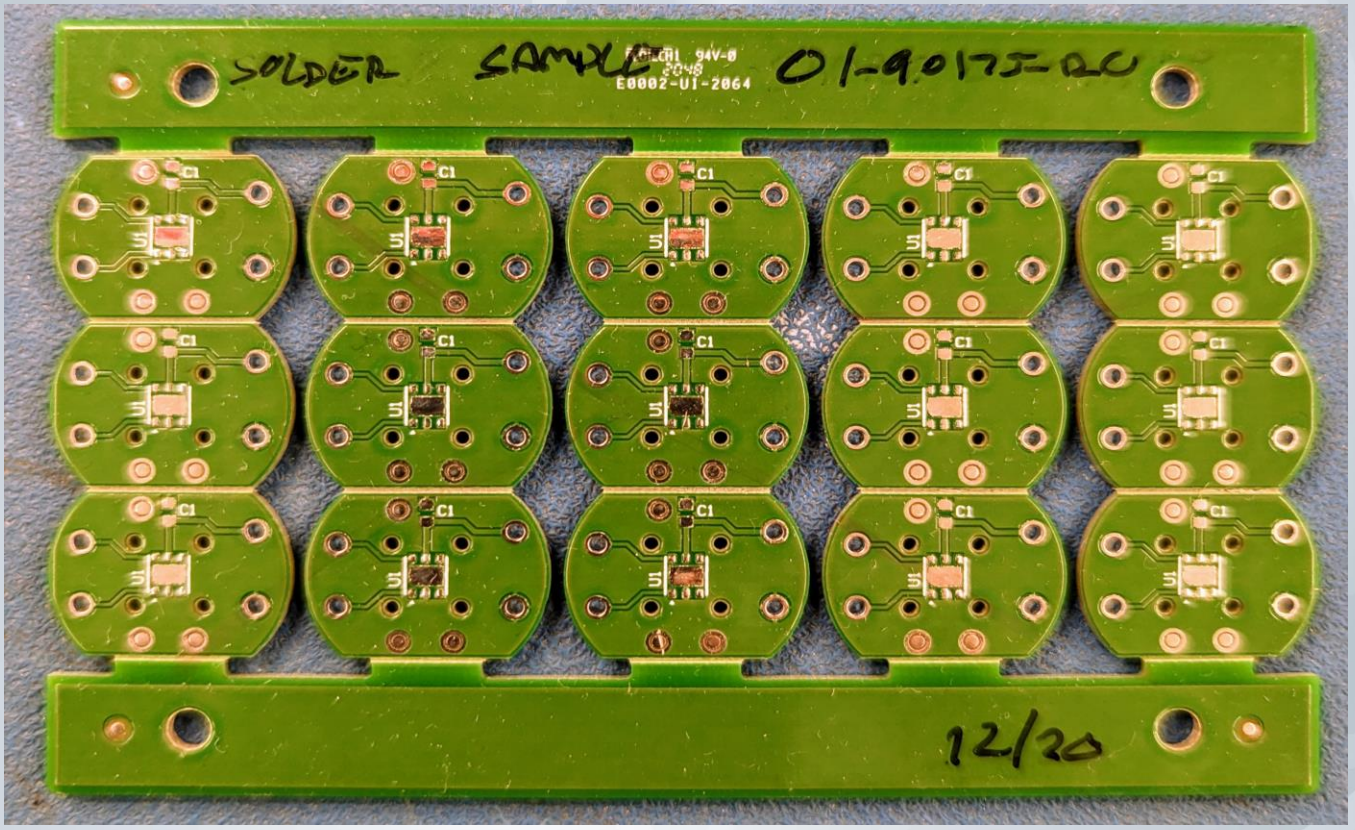
Design For Manufacturability (continued)

- **Do not utilize 0201 or smaller components unless necessary**



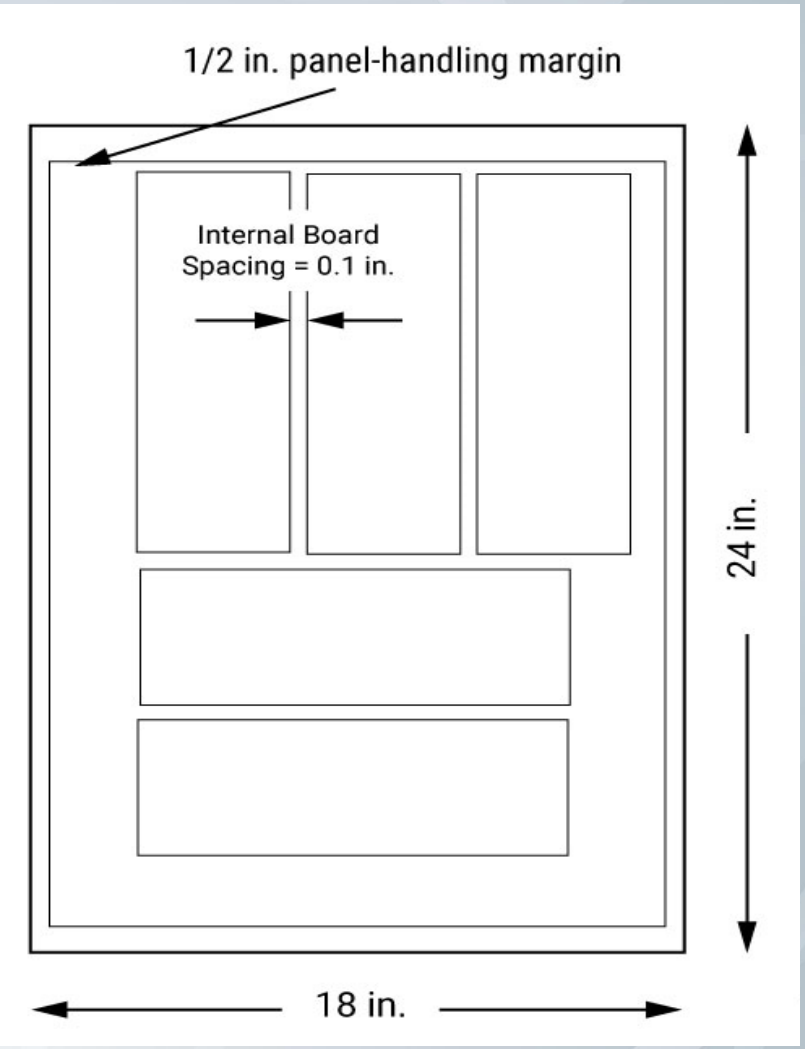
Design For Manufacturability (continued)

- Use 3 Fiducials on Tooling rails to determine direction
- Give consideration to the number of boards in a panel



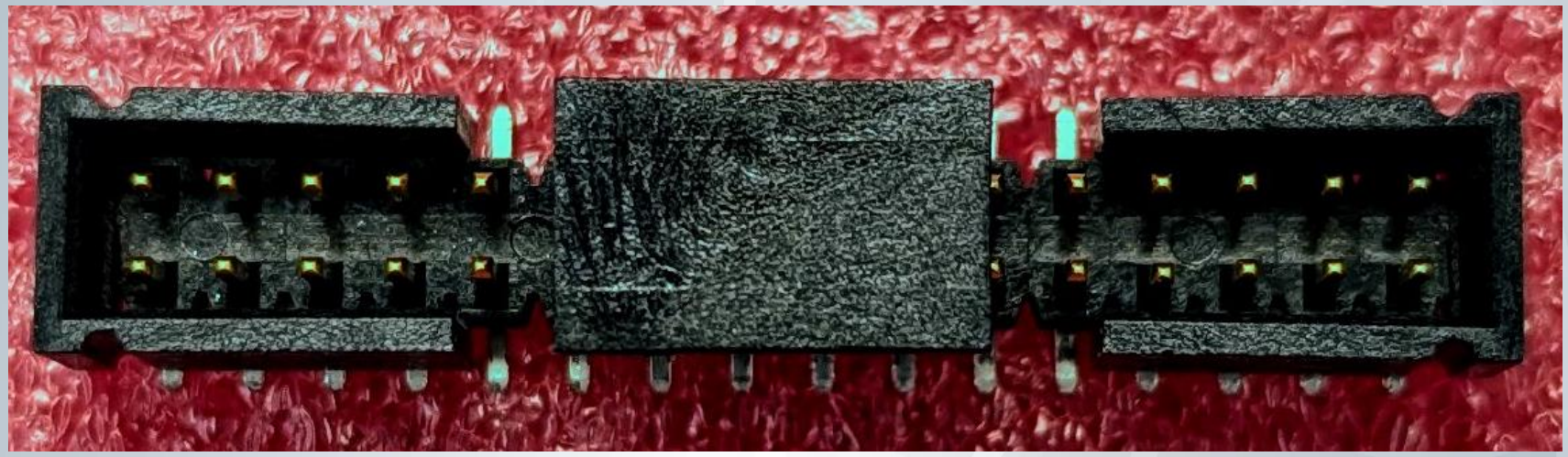
Design For Manufacturability (continued)

- If you are performing the panelization, make sure to define a target panel with > 75% panel utilization.
- The 3 most preferred panel sizes in the USA are 12x18”, 18x24” & 21x24”, with 18x24” being the most common.



Design For Manufacturability (continued)

- Make sure to allocate parts with pick-up tabs when required (connectors)



Design For Manufacturability (continued)

- Minimize secondary operations (reduce part count, efficient placement of parts - automated assembly)
- Be sure to review Assembly House Guidelines

https://ftp.emacinc.com/Tech_Info/CM_files/CM_Board_Design_Guidelines-R1.pdf

Design For Test (DTF)

DFT consists of the Best Practices for Designing a PCBA that can be Tested efficiently. Note, meeting the above does not mean that this PCBA will be Functional or be able to be Manufactured efficiently or at all.

Types of Testing

- **Automated Optical Inspection (AOI)**
- **In Circuit Testing (ICT)**
- **Automated X-Ray Testing (AXT)**
- **Boundary Scan Testing (BCT)**
- **Functional Circuit Testing (FCT)**

- **Automated Optical Inspection (AOI)**
  - **Inspects many of the same things that ICT checks for**
    - **Shorts between component leads & traces**
    - **Solder bridges**
    - **Component top markings**
    - **Soldering & process issues**
    - **Correct location/setting of switches or jumpers**
    - **Presence or absence of or wrong Components**
    - **Misoriented Components**
  - **Cannot detect wrong values without markings**
  - **Very dependent on operator & programming**

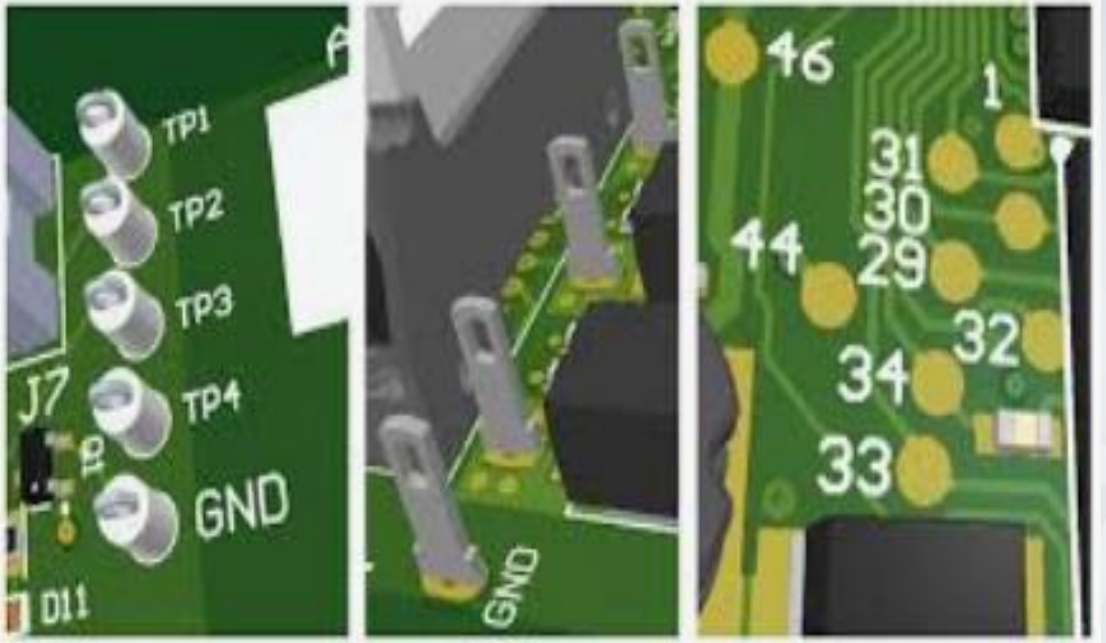
- **In Circuit Testing (ICT; Custom Test Head)**
  - **ICT mainly tests the performance of selected parts**
  - **ICT is a somewhat Universal Tester with a Custom Head & Test Criteria**
  - **Advantages:**
    - **Can detect up to 99% of manufacturing Defects**
    - **Very fast Testing (good for high volume)**
    - **Does not requiring powering the whole board**
  - **Disadvantages:**
    - **Can be Expensive + Custom Test Head**
    - **Limited access to test points on dense PCBs**
    - **The Test Head & programs may need to be redesigned for each new board revision**

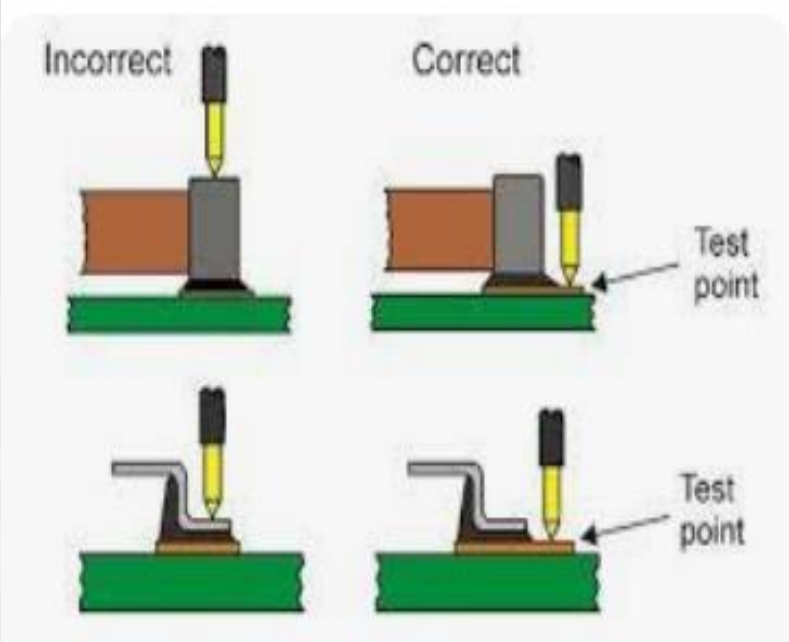
- **Functional Circuit Testing (Continued)**
  - FCT is a Custom Tester specific to the UUT
  - Requires good planning & known quantity needs
  - Can be used in Lot Sampling (Statistical) scenario
  - Advantages:
    - Best overall test (assures customer satisfaction)
    - Can be less expensive depending on FCT design
    - Less complex than other Testing methods
  - Disadvantages:
    - Can be Time consuming especially when paired with Programming
    - Can add greatly to production test time & cost
    - Less accurate in finding all faults

- **Functional Circuit Testing (FCT)**
  - **Types of Functional Testers**
    - **Level I: Simple Manual Test-Set (requires connecting of cables & manual logging.**
    - **Level II: Simple Manual Test-Set (requires connecting of cables but automatic logging.**
    - **Level III: Pogo Pin Test-Set (Few if any cables to connect and automatic logging.**
    - **Level IV: Pogo Pin High Volume Test-Set (Tests Multiple Boards at same time. For more info goto: https://ftp.emacinc.com/Tech_Info/CM_files/Test_Fixture_Level_Summary-R1.pdf**

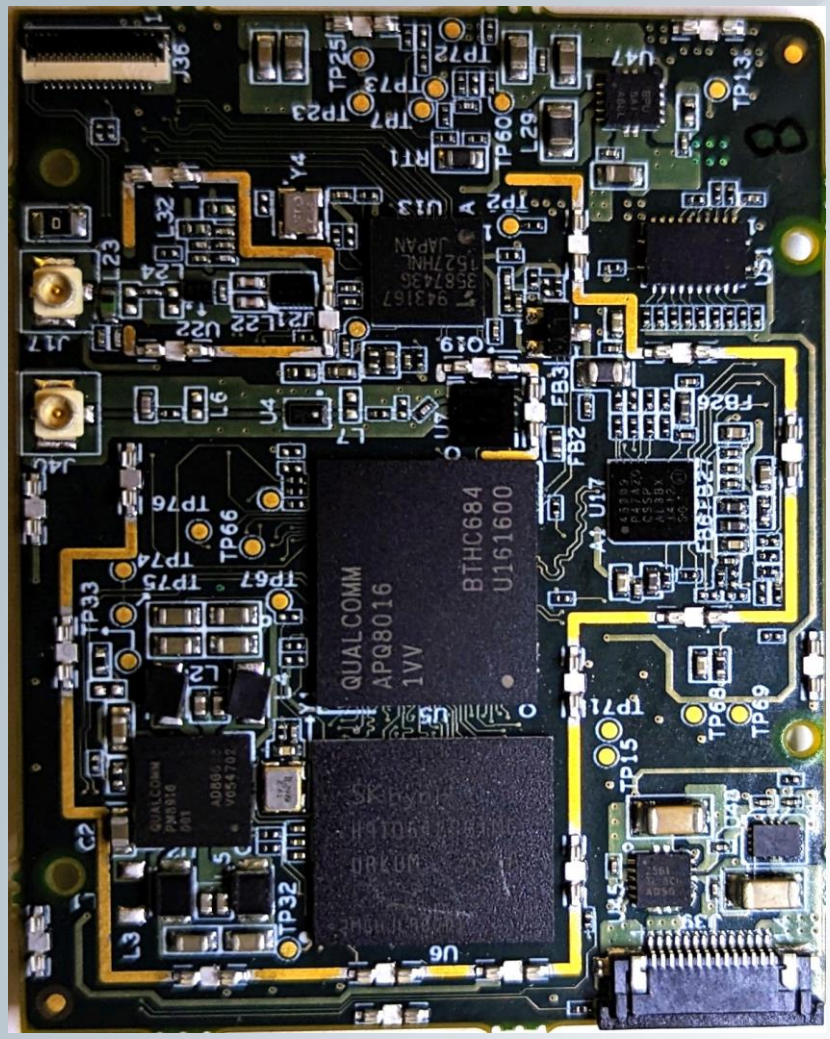
Design For Test

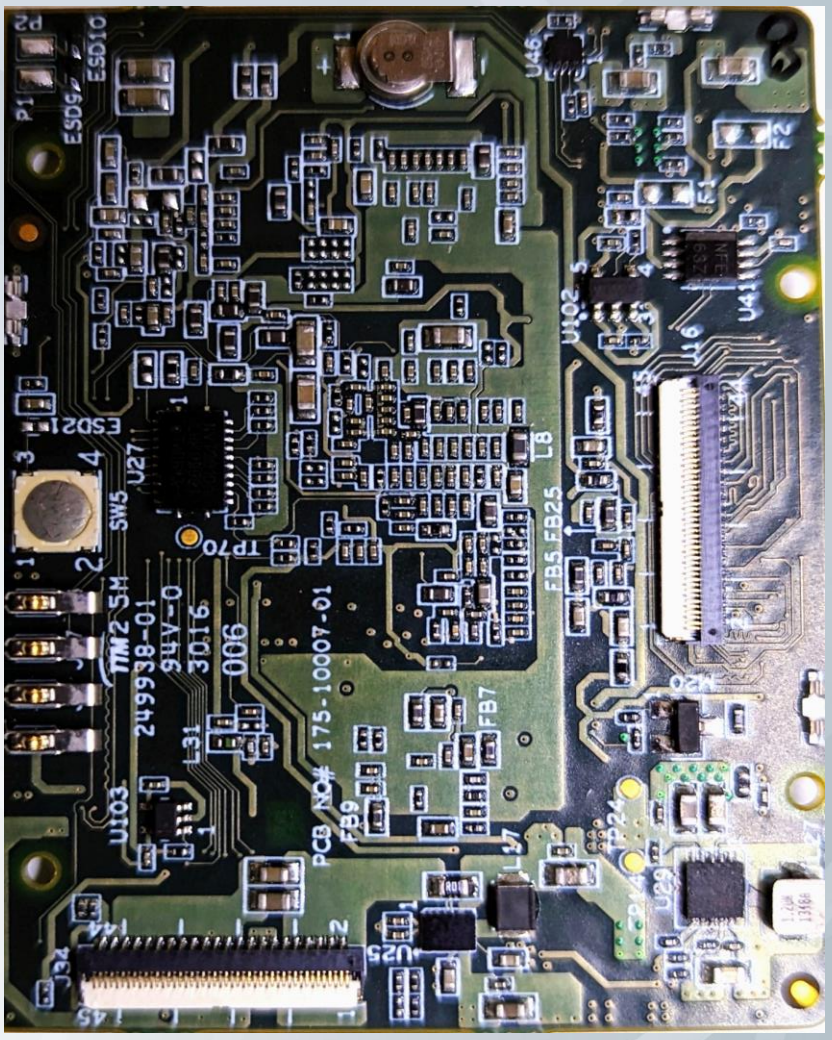
- **Test Targets:**
  - **Test Pad; Via (untented; best if solder filled)**
  - **TH Pin (known length)**
  - **Turrets/Loops/Lugs; (no SMT leads)**





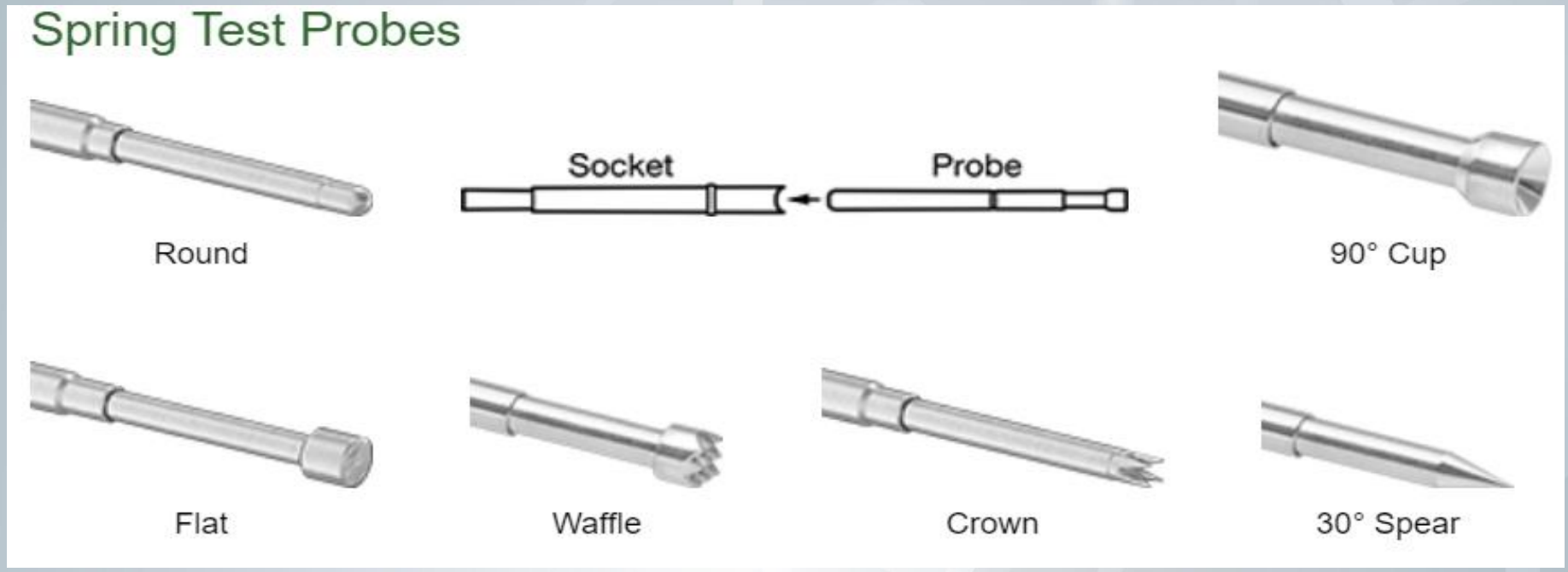
Actual PCB with Test Points Top & Bottom





Design For Test (Continued)

- **Test Probe Types: (Pogo Pins) Round, Cup, Flat, Waffle, Crown, Spear, Chisel**



- **Try to keep all Test Points on one side of the board & Distribute Targets evenly across the PCB**

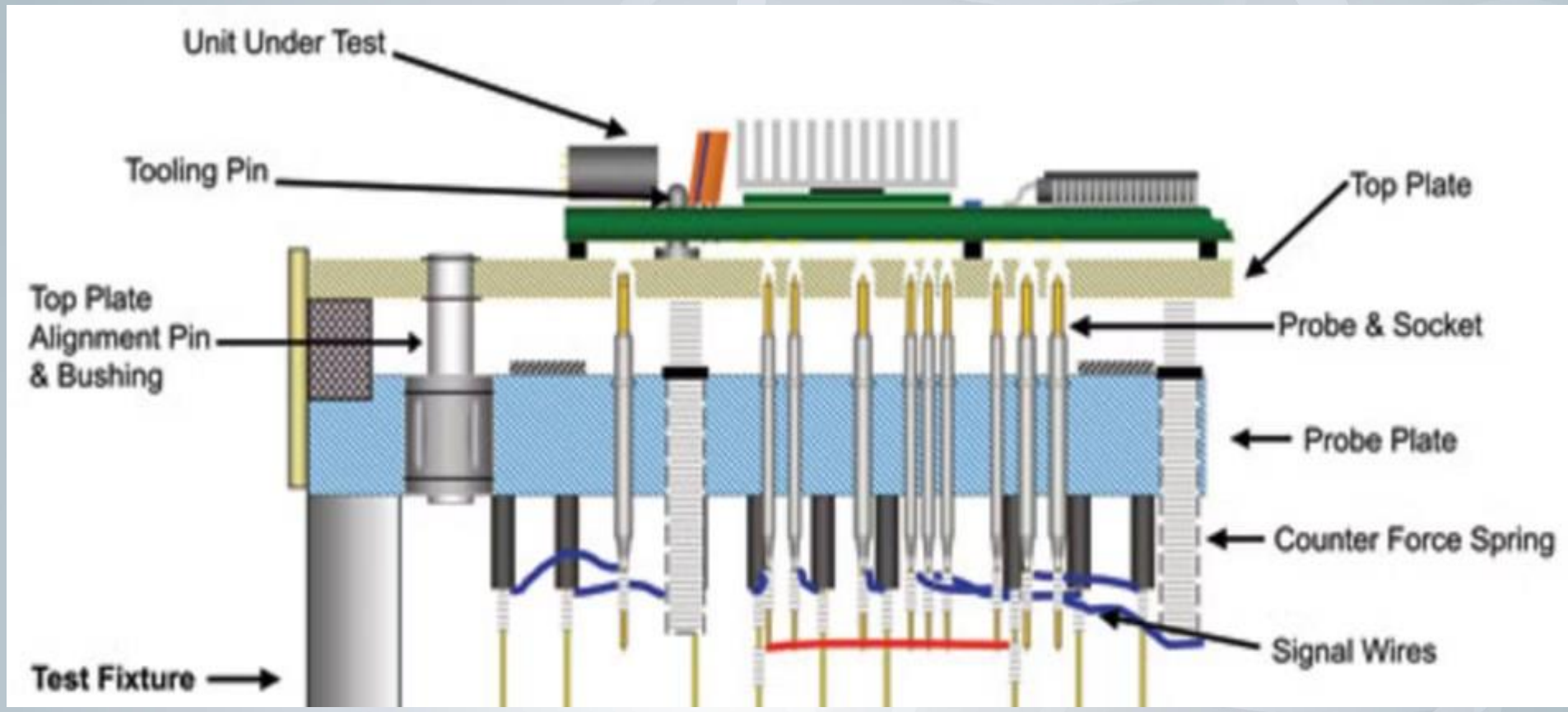
Design For Test (Continued)

- Test Probe Sizes: Best .1”; Adequate .075”; Tolerable .050” & .039”
- Test Target Size: Best > .035”; Adequate > .028”; Tolerable < .020”
- Test Target Clearance: minimum of .018” annular ring that is free of components
- Test Target Edge Spacing: Targets should be .125” from board edge
- Tooling Holes: Minimum of two 0.125” holes with .2” clearance
- Leave adequate space for Push Rods (Hold Down Posts)

Design For Test (Continued)

- Do not put Test Points under BGAs
- Use multiple Test Points for Power Connections
- Be sure to distribute Test Points across the board to prevent Flex Stress
- Be aware of the total force of all pogo pins (~1 newton per pin)
- Try not to use No-Clean Flux in your manufacturing process if using a Test-Set with Pogo Pins

Bed of Nails Test-Fixture Example



FCT Test-Set Software

- Considerations
  - Running the Test SW on the UUT
  - Running the Test on a Computer
  - Using the Test-Set for Repair as well as Testing
- Data Logging & Reporting
  - Serial#
  - Time, Date, Duration & Tester
  - Pass/Fail Status & What Failed
  - Measurements of Key Test Points a (Voltage, Current, Frequency, etc.)
  - Board Tracker (EMAC's Logging DB)

FCT Test-Set Software (Continued)

- What to Report
  - First Pass Yield
  - What Failures are most prevalent
  - Average Test Time
- Test/Program Application (TPA)
  - TPA - Is a Custom Application written by EMAC to allow the efficient reuse of Test SW and User Interface for Programming & Testing PCBAs
  - TPA Application Programming Interface (API)
    - Stand Alone use or with Back-End Server

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EQUIPMENT MONITOR AND CONTROL

ISO 9001: 2008

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PERRY JOHNSON REGISTRARS, INC.

ANAB ACCREDITED ISO/IEC 17021 MANAGEMENT SYSTEMS CERTIFICATION BODY

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