SoM-A5D36

User Manual

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1 Introduction

This document describes EMAC's SoM-A5D36 System on Module (SoMs). The SoM-A5D36 is a System on Module, designed to be compatible with EMAC's 200-pin SODIMM form factor. This module is built around the ATSAMA5D36 ARM based microcontrollers, which provides several of its key features. The SoM-A5D36 has an onboard Gigabit Ethernet PHY, 6 serial ports, an RTC, onboard eMMC flash, Serial NOR Flash, and SDRAM. In addition to the standard SoM features, the SoM-A5D36 also features a fast 32-bit core, open source software support, and a wide range of controller I/O pins.

1.1 Features

- **Small, 200 pin SODIMM form factor (2.66" x 2.384")**
- **Atmel ARM Cortex-A5 ATSAMA5D36 536MHz Processor**
- **10/100/1000 BaseT Ethernet with on-board PHY**
- **RMII Interface for additional 10/100 BaseT PHY**
- **6x Serial ports, 1x with full handshake and 3x with RTS/CTS handshake**
- **2x USB 2.0 (High Speed) Host port**
- **1x USB 2.0 (High Speed) OTG Host/Device port**
- **Up to 512MB of LPDDR2 SDRAM**
- **4GB of eMMC Flash**
- **16MB of NOR Serial Flash**
- **2x SD/MMC Flash Card Interfaces**
- **Battery-backed Real-Time Clock**
- **2x SPI ports**
- **2x I2C ports**
- **1x I2S Audio port**
- **2x CAN ports**
- **6-Channel 12-bit Analog-to-Digital converter with 4-wire Touchscreen Interface**
- **Image Sensor Interface (ISI), ITU-R BT. 601/656**
- **Timer/Counters and Pulse Width Modulation (PWM) ports**
- **Graphic LCD Interface with 2D acceleration with 2048x2048 Resolution or up to 720p**
- **32-bit True Random Number Generator**
- **Typical power requirement less than 1 Watt**
- **JTAG for debug, including real-time trace**
- **FREE Qt Creator IDE with GCC & GDB development tools**

2 Hardware

2.1 Specifications

- **CPU:** Embedded Atmel ATSAMA5D36 processor running at 536MHz
- **Flash:** 4GB eMMC Flash and 16MB of Serial Data Flash
- **RAM:** 512MB 133 MHz LPDDR2
- **Flash Disk:** 4-bit SDHC/MMC interface
- **System Reset:** Supervisor with external Reset Button provision
- **RTC:** Real-Time Clock/Calendar w/ battery-backed provision using 32-bit free-running counter
- **Timer/Counters:** 5x 2-channel, 32-bit timers/counters with capture, compare, and PWM
- **PWM:** 4x PWM channels, one with complimentary outputs
- **Watchdog Timer:** External Watchdog Timer (MAX6747)
- **Digital I/O:** 32x General Purpose I/Os with 16 mA drive when used as an output
- **Analog I/O:** 6-channel, 12-bit Analog-to-Digital converter (ADC)
- **Power:** Power Management Controller allows selectively shutting down on-processor I/O functionality and running from a slow clock
- **JTAG:** JTAG for debug, including real-time trace
- **Clocks:** PLL synthesized 8MHz, 200KHz, 14.3MHz clock outputs

Serial Interfaces

- **UARTS:** 6x serial TTL level serial ports with Auto RS485 and most with handshaking (each UART requires external RS level shifting)
- **SPI:** 2x High-Speed SPI ports with Chip Selects
- **Audio:** I2S Synchronous Serial Controller with analog interface support
- **USB:** Dual USB 2.0 High Speed Host and single USB 2.0 High Speed Device ports
- **I2C:** 2x I2C ports

Ethernet Interface

- **MAC:** ATSAMA5D36 on chip MAC
- **PHY:** Microchip Technology KSZ9031 Gigabit PHY with software shutdown
- **Interface:** IEEE 802.3u 10/100/1000 BaseT Fast Ethernet (requires external magnetics & Jack)

Bus Interface:

- Local Bus accessible through SODIMM provides 22 address lines, 16 data bus lines, and control lines.

Mechanical and Environmental:

- **Dimensions:** SODIMM form factor with the length dimension extended (2.66" x 2.384")
- **SODIMM TYPE:** 200 Pin DDR1 (not compatible with DDR2)
- **Power Supply Voltage:** +3.3 Volts DC +/- 5%
- **Power Requirements (typical):**
  - 3.3 Volts @ 300 mA (less than 1 watt)
  - Max current draw during boot process: 340 mA
  - Constant busy loop: 260 mA
  - Idle system: 245mA
- **Operating Temperature:** -40 ~ 85° C (-40 ~ 185 ° F), fanless operation.
- **Operating Humidity:** 0% ~ 90% relative humidity, non-condensing

2.2 Real-Time Clock

The SoM-A5D36 has an embedded Real-time Clock. Battery backup is provided from the carrier board using the VSTBY pin. The SoM-A5D36 will retain the RTT value register during reset and hence use it as an RTC. The RTC has the provision to set alarms that can interrupt the processor. For example, the processor can be placed in sleep mode and then later awakened using the alarm function.

2.3 Watchdog Timer

The SoM-A5D36 provides an external Watchdog Timer/ Supervisor (MAX6747) with an extended watchdog timeout period of 1.42 seconds (±10%). Upon power-up the Watchdog is disabled and does not require pulsing. To start the Watchdog, it must first be enabled. This is done by configuring port line PD8 as an output and setting it low in software. Once enabled, the Watchdog should be pulsed, using port line PD6, continually every 1.28 seconds or faster to prevent the Watchdog from timing out and resetting the module. If you are using the watchdog to force a system reset, you may need up to 1.56 seconds of inactivity before the Watchdog reset will occur. The watchdog is automatically disabled upon reset but it can also be disabled by setting PD8 high.

2.4 External Connections

The SoM-A5D36 connects to a carrier board containing its connectors, power supply and any expansion IO, through a standard ENIG-plated (Electroless Nickel Immersion Gold) SODIMM 200-pin edge card connection shown below.

The SoM model will fit in any standard 200-pin SODIMM socket. These connections are designed to be compatible with all EMAC 200-pin SoM products. See EMAC SoM 200-pin SODIMM Pinout

Specification to see how other 200-pin SoM pinouts line up with the SoM-A5D36's pinout. The use of the DDR SODIMM form-factor for EMAC's SoMs is a sound choice that has been proven rugged and reliable in the laptop and embedded SBC markets.

The remainder of this section describes the pinout as it applies specifically to the SoM-A5D36 processor.

2.4.1 External Bus

The SoM-A5D36 provides a flexible external bus for connecting peripherals. The CPLD of the SoM-200GS connects through a subset of these connections. The WKUP pin has a Maximum input voltage of 3.3V (pulled up on-module to 3.3V) and Shutdown has a maximum output voltage of 3.3V. The Flash WP for the Serial Flash is active-low and pulled up on-module.

Table 1: External Bus Interface

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
145	GP_CSA	NCS1	PE27	General Purpose Chip Select CS0
146	GP_CSB	NCS2	PE28	General Purpose Chip Select CS4
147	GP_CSC	NCS3	N/A	General Purpose Chip Select CS2
148	GP_CSD/Shutdown	PWRDN	N/A	Processor Shutdown Output
149	WR	NWE	N/A	Write Signal
150	RD	NRD	N/A	Read Signal
151	RST_IN	NRST	*	Processor Reset
152	RST_OUT	~RST_OUT	*	Processor Reset
153	WAIT	NWAIT	PE30	Shutdown Control
154	~FLASH WP	*	*	Serial Flash Write Protect
54	WAKEUP	WKUP	N/A	Processor Wakeup Input
157	BOOT_OPTION0	BMS	N/A	Boot0 Option Select
158	BOOT_OPTION1	*	*	Boot1 Option Select
175-193	A0 – A18	A0 – A18	PE0-PE18	Address Bus
194	A19	A19	PE19	Address Bus line A19
195	A20	A20	PE20	Address Bus line A20
196	A21	A21	PE21	Address Bus line A23
159-174	D0 - D15	D0 – D15	N/A	Data Bus

*The RST_IN pin is an active low input that drives the processor reset pin. The RST_OUT pin is an active low output that is driven low by either the watchdog timer or a software reset. The ~FLASH_WP pin is an active low input that prevents the serial NOR flash from being written to. The BOOT_OPTION1 pin is an input that disables the serial NOR flash.

2.4.2 JTAG

The SoM specification allows for access to the JTAG lines for the ATSAMA5D36 processor. These connections will allow the Flash to be programmed in circuit via a program running from the processor and also the capability to debug software.

Table 2: Processor JTAG

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
139	JTAG_TCK	JTAG_TCK	JTAG Clock
140	JTAG_TDI	JTAG_TDI	JTAG Serial In
141	JTAG_TDO	JTAG_TDO	JTAG Serial Out
142	JTAG_TMS	JTAG_TMS	JTAG Operation Mode
143	JTAG_TRST	JTAG_TRST	Test Reset Signal
144	JTAG_RTCK	NC	Dynamic Clock Sync

2.4.3 I2C

The SoM-200 specification calls for a two-wire I2C port. Some Carrier boards connect an EEPROM to this port in order for the Linux OS to self-identify the Carrier board.

Table 3: I2C (EEPROM)

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
29	CLK	TWCK0	PA31	Clock Pin
30	DATA	TWD0	PA30	Data Pin

There is an additional available I2C interface that is shared with the USB OTG pins. This additional I2C port can be utilized on a custom carrier board.

Table 4: Additional I2C Port

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
10	USB_OTG_VBUS	TWCK1	PC27	Clock Pin
40	USB_OTG_ID	TWD1	PC26	Data Pin

2.4.4 Ethernet

The SoM-A5D36 provides a Microchip Technology KSZ9031 10/100/1000 Ethernet PHY IC on board. Carrier designers need only run these lines through the appropriate magnetics layer to have a functional Ethernet connection. Remember the RX and TX lines are differential pairs and need to be routed as such.

The LED/configuration pins' state at reset determines the PHY address. These pins are pulled to set the PHY address to 0x01 by default. The address can be changed by pulling these lines to a different value on a custom carrier board. This can be especially useful if an additional PHY is added to a custom carrier by accessing the RMII pins described below.

Table 5: Ethernet 1000 BaseT Interface

SODIMM Pin#	SoM Pin Name	KSZ9031 Pin Name	Description
12	GIG D-	TXRXD_N	GIG Ethernet D- pin
14	GIG D+	TXRXD_P	GIG Ethernet D+ pin
13	GIG C-	TXRXC_N	GIG Ethernet C- pin
15	GIG C+	TXRXC_P	GIG Ethernet C+ pin
16	Ethernet_Rx-/GIG B-	TXRXB_N	Low differential Ethernet receive
18	Ethernet_Rx+/GIG B+	TXRXB_P	High differential Ethernet receive
17	Ethernet_Tx-/GIG A-	TXRXA_N	Low differential Ethernet transmit
19	Ethernet_Tx+/GIG A+	TXRXA_P	High differential Ethernet transmit
38	LED_LINK/CFG_2	LED2/PHY_AD1	Ethernet Link LED/Configuration
39	LED_ACT/CFG_3	LED1/PHY_AD0	Ethernet Activity LED/Configuration

Table 6: RMII Ethernet 100 BaseT Interface

SODIMM Pin#	SoM Pin Name	Processor Pin Name	Description
99	COMA_DTR	ETX0	RMII Transmit Data 0
100	COMA_DSR	ETX1	RMII Transmit Data 1
101	COMA_RI	ERX0	RMII Receive Data 0
104	COMB_CTS	ERX1	RMII Receive Data 1
105	COMB_RTS	ETXEN	RMII Transmit Control
37	Card_Detect	ECRSDV	RMII Receive Control
116	GPIO2	ERXER	RMII Receive Error
117	GPIO3	EREFCK	RMII Reference Clock
118	GPIO4	EMDC	RMII Management Data Clock
119	GPIO5	EMDIO	RMII Management Data IO

2.4.5 USB

The SoM 200-pin specification provides for 2 USB hosts and 1 USB device or OTG (On-The-GO) port. The SoM-A5D36 does provide a USB OTG-like port. EMAC has mapped this port to both Host A and Device A ports. This allows the port to be used as a Full time Host port by connection to Host A or for a full time Device port by connection to device Port A. The use of Port A also allows for USB OTG in conjunction with VBUS and ID signals. There is a GPIO line that can be utilized to

enable USB power if necessary. This is SoM pin# 125, GPIO11 and is not required if power will always be on. Remember the USB Data lines are differential pairs and need to be routed as such.

Table 7: USB

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
5	Host_A+	HHSD2_P	N/A	Host USB 2.0 PortB +
7	Host_A-	HHSD2_N	N/A	Host USB 2.0 PortB -
6	Host_B+	HHSD3_P	N/A	Host USB 2.0 PortC +
8	Host_B-	HHSD3_N	N/A	Host USB 2.0 PortC -
9	Host/Device/OTC_C-	H/D_HSD1_N	N/A	OTG USB 2.0 PortA -
11	Host/Device/OTG_C+	H/D_HSD1_P	N/A	OTG USB 2.0 PortA +
10	USB_OTG_VBUS	PC27/SPI1_NPCS2/TWCK1	N/A	OTG VBUS
40	USB_OTG_ID	PC26/SPI1_NPCS1/TWD1	N/A	OTG ID

2.4.6 SPI

The ATSAMA5D36 processor provides two SPI (Serial Peripheral Interface) channels, SPI0 and SPI1, for communicating with peripheral devices. The SPI0 bus is connected internally to the serial flash, which uses SPI0_NPCS0 (SPI0_NPCS0 is not brought out to the card fingers. Care should be taken not to disrupt the SPI0 port as this is used in the boot process). Table 8 below lists the lines for SPI channel 0. Table 9 below lists the lines for the SPI channel 1. These pins have shared functions and can be accessed through the GPIO header on the SoM-200 carrier board. Note SPI Chip Selects (CS) for Linux do not require a specific SPI_CS and as such can use any GPIO allowing additional chip selects if a custom carrier is used.

Table 8: SPI Channel 0

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
22	SPI_MI	SPI0_MISO	PD10	SPI0 serial data in
23	SPI_MO	SPI0_MOSI	PD11	SPI0 serial data out
24	SPI_SCK	SPI0_SPCK	PD12	SPI0 serial clock out
25	SPI_CS0	SPI0_NCS1/CANRX0	PD14	SPI0 slave select line 0
26	SPI_CS1	SPI0_NCS2/CANTX0	PD15	SPI0 slave select line 1
27	SPI_CS2	SPI0_NCS3	PD16	SPI0 slave select line 2
28	SPI_CS3	SPI0_NCS4/PWMFI2	PC28	SPI0 slave select line 3

Table 9: SPI Channel 1

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
126	GPIO12	SPI1_MISO	PC22	SPI1 serial data in
127	GPIO13	SPI1_MOSI	PC23	SPI1 serial data out
128	GPIO14	SPI1_SPCK	PC24	SPI1 serial clock out
134	GPIO15	SPI1_NCS0	PC25	SPI1 slave select line 0
40	USB_OTG_ID	SPI1_NCS1	PC26	SPI1 slave select line 1
10	USB_OTG_VBUS	SPI1_NCS2	PC27	SPI1 slave select line 2

2.4.7 MMC/SDIO Ports

The SoM-A5D36 provides two 4-bit MMC/SD card interfaces, MCI1 and MCI2. The SoM-200 specification provides for three associated but optional SD/MMC control lines. Since these lines are optional and will not always be used, they are not part of the SD/MMC group but are part of the GPIO group. SoM pin#s 122, 123, and 124 can be used as SD_LED, SD_Power, and SD_protect, respectively.

MCI1 is allocated to the SoM Pin Specification in the SD/MMC section as the default SD port. When designing a custom carrier, MCI1 should be used rather than MCI2 if you want to maintain compatibility with present and future SoMs. The SoM-200GS/250GS Carrier boards' memory sockets make use of MCI1. The MCI2 interface should only be used if you are not concerned about compatibility with existing and future SoMs. MCI2 is accessed through the SoM-A5D36's GPIO section.

Table 10: MMC/SDIO Card Interface

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
31	SDCLK	MCI1_CLK	PB24	MCI Clock
32	CMD	MCI1_CDA	PB19	MCIB Command
33	DAT0	MCI1_DA0	PB20	MCIB D0
34	DAT1	MCI1_DA1	PB21	MCIB D1
35	DAT2	MCI1_DA2	PB22	MCIB D2
36	DAT3	MCI1_DA3	PB23	MCIB D3
37	Card_Detect	PC5/TCLK4	PC5	Card Detect

An additional MMC/SD interface is available through shared GPIO lines. All the lines for the second MMC/SD port are brought out to a header on the SoM-200 carrier.

Table 11: Additional MMC/SD Card Interface

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
125	GPIO11	MCI2_CK/PCK2	PC15	MCI Clock
120	GPIO6	MCI2_CDA	PC10	MCIC Command
121	GPIO7	MCI2_DA0	PC11	MCIC D0
122	GPIO8	MCI2_DA1/TIOA1	PC12	MCIC D1
123	GPIO9	MCI2_DA2/TIOB1	PC13	MCIC D2
124	GPIO10	MCI2_DA3/TCLK1	PC14	MCIC D3

2.4.8 Serial Ports

The SoM-200 pin specification has the provision for 4 serial ports. However, the ATSAMA5D36 provides 6 serial ports. The additional serial ports are accommodated through the use of alternate SoM pins. COMB (Debug port) is normally the console port. The ATSAMA5D36 processor does not provide full modem handshaking for COMA as called for in the SoM-200 pin specification, therefore EMAC has utilized processor GPIO lines for this function. The RTS lines for each port can be used to achieve automatic RS485 direction control.

Table 12: Serial Ports

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	SoM Description
95	COMA_TXD	TXD1	PB29	COMA transmit/GPIO
96	COMA_RXD	RXD1	PB28	COMA receive/GPIO
97	COMA_CTS	CTS1	PB26	COMA CTS/GPIO
98	COMA_RTS	RTS1	PB27	COMA RTS/GPIO
99	COMA_DTR	PC0/TIOA3	PC0	COMA DTR/GPIO
100	COMA_DSR	PC1/TIOB3	PC1	COMA DSR /GPIO
101	COMA_RI	PC2/TCLK3	PC2	COMA RING/GPIO
102	COMB_TXD	DTXD	PB31	COMB transmit/GPIO
103	COMB_RXD	DRXD	PB30	COMB receive/GPIO
104	COMB_CTS	PC3/TIOA4	PC3	COMB CTS/GPIO
105	COMB_RTS	PC4/TIOB4	PC4	COMB RTS/GPIO
106	COMC_TXD	TXD2	PE26	COMC transmit/GPIO
107	COMC_RXD	RXD2	PE25	COMC receive/GPIO
108	COMC_CTS	CTS2	PE23	COMC CTS/GPIO
109	COMC_RTS	RTS2	PE24	COMC RTS/GPIO
110	COMD_TXD	TXD0	PD18	COMD transmit/GPIO
111	COMD_RXD	RXD0	PD17	COMD receive/GPIO
112	COMD_CTS	CTS0/URXD0	PC29	COMD CTS/GPIO
113	COMD_RTS	RTS0/UTXD0	PC30	COMD RTS/GPIO

The additional 2 serial ports are available through the alternative multiplexed SoM pins.

Table 13: Additional Serial Ports

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Pin Description
29	I2C_CLK	UTXD1	PA31	UART 1 Transmit Data
30	I2C_DAT	URXD1	PA30	UART 1 Receive Data
113	COMD_RTS	UTXD0	PC30	UART 0 Transmit Data
112	COMD_CTS	URXD0	PC29	UART 0 Receive Data

2.4.9 I2S

The ATSAMA5D36 provides an I2S audio port which is accommodated within the SoM specification. Note that there is no CODEC on the SoM and therefore must be provided on the Carrier. In addition, the CODEC will require either SPI or I2C for control.

Table 14: I2S

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
86	AudioA_SCLK	TK0	PC16	I2S Serial Clock
87	AudioA_LRCLK/Frame	TF0	PC17	I2S Left / Right Clock
88	AudioA_MCLK	*	*	I2S Master Clock
89	AudioA_DIN	RD0	PC21	I2S Data Input
90	AudioA_DOUT	TD0	PC18	I2S Data Output

*The Master clock is driven On-Module by a 12.288 MHz oscillator to produce the 12.288 MHz Master clock. This oscillator is off by default and must be turned on via setting GPIO port line PC19 High. To reduce power the oscillator should be turned off when not required.

2.4.10 CAN

The SoM-200 specification provides for one CAN port. The SoM-A5D36 has two CAN ports. One is available through the SoM pin specification and the other is available through shared pins.

Table 15: CAN

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
93	CANTX	CANTX1	PB15	CAN Transmit
94	CANRX	CANRX1	PB14	CAN Receive

The second CAN port is available through the SPI chip select lines. With a custom carrier the use of the second CAN port can be utilized.

Table 16: CAN 2

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Pin Description
26	SPI_CS1	CANTX0	PD15	CAN Transmit
25	SPI_CS0	CANRX0	PD14	CAN Receive

2.4.11 GPIO

This section provides for the SoM general purpose IO section. All of these pins can be configured to be general-purpose digital ports. They can also be configured to take advantage of several of the functions of the SoM-A5D36's internal silicon as referenced in this User Manual. The second SPI and the pins for general-purpose timer/counters are brought out here and are somewhat standardized at these pin locations.

Table 17: General Purpose IO

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
114	GPIO0	PD5	Port D5
115	GPIO1	PD7	Port D7
116	GPIO2	PC6	Port C6
117	GPIO3	PC7	Port C7
118	GPIO4	PC8	Port C8
119	GPIO5	PC9	Port C9
120	GPIO6	PC10	Port C10
121	GPIO7	PC11	Port C11
122	GPIO8	PC12	Port C12
123	GPIO9	PC13	Port C13
124	GPIO10	PC14	Port C14
125	GPIO11	PC15	Port C15
126	GPIO12	PC22	Port C22
127	GPIO13	PC23	Port C23
128	GPIO14	PC24	Port C24
134	GPIO15	PC25	Port C25

2.4.12 Interrupts

The SoM specification defines 3 interrupt lines however, any GPIO on the ATSAMA5D36 processor may be programmed for interrupts.

Table 18: Interrupt Lines

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
129	IRQA	FIQ/PC31	Fast Interrupt Request
130	IRQB	IRQ/PE31	General Interrupt Request
131	IRQC	PE29	General Interrupt Request

2.4.13 ADC

The SoM-200 Pin Specification allocates SoM pins that can be utilized as Touchscreen or ADC inputs. Also, if a touchscreen is not used, the lines that would normally be used in this capacity can also be used as ADC inputs. The ATSAMA5D36 features a 12-channel, 12-bit ADC that can be used in single or dual ended configuration. Ten of these channels are available through the edge connector. The first four lines are used for a typical resistive 4-wire touchscreen. The ATSAMA5D36 does support 5 wire touchscreens. In addition to the 8 ADC pins allocated by the SoM specification there are an additional 2 ADC channels available through alternative pin functions. The analog reference is enabled by default, but it can be turned off if you are not using the touchscreen or ADC inputs by changing PB25 to an output and driving it low. The SoM-A5D36 provides a filtered onboard 3.3 Volt reference for the ADC.

Table 19: Analog to Digital Converters

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
45	X+/Xr/ADC0	AD0	PD20	X+ or ADC0
46	X-/Xl/ADC1	AD1	PD21	X- or ADC1
47	Y+/Yu/ADC2	AD2	PD22	Y+ or ADC2
48	Y-/Yd/ADC3	AD3	PD23	Y- or ADC3
49	SX+/ADC4	AD4	PD24	SX+ or ADC4
50	SX-/ADC5	AD5	PD25	SX- or ADC5
51	SY+/ADC6	AD6	PD26	SY+ or ADC6
52	SY-/ADC7	AD7	PD27	SY- or ADC7

Table 20: Additional ADC Channels

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
132	OSC0	AD10/PD30	ADC Channel 10
133	OSC1	AD11/PD31	ADC Channel 11

2.4.14 Timers/Counters

The general-purpose Timer/Counter (TC) module on the ATSAMA5D36 is comprised of six 32-bit timer/counter channels with independently programmable input capture or output compare lines. These can be used for a wide variety of timed applications, including counters and PWM. There are 5 separate Timer/Counters available on the card edge. Some of them are pinned out to the GPIO section of the SoM and the rest are available as alternate pin functions.

Table 21: Timers/Counters

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
99	COMA_DTR	TIOA3/PC0	Timer 3 IO A
100	COMA_DSR	TIOB3/PC1	Timer 3 IO B
101	COMA_RI	TCLK3/PC2	Timer 3 Clock
104	COMB_CTS	TIOA4/PC3	Timer 4 IO A
105	COMB_RTS	TIOB4/PC4	Timer 4 IO B
37	Card_Detect	TCLK4/PC5	Timer 4 Clock
114	GPIO0	TIOA0/PD5	Timer 0 IO A
115	GPIO1	TCLK0/PD7	Timer 0 Clock
116	GPIO2	TIOA5/PC6	Timer 5 IO A
117	GPIO3	TIOB5/PC7	Timer 5 IO B
118	GPIO4	TCLK5/PC8	Timer 5 Clock
122	GPIO8	TIOA1/PC12	Timer 1 IO A
123	GPIO9	TIOB1/PC13	Timer 1 IO B
124	GPIO10	TCLK1/PC14	Timer 1 Clock

2.4.15 SoM Status LED

One general purpose IO is connected to a green status LED on the SoM. The LED may be turned on by writing port line PE22 high.

2.4.16 LCD

The SoM-200 specification has provision for up to 24-bit LCDs (8-bits per RGB color). These lines can also be used to provide analog VGA connectivity for use with a conventional monitor by adding a video DAC to the Carrier. A Brightness PWM is also provided to allow for software control of the LCD's Brightness.

Table 22: LCD

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
57	LCD_BLUE0	LCDDAT0	PA0	LCD BLUE0
58	LCD_BLUE1	LCDDAT1	PA1	LCD BLUE1
59	LCD_BLUE2	LCDDAT2	PA2	LCD BLUE2
60	LCD_BLUE3	LCDDAT3	PA3	LCD BLUE3
61	LCD_BLUE4	LCDDAT4	PA4	LCD BLUE4
62	LCD_BLUE5	LCDDAT5	PA5	LCD BLUE5
63	LCD_BLUE6	LCDDAT6	PA6	LCD BLUE6
64	LCD_BLUE7	LCDDAT7	PA7	LCD BLUE7
65	LCD_GREEN0	LCDDAT8	PA8	LCD GREEN0
66	LCD_GREEN1	LCDDAT9	PA9	LCD GREEN1
67	LCD_GREEN2	LCDDAT10	PA10	LCD GREEN2
68	LCD_GREEN3	LCDDAT11	PA11	LCD GREEN3
69	LCD_GREEN4	LCDDAT12	PA12	LCD GREEN4
70	LCD_GREEN5	LCDDAT13	PA13	LCD GREEN5
71	LCD_GREEN6	LCDDAT14	PA14	LCD GREEN6
72	LCD_GREEN7	LCDDAT15	PA15	LCD GREEN7
73	LCD_RED0	LCDDAT16	PA16	LCD RED0
74	LCD_RED1	LCDDAT17	PA17	LCD RED1
75	LCD_RED2	LCDDAT18	PA18	LCD RED2
76	LCD_RED3	LCDDAT19	PA19	LCD RED3
77	LCD_RED4	LCDDAT20	PA20	LCD RED4
78	LCD_RED5	LCDDAT21	PA21	LCD RED5
79	LCD_RED6	LCDDAT22	PA22	LCD RED6
80	LCD_RED7	LCDDAT23	PA23	LCD RED7
81	LCD_HORZ/LP	LCDHSYNC	PA27	Horizontal Sync
82	LCD_VERT/FP/FLM	LCDVSYNC	PA26	Vertical Sync
83	LCD_ENABLE/DE/M	LCDDEN	PA29	Enable
84	LCD_CLK/SFK/SHFCLK	LCDPCK	PA28	LCD Clock
85	BCKLIGHT	LCDPWM	PA24	Backlight Brightness Control

2.4.17 Additional Interfaces

The SoM-A5D36 has additional optional interfaces available by trading some of the features outlined in the SoM specification.

Image Sensor Interface (ISI):

The ATSAMA5D36 Processor has a 12-bit Image Sensor Interface available for use if the LCD is not used. The table below shows the SoM pin connections for a custom carrier that uses the ISI.

The Image Sensor Interface connects a CMOS-type image sensor to the processor and provides image capture in various formats. It does data conversion, if necessary, before storing in memory through DMA. The interface can accommodate both 8 and 12-bit sensors.

Table 23: Image Sensor Interface

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
73	LCD_RED0	ISI_D0/LCDDAT16	ISI Data 0
74	LCD_RED1	ISI_D1/LCDDAT17	ISI Data 1
75	LCD_RED2	ISI_D2/LCDDAT18	ISI Data 2
76	LCD_RED3	ISI_D3/LCDDAT19	ISI Data 3
77	LCD_RED4	ISI_D4/LCDDAT20	ISI Data 4
78	LCD_RED5	ISI_D5/LCDDAT21	ISI Data 5
79	LCD_RED6	ISI_D6/LCDDAT22	ISI Data 6
80	LCD_RED7	ISI_D7/LCDDAT23	ISI Data 7
112	COMD_CTS	ISI_D8/PC29	ISI Data 8
28	SPI_CS3	ISI_D9/PC28	ISI Data 9
10	USB_OTG_VBUS	ISI_D10/PC27	ISI Data 10
40	USB_OTG_ID	ISI_D11/PC26	ISI Data 11
113	COMD_RTS	ISI_PCK/PC30	ISI Pixel Clock
30	I2C_DATA	ISI_VSYNC/PA30	ISI Vertical Sync
29	I2C_CLK	ISI_HSYNC/PA31	ISI Horizontal Sync

2.5 Power Connections

The SoM-A5D36 requires a 3.3V supply for the Bus and I/O voltages. The 1.2V core voltage is regulated on module from the 3.3V. Unlike some other modules no other supply voltage other than 3.3V is required.

Table 24: Power Connections

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
3,4,43,44,135, 136,197,198	3.3VCC	3.3VCC	3.3 Volt SoM Supply Voltage
1,2,20,21,41,42, 91,92,137,138, 155,156,199,200	GND	GND	Digital Ground
53	Analog_GND	ADC_GND	Analog Ground
56	VSTBY	Vstandby_3.3	Voltage standby, this is the backup voltage provided to the SoM's RTC. If RTC readings are not important for the application, this can be attached to the 3.3V rail.
55	AV_REF	NC	Analog power/reference. This voltage provides power to the internal analog circuitry of the processor. It can be typically connected to 3.3V. LC filtering for this power signal is provided on-module.

2.6 Boot Options

The SoM specification provides two pins for boot-time configuration. On the SoM-A5D36, these are BMS and Flash Disable. The Boot Mode Select (BMS) pin allows the SoM-A5D36 to be low-level booted from either its internal ROM (3.3V) or external (carrier resident) NOR flash (GND). The Flash Disable pin should be tied to GND to enable the Serial Flash or 3.3V to disable.

For normal system Boot, the SoM-A5D36 should be configured as follows:

BOOT_OPTION0 – 3.3V

BOOT_OPTION1 – GND

The Module can high-level boot from either the Serial Flash or the eMMC Flash (selected through the low- level bootloader). It is recommended to high-level boot from the Serial Flash, as this Flash is more reliable than the eMMC Flash. The eMMC flash is ideal for the Operating System's File System which can normally mark bad blocks.

Table 25: Boot Options

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
157	BOOT_OPTION0	BMS	Serial Boot Mode Select
158	BOOT_OPTION1	-	Disable Serial Flash

2.7 Serial Data Flash

The Serial Flash is connected to SPI0 and uses SPI0_NPCS0 to enable it. The Serial Flash also has a Write- Protect Provision. To Write-Protect the Serial Flash, pull SoM pin# 154 low. SoM pin# 154 is pulled up by a 10K ohm resistor on the module.

If this feature is required it would be implemented on the carrier as a jumper or an I/O line.

3 Design Considerations

One of the goals of the SoM-A5D36 is to provide a modular, flexible and inexpensive solution capable of delivering high-end microcontroller performance with low power requirements.

3.1 Off-the-Shelf Carriers

Many SoM-A5D36 applications can make use of EMAC's off-the-shelf carriers. These carriers provide power to the SoM as well as a wealth of connectors and interfaces to access peripheral I/O including audio and LCD.

3.1.1 SoM-200GS

This is a Half-EBX mounting hole form factor (4.37" x 6.00") carrier that comes with a 4.3" LCD interface as well as full schematics and a BOM, and can be used as is, or as a reference for a customer's own design.

- 10/100/1000 BaseT Ethernet with Status LEDs
- 3 serial RS232 ports and 1 RS232/422/485 port
- Resistive Touchscreen interface
- 480 x 272 Graphic LCD with Touchscreen
- Battery for nonvolatile RAM and Real Time Clock
- Micro SD Card Socket
- 2 USB Host & 1 USB OTG ports
- 1 I2S Audio port with Line-In/Line-Out
- 5 VDC Power Requirement

http://emacinc.com/products/system_on_module/SoM-200GS

3.1.2 SoM-250GS

This is a 6.55" x 4.15" carrier designed as a basis for a 7” or 10” Panel PC.

- 10/100/1000 BaseT Ethernet with onboard Magnetics and RJ45
- 3 serial RS232 ports and 1 RS232/422/485 port
- Resistive Touchscreen interface
- 800 x 480 (WVGA) or 1024 x 600 (WSVGA) Graphic LCD with Touchscreen
- Battery for nonvolatile RAM and Real Time Clock
- Micro SDHC/MMC Flash Card Socket
- 2 USB Host & 1 USB OTG ports
- 1 I2S Audio port with Line-In/Line-Out
- 1 Audio Beeper
- Timer/Counters and Pulse Width Modulation (PWM) ports
- Operating Voltage of 12 to 28 Vdc.
- Graphic LCD Interface

http://emacinc.com/products/system_on_module/SoM-250GS

3.2 Semi-Custom Carriers

EMAC also offers a semi-custom engineering service. By modifying one of our existing designs, EMAC can offer quick-turn, low-cost engineering, for your specific application.

3.3 Designing Your Own Carrier

It is best to start with the SoM-200GS as a reference. When designing a carrier be sure to use a 200 pin DDR1 SODIMM socket instead of the more common DDR2 socket. The DDR2 socket is keyed in such a way as to prevent the SoM from being inserted into it. The part number for a compatible DDR1 socket made by Tyco is 1473005-1. This socket will provide 3.0 mm of height from the top of carrier PCB to the bottom of the module PCB. The module specification allows for a 1.5 mm maximum height for bottom components. Therefore, this allows the user < 1.5 mm for placing components safely under the module. If more height is needed, Tyco as well as other manufacturers make SODIMM sockets with additional height, although these are more expensive.

If using the SoM-A5D36’s external bus, it is highly recommended to buffer the bus on the carrier board in close proximity to the SoM SODIMM connector (see the SoM-200 carrier schematics for reference).

3.3.1 Power

The SoM-A5D36 requires a voltage of 3.3V at 300mA for a normal operation, users can get away with using only 3.3V, and simply provide this to all the voltage inputs listed in 3.6. This however, will not provide battery backup for the RTC. Additionally, 5V is required if USB Host capability is required.

3.3.2 Analog Reference

The reference for the analog to digital converter is provided on the SoM with no need to provide and external reference. The onboard ADC reference is 3.3 Volts and can be switched on and off. The touch screen uses the ADC pins on the processor so the ADC reference must be enabled for the touch screen controller to function properly.

3.3.3 Battery Backup

The SoM-A5D36 contains 3 potentially non-volatile memory areas, the eMMC flash, the real-time clock, and the serial flash of the processor. The flash is always non-volatile, the real-time clock requires a backup voltage to maintain its data. This backup voltage comes from the VSTBY SoM pin, and should be connected to 3.3 volts.

The RTC will draw approximately 8 µA when the processor is not powered by the 3.3V supply. Be aware that the Static current can rise if the temperature increases to 85° C. When the module is powered no current is drawn from the backup battery supply. If RTC backup is not needed, this can be tied to 3.3V.

The SoM-200GS, as well as other carriers, provide battery backup voltage through a replaceable BR2032, which is a standard 3V 190mA/H 20MM coin battery that can be picked up from most electronics stores.

3.3.4 Shutdown Logic Pins

The SHDN is a digital output only (0 to 3.3V, pulled up on-module), which is driven by the Shutdown Controller on the processor. The WKUP pin has a Maximum input voltage of 3.3V, but cannot exceed VDDBU. Both of these pins are connected directly to the processor.

4 Software

The SoM-A5D36 offers a wide variety of software support from both open source and proprietary sources. The hardware core utilizes the Atmel ARM Cortex-A5 ATSAMA5D36, which is supported by Linux.

For more information on Linux Software Support, please visit the EMAC Wiki Software Section

at: http://wiki.emacinc.com/wiki/Product_wiki

4.1 Das U-Boot

EMAC utilizes Das U-Boot for its ARM based products. U-Boot is an open source/cross-architecture platform independent bootloader. It supports reading and writing to the flash, auto-booting, environmental variables, and TFTP. Das U-boot can be used to upload and run and/or reflash the OS or to run stand-alone programs without an OS. Products are shipped with a valid MAC address installed in flash in the protected U-boot environmental variable “ethaddr”. At boot time U-Boot automatically stores this address in a register within the MAC, which effectively provides it to any OS loaded after that point.

4.2 Embedded Linux

EMAC Open Embedded Linux (EMAC OE Linux) is an open source Linux distribution for use in embedded systems. The EMAC OE Linux Build is based on the Open Embedded (www.openembedded.org) and Yocto (www.yoctoproject.org) Linux build systems. Open Embedded is a superior Linux distribution for embedded systems. Custom Linux builds are also available on request.

The distribution contains everything a user could expect from a standard Linux kernel: powerful networking features, advanced file system support, security, debugging utilities, and countless other features.

The basic root file system includes:

- Busybox
- Hotplugging support
- APM utilities for power management
- Openssh SSH server
- lighttpd HTTP server
- EXT4 file system with utilities

4.2.1 Linux with PREEMPT RT

PREEMPT RT provides pseudo real time to the kernel and can be used to schedule tasks with hard deadlines and minimal latencies. The PREEMPT RT build is an option to the standard Linux build and is available for a one-time inexpensive support/installation fee.

4.2.2 Linux Packages

EMAC provides support for many Linux Packages such as: PHP, SQLite, Perl, SNMP, DHCP Server, etc. As with the PREEMPT RT Option, other Packages can be added to the standard Linux file system and are available for a one-time inexpensive support/installation fee.

4.2.3 Linux Patches

In addition to standard Embedded Linux support, EMAC has released a number of patches and device drivers from the open source community and from internal EMAC engineering into its standard distribution. Along with kernel patches, EMAC provides the binaries for the kernel and root file system.

4.3 Qt Creator

Qt Creator is a cross-platform IDE (Integrated Development Environment) tailored to the needs of Qt developers but works well for Headless applications as well. EMAC provides sample code as projects that can be imported into Qt Creator. Qt Creator supports remote deployment and source debugging.

http://wiki.qt.io/Main

4.4 ARM EABI Cross Compiler

The popular open source gcc compiler has a stable build for the ARM family. EMAC uses the 4.9.1 version of the ARM EABI compiler. The Embedded Linux kernel and EMAC Qt Creator projects use this compiler for building ARM stand alone, and OS specific binaries. The EMAC Qt Creator provides source level debugging over Ethernet or serial using gdbserver. The Linux binaries for the ARM EABI cross compiler are available online along with the SDK. See the EMAC wiki for further information.