# SoM-A5D35

## User Manual

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EMAC, inc.
EQUIPMENT MONITOR AND CONTROL
2390 EMAC Way, Carbondale, Illinois 62902
Phone: (618) 529-4525 Fax: (618) 457-0110
http://www.emacinc.com

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# 1 Introduction

This document describes EMAC's SoM-A5D35 System on Module. The SoM-A5D35 is designed to be compatible with EMAC's 144-pin SODIMM form factor. This module is built around the ATMEL AT91SAMA5D35 microcontroller, which provides several of its key features.

The SoM-A5D35 has an onboard Ethernet PHY, 6 serial ports, 3 USB 2.0 ports, an I2S audio port, an MMC port, a RTC, a programmable clock synthesizer, onboard eMMC flash, Serial NOR Flash, and LPDDR2.

In addition to these standard SoM features, the SoM-A5D35 also features a fast 32-bit core, open-source software support, and a wide range of controller IO pins.

## 1.1 Features

- **Small, 144 pin SODIMM form factor (2.66" x 1.5")**
- **Atmel ARM Cortex-A5 ATSAMA5D35 536MHz Processor**
- **10/100 BaseT Ethernet with on-board PHY**
- **16-bit External Bus Interface**
- **6x Serial ports, one with full handshake and one with CTS/RTS handshake**
- **2x USB 2.0 (High Speed) Host ports**
- **1x USB 2.0 (High Speed) Device/Host port**
- **512 MB of LPDDR2**
- **4 GB of Resident eMMC Flash**
- **16 MB of Serial NOR Flash**
- **Battery-backed Real-Time Clock**
- **SD/MMC Flash Card Interface**
- **2x SPI ports**
- **2x I2C Ports**
- **1x I2S Audio Port**
- **2x CAN Bus Interfaces**
- **Timer/Counters and Pulse Width Modulation (PWM) ports**
- **4-Channel 12-bit Analog-to-Digital converter**
- **Typical power requirement less than 1 Watt**
- **JTAG for debug, including real-time trace**
- **FREE QT Creator IDE with GCC and GDB development tools**

# 2 Hardware

## 2.1 Specifications

- **CPU:** Embedded Atmel ATSAMA5D35 processor running at 536 MHz
- **Flash:** 4GB eMMC Flash and 16MB of Serial NOR Flash
- **RAM:** 512MB 133MHz LPDDR2
- **Flash Disk:** 4-bit Parallel or SPI serial SDHC/MMC interface
- **System Reset:** Supervisor with external Reset Button provision
- **RTC:** Real-Time Clock/Calendar with battery-backed provision using 32-bit free running counter
- **Timer/Counters:** 2x 3-channel, 32-bit timers/counters with capture, compare, and PWM
- **Watchdog Timer:** External Watchdog Timer (MAX6747)
- **Digital I/O:** 32x General Purpose I/Os with 16 mA drive when used as an output
- **Analog I/O:** 4-channel, 12-bit Analog-to-Digital converter (ADC)
- **Power:** Power Management Controller allows selectively shutting down on-processor I/O functionality and running from a slow clock
- **JTAG:** JTAG for debug, including real-time trace
- **Clocks:** PLL synthesized 8MHz, 200KHz, 14.3MHz clock outputs

**Serial Interfaces**

- **UARTS:** 6x serial TTL level serial ports with Auto RS485 and some with handshaking (each UART requires external RS level shifting)
- **SPI:** 2x High-Speed SPI ports with Chip Selects
- **Audio:** I2S Synchronous Serial Controller with analog interface support
- **USB:** Dual USB 2.0 High Speed Host ports and single USB 2.0 High Speed Device port (OTG)

**Ethernet Interface**

- **MAC:** ATSAMA5D35 on chip MAC
- **PHY:** Microchip KSZ8081 low power PHY with software shutdown and slow clock modes
- **Interface:** IEEE 802.3u 10/100 BaseT Fast Ethernet (requires external magnetics and Jack)

**Bus Interface:**

- Local ARM ATSAMA5D35 Bus accessible through card fingers provides 22 address lines, 16 data bus lines, and control lines

**Mechanical and Environmental**

- **Dimensions:** SODIMM form factor with the length dimension extended (2.66" x 1.5")
- **Power Supply Voltage:** +3.3 Volts DC +/- 5%
- **Power Requirements (typical):**
  - Typical 3.3 Volts @ 175 mA (less than 1 watt)
  - Max current draw during boot process: 210 mA
  - Constant busy loop: 180 mA
  - Idle system: 160 mA
  - Idle system with Ethernet PHY disabled: 65 mA
  - APM sleep mode with Ethernet PHY disabled: 9.5 mA
  - APM sleep mode with Ethernet PHY and USB disabled: 4.0 mA
  - APM sleep mode with Ethernet PHY enabled: 60 mA
- **Operating Temperature:** -40 ~ 85° C (-40 ~ 185 ° F), fanless operation
- **Operating Humidity:** 0% ~ 90% relative humidity, non-condensing

## 2.2 Real-Time Clock

The SoM-A5D35 has an embedded Real-time Clock. Battery backup is provided from the carrier board using the VSTBY pin. The SoM-A5D35 will retain the RTT value register during reset and hence use it as an RTC. The RTC has the provision to set alarms that can interrupt the processor. For example, the processor can be placed in sleep mode and then later awakened using the alarm function.

## 2.3 Watchdog Timer

The SoM-A5D35 provides an external Watchdog Timer/ Supervisor (MAX6747) with an extended watchdog timeout period of 1.42 seconds (±10%). Upon power-up the Watchdog is disabled and does not require pulsing. To start the Watchdog, it must first be enabled. This is done by configuring port line PA24 as an output and setting it low in software. Once enabled, the Watchdog should be pulsed, using port line PA23, continually every 1.28 seconds or faster to prevent the Watchdog from timing out and resetting the module. If the user is using the watchdog to force a system reset, the watchdog may need up to 1.56 seconds of inactivity before the watchdog reset will occur. The watchdog is automatically disabled upon reset but it can also be disabled by setting PA24 high.

## 2.4 External Connections

The SoM-A5D35 connects to a carrier board containing its connectors, power supply and any expansion IO, through a standard ENIG-plated (Electroless Nickel Immersion Gold) SODIMM 144 pin connection (top half shown below).

The SoM model will fit in any standard 144-pin SODIMM socket. These connections are designed to be compatible with all EMAC 144-pin SoM products. See EMAC SoM 144-pin SODIMM Pinout Specification to see how other 144-pin SoMs pin-outs line up with the SoM-A5D35's pin-out.

The use of the SODIMM form-factor for EMAC's SoMs is a sound choice that has been proven rugged and reliable in the laptop market.

The remainder of this section describes the pin-out as it applies specifically to the SoM-A5D35 processor.

### 2.4.1 External Bus

The SoM-A5D35 provides a flexible external bus for connecting peripherals. The WKUP pin has a Maximum input voltage of 3.3V (pulled up on-module to 3.3V) and Shutdown has a maximum output voltage of 3.3V. The Flash WP for the Serial Flash is active-low and pulled up on-module.

**Table 1: External Bus**

| SODIMM Pin# | SoM Pin Name | Processor Pin Name(s) | Description |
|---|---|---|---|
| **100** | GP_CS1 | NCS1/PE27 | General Purpose Processor Chip Select CS2 |
| **98** | GP_CS2 | NCS2/PE28 | General Purpose Processor Chip Select CS4 |
| **108** | GP_CS3 | NCS3 | General Purpose Processor Chip Select CS5 |
| **16** | ~OE | NRD | Read Signal |
| **83** | ~WR | NWE | Write Signal |
| **6** | ~RST_IN | SOM_RST_OUT | Processor Reset |
| **43** | ~RST_OUT | NRST | Processor Reset |
| **44** | ~EA | SHDN | Shutdown Control |
| **85** | Flash WP | Serial Flash WP | Serial Flash Write Protect |
| **72** | ALE/~TS | WKUP | Wake-Up Input |
| **26,35,33,31,28, 109,111,113,10,12, 18,14,37,5,11,9,7, 13,97,17,15,104** | A0-A21 | A0-A21 | Address Bus |
| **29,27,25,22,23,21, 19,20,8,24,34,70, 77,81,84,86** | D0-D15 | D0-D15 | Data Bus |

### 2.4.2 JTAG

The SoM specification allows for access to the JTAG lines for the ATSAMA5D35 processor. These connections will allow the Flash to be programmed in-circuit via a program running from the processor and also the capability to debug software.

**Table 2: Processor JTAG**

| SODIMM Pin# | SoM Pin Name | Processor Pin Name(s) | Description |
|---|---|---|---|
| **139** | JTAG_TCK | TCK/SWCLK | JTAG clock |
| **137** | JTAG_TDI | TDI | JTAG serial in |
| **138** | JTAG_TDO | TDO | JTAG serial out |
| **140** | JTAG_TMS | TMS/SWDIO | JTAG operation mode |
| **112** | JTAG_TRST | NTRST | Test Reset Signal |

### 2.4.3 One-Wire / I2C

The SoM specification calls for a one-wire port. Since the SoM-A5D35 does not have a one-wire port, this line is not connected for One-Wire Operation. The ATSAMA5D35 processor does provide an I2C bus and so these pins are dedicated to that function although they can also be used as GPIOs.

**Table 3: One-Wire / I2C Port**

| SODIMM Pin# | SoM Pin Name | Processor Pin Name(s) | Description |
|---|---|---|---|
| **116** | LOCAL1W/SCL | TWCK0/PA31 | I2C Clock |
| **88** | SDA | TWD0/PA30 | I2C Data |

### 2.4.4 Ethernet

The SoM-A5D35 provides a Microchip KSZ8081 Low Power Ethernet RMII PHY IC on board. Carrier designers need only run these lines through the appropriate magnetics layer to have a functional Ethernet connection. Remember the RX and TX lines are differential pairs and need to be routed as such.

The LED/configuration pins' state at reset determines the Ethernet's configuration (10-baseT, 100-base-T, autoconfig) and the function of the LED's. The SoM-112ES and the SoM-150ES pull them all high, which configures the chip for network autoconfig, with LED0 functioning as active low link, and LED1 functioning as active low Rx Activity (Refer to Carrier schematics).

The Ethernet PHY can be put into a low power mode by writing directly to the MAC via software.

Additional power can be saved by turning off the PHY Oscillator. This is done by setting GPIO PC10 low. Make sure to send software commands to the PHY to put it into slow clock and power-down mode before shutting off the Oscillator. When restoring the PHY first turn the Oscillator on and disable slow clock mode before accessing the PHY.

**Table 4: Ethernet**

| SODIMM Pin# | SoM Pin Name | {PHY} Pin Name | Description |
|---|---|---|---|
| **89** | LED_LINK/ CFG_1 | LED_0 NWAYEN | Ethernet Link LED Configuration Pin |
| **90** | LED_RX/ CFG_2 | LED_1 SPEED | Ethernet Activity LED Configuration pin |
| **94** | Ethernet_Rx- | RXM | Low differential Ethernet receive line |
| **92** | Ethernet_Rx+ | RXP | High differential Ethernet receive line |
| **93** | Ethernet_Tx- | TXM | Low differential Ethernet transmit line |
| **91** | Ethernet_Tx+ | TXP | High differential Ethernet transmit line |

### 2.4.5 USB

The SoM-A5D35 provides 2 High speed USB 2.0 Host ports and 1 High Speed USB 2.0 Device/Host port. The USB Device/Host port can be used as an “On-The-Go”-like port on custom carriers. The Device/Host port is connected to a USB Type B connector on the SoM-112ES and SoM-150ES carrier boards.

**Table 5: USB**

| SODIMM Pin# | SoM Pin Name | Processor Pin Name(s) | Description |
|---|---|---|---|
| **64** | USB1_D+ | HHSDPB | Host, High Speed USB 1 |
| **66** | USB1_D- | HHSDMB | Host, High Speed USB 1 |
| **65** | USB2_D+ | HHSDPC | Host, High Speed USB 2 |
| **67** | USB2_D- | HHSDMC | Host, High Speed USB 2 |
| **60** | USB3/OTG_D- | H/DHSDMA | Device/Host, HS USB 3 |
| **61** | USB3/OTG_D+ | H/DHSDPA | Device/Host, HS USB 3 |
| **45** | USB_OTG_VBUS | AD10/PD30 | USB OTG VBUS Detect |

### 2.4.6 SPI

The ATSAMA5D35 processor provides a dual (SPI0 and SPI1) SPI module for communicating with peripheral devices. On the SoM the SPI0 bus is already connected to the serial flash, which uses SPI0_NPCS0 (SPI0_NPCS0 is not brought out to the card fingers). The first Table below lists the lines for the #0 SPI module. The SoM pin specification allows for three SPI chip selects. The SPI chip selects available to the card edge are SPI0_NPCS1, SPI0_NPCS2, and SPI0_NPCS3. The second Table below lists the lines for the #1 SPI module.

**Table 6: Serial Peripheral Interface (SPI)**

| SODIMM Pin# | SoM Pin Name | Processor Pin Name(s) | Description |
|---|---|---|---|
| **122** | SPI0_MI | SPI0_MISO/PD10 | SPI0 serial data in |
| **121** | SPI0_MO | SPI0_MOSI/PD11 | SPI0 serial data out |
| **120** | SPI0_SCK | SPI0_SPCK/PD12 | SPI0 serial clock out |
| **123** | SPI0_CS0 | SPI0_NPCS1/PD14 | SPI0 slave select line 0 |
| **124** | SPI0_CS1 | SPI0_NPCS2/PD15 | SPI0 slave select line 1 |
| **110** | SPI0_CS2 | SPI0_NPCS3/PD16 | SPI0 slave select line 2 |

**Table 7: Additional SPI**

| SODIMM Pin# | SoM Pin Name | Processor Pin Name(s) | Description |
|---|---|---|---|
| **133** | SPI1_MISO/GPIO | SPI1_MISO/PC22 | SPI1 serial data in / GPIO |
| **134** | SPI1_MOSI/GPIO | SPI1_MOSI/PC23 | SPI1 serial data out / GPIO |
| **135** | SPI1_SCK/GPIO | SPI1_SPCK/PC24 | SPI1 serial clock out / GPIO |
| **136** | SPI1_NPCS0/GPIO | SPI1_NPCS2/TWCK1/PC27 | SPI1 slave select line 0 / GPIO |
| **105** | SPI1_NPCS1/GPIO | SPI1_NPCS1/TWD1/PC26 | SPI1 slave select line 1/ GPIO |

### 2.4.7 MCI SDIO Multimedia Card

The ATSAMA5D35 processor provides a 4-bit SDIO MMC/SD card interface using the SDIO lines. The SoM-A5D35 utilizes this interface to provide SDIO. The SoM-112ES and SoM-150ES Carrier boards provide and SD Card Slot that is compatible with the SOM-A5D35.

**Table 8: MMC/SD Card Interface**

| SODIMM Pin# | SoM Pin Name | Processor Pin Name(s) | Description |
|---|---|---|---|
| **54** | MCI_CK | MCI0_CK/PB24 | MCI Clock |
| **51** | MCI_CDA | MCI0_CDA/PB19 | MCIA Command |
| **50** | MCI_DA0 | MCI0_DA0/PB20 | MCIA D0 |
| **55** | MCI_DA1 | MCI0_DA1/PB21 | MCIA D1 |
| **56** | MCI_DA2 | MCI0_DA2/PB22 | MCIA D2 |
| **57** | MCI_DA3 | MCI0_DA3/PB23 | MCIA D3 |
| **42** | MCI_CD | TIOB1/PC13 | MCIA Card Detect |

### 2.4.8 Serial Ports

The SoM-144 pin specification has the provision for 3 serial ports. However, the ATSAMA5D35 provides 6 serial ports so the 3 additional serial ports are accommodated through the use of alternate SoM pins. UART1 on the ATSAMA5D35 processor provides handshaking pins, however the RING, DSR, DCD, and DTR signals are not available on the processor and are generated by software using GPIOs.

**Table 9: Serial Ports**

| SODIMM Pin# | SoM Pin Name | Processor Pin Name(s) | Description |
|---|---|---|---|
| **71** | COMA_RXD | RXD0/PD17 | UART0 Receive/GPIO |
| **73** | COMA_TXD | TXD0/PD18 | UART0 Transmit/GPIO |
| **38** | COMB_RXD | RXD2/PE25 | UART2 Receive/GPIO |
| **36** | COMB_TXD | TXD2/PE26 | UART2 Transmit/GPIO |
| **82** | COMB_RTS/GPIO | RTS2/PE24 | UART2 RTS/GPIO |
| **78** | COMB_CTS/GPIO | CTS2/PE23 | UART2 CTS/GPIO |
| **103** | COMC_RXD | RXD1/PB28 | UART1 Receive/GPIO |
| **102** | COMC_TXD | TXD1/PB29 | UART1 Transmit/GPIO |
| **107** | COMC_DSR/GPIO | PWMH1/PA22 | UART1 DSR /GPIO |
| **106** | COMC_DTR/GPIO | PWMH2/PB8 | UART1 DTR/GPIO |
| **76** | COMC_RI/GPIO | PWMH3/PB12 | UART1 RING/GPIO |
| **30** | COMC_DCD/GPIO | PWMH0/PA20 | UART1 DCD/GPIO |
| **39** | COMC_RTS/GPIO | RTS1/PB27 | UART1 RTS/GPIO |
| **79** | COMC_CTS/GPIO | CTS1/PB26 | UART1 CTS/GPIO |

**Table 10: Additional Serial Ports**

| SODIMM Pin# | SoM Pin Name | Processor Pin Name(s) | Description |
|---|---|---|---|
| **46** | Debug RXD | DRXD/PB30 | Debug Receive / GPIO |
| **47** | Debug TXD | DTXD/PB31 | Debug Transmit / GPIO |
| **49** | COMD RXD | RXD3/PE18 | UART3 Receive / GPIO |
| **48** | COMD TXD | TXD3/PE19 | UART3 Transmit / GPIO |
| **88** | SDA | URXD1/PA30 | USART1 RXD / GPIO |
| **116** | LOCAL1W /SCL | UTXD1/PA31 | USART1 TXD / GPIO |

### 2.4.9 I2S

The SoM-A5D35 provides an I2S serial interface for connecting to an audio codec.

**Table 11: I2S**

| SODIMM Pin# | SoM Pin Name | Processor Pin Name(s) | Description |
|---|---|---|---|
| **87** | I2S_TXCK | TK1/PB2 | Transmit Clock / GPIO |
| **80** | I2S_LRCK | TF1/PB3 | Transmit Frame / GPIO |
| **125** | I2S_TXD | TD1/PB6 | Serial Transmit Data / GPIO |
| **126** | I2S_RXD | RD1/PB11 | Serial Receive Data / GPIO |
| **128** | I2S_RF | RF1/PB10 | Receive Frame / GPIO |
| **127** | I2S_RXCK | RK1/PB7 | Receive Clock / GPIO |

### 2.4.10 CAN

The ATSAMA5D35 has two CAN controllers that are brought out to the SoM card edge. One is defined by the SoM specification and the second can be utilized instead of the SPI chip selects. The SoM specified CAN port can be used as GPIO if desired.

**Table 12: CAN**

| SODIMM Pin# | SoM Pin Name | Processor Pin Name(s) | Description |
|---|---|---|---|
| **96** | CANTX | CANTX1/PB15 | CAN Transmit / GPIO |
| **95** | CANRX | CANRX1/PB14 | CAN Receive / GPIO |

**Table 13: Additional CAN Port**

| SODIMM Pin# | SoM Pin Name | Processor Pin Name(s) | Description |
|---|---|---|---|
| **123** | SPI0_CS0 | CANRX0/SPI0_NPCS1PD14 | CAN Receive / SPI Chip Select 1 |
| **124** | SPI0_CS1 | CANTX0/SPI0_NPCS2/PD15 | CAN Transmit / SPI Chip select 2 |

### 2.4.11 GPIO

This section provides for the SoM general purpose IO section. All of these pins can be configured to be general-purpose digital ports. They can also be configured to take advantage of several of the functions of the ATSAMA5D35's internal silicon. All of the internal A/D ports are brought out here, as well as all of the available IRQs, the second SPI and the pins for general-purpose timer/counters.

**Interrupts:**

The ATSAMA5D35 is capable of using any GPIO pin as an interrupt as well as the pins that are labeled IRQ. The 144-Pin SoM Specification defines 3 IRQs.

**Table 14: Interrupt Lines**

| SODIMM Pin# | SoM Pin Name | Processor Pin Name(s) | Description |
|---|---|---|---|
| **75** | IRQA/GPIO_1 | FIQ/PC31 | Interrupt A / GPIO 1 |
| **32** | IRQB/GPIO_2 | IRQ/PWML1/PE31 | Interrupt B / GPIO 2 |
| **40** | IRQC/GPIO_0 | TCLK1/PC16 | Interrupt C / GPIO 0 |

**A/D:**

The ATSAMA5D35 Analog to Digital pins provides 4 channels of 12-bit resolution with a 1 us conversion time. With the enhanced DSP extensions, this can make quite a capable signal processor. The Analog to Digital Reference Voltage is enabled by default, but can be controlled by PA25. PA25 configured as an input disables the reference, or it can be enabled by configuring it as an output and driving it low.

**Table 15: Analog to Digital Converters**

| SODIMM Pin# | SoM Pin Name | Processor Pin Name(s) | Description |
|---|---|---|---|
| **129** | AD1/GPIO_5 | AD0/PD20 | ADC CH1 / GPIO 5 |
| **130** | AD2/GPIO_6 | AD1/PD21 | ADC CH2 / GPIO 6 |
| **131** | AD3/GPIO_7 | AD2/PD22 | ADC CH3 / GPIO 7 |
| **132** | AD4/GPIO_8 | AD3/PD23 | ADC CH4 / GPIO 8 |

**Timer/Counters:**

The general-purpose Timer/Counter (TC) module on the ATSAMA5D35 is comprised of six 32-bit timer/counter channels with independently programmable input capture or output compare lines. These can be used for a wide variety of timed applications, including counters and PWM.

**Table 16: Timers/Counters**

| SODIMM Pin# | SoM Pin Name | Processor Pin Name(s) | Description |
|---|---|---|---|
| **117** | CLK1/GPIO_3 | PCK2/PC15 | Programmable Clock / GPIO 3 |
| **127** | CLK2/GPIO_4 | RK1/PB7 | Programmable Clock / GPIO 4 |
| **114** | PWM1/GPIO_14 | TIOA1/PC12 | PWM / Clock / GPIO 14 |
| **115** | PWM2/GPIO_15 | TIOB0/PD6 | PWM / Clock / GPIO 15 |

For more information on the A/D and Timer functions of the ATSAMA5D35 processor, users are referred to the TC section of the *ATSAMA5D35 User's Manual*.

**Module Status LED:**

A Green general-purpose Status LED is connected to PA26.

**Table 17: General Purpose IO**

| SODIMM Pin# | SoM Pin Name | Processor Pin Name(s) | Description |
|---|---|---|---|
| **40** | IRQC/GPIO_0 | TCLK1/PC16 | Interrupt C / GPIO 0 |
| **75** | IRQA/GPIO_1 | FIQ/PC31 | Interrupt A / GPIO 1 |
| **32** | IRQB/GPIO_2 | IRQ/PWML1/PE31 | Interrupt B / GPIO 2 |
| **117** | CLK1/GPIO_3 | PCK2/PC15 | Programmable Clock / GPIO 3 |
| **127** | CLK2/GPIO_4 | RK1/PB7 | Programmable Clock / GPIO 4 |
| **129** | AD1/GPIO_5 | AD0/PD20 | ADC CH1 / GPIO 5 |
| **130** | AD2/GPIO_6 | AD1/PD21 | ADC CH2 / GPIO 6 |
| **131** | AD3/GPIO_7 | AD2/PD22 | ADC CH3 / GPIO 7 |
| **132** | AD4/GPIO_8 | AD3/PD23 | ADC CH4 / GPIO 8 |
| **133** | SPI0_MI/GPIO_9 | SPI1_MISO/PC22 | SPI1 Master In / GPIO 9 |
| **134** | SPI0_MO/GPIO_10 | SPI1_MOSI/PC23 | SPI1 Master Out / GPIO 10 |
| **135** | SPI0_SCK/GPIO_11 | SPI1_SPCK/PC24 | SPI1 Serial Clock / GPIO 11 |
| **136** | SPI0_CS0/GPIO_12 | SPI1_NPCS2/TWCK1/PC27 | SPI1 Chip Select 0 / GPIO 12 |
| **105** | SPI0_CS1/GPIO_13 | SPI1_NPCS1/TWD1/PC26 | SPI1 Chip Select 1 / GPIO 13 |
| **114** | PWM1/GPIO_14 | TIOA1/PC12 | PWM / Clock / GPIO 14 |
| **115** | PWM2/GPIO_15 | TIOB0/PD6 | PWM / Clock / GPIO 15 |
| **48** | COMD TXD | TXD3/PE19 | SER E Transmit / GPIO |
| **49** | COMD RXD | RXD3/PE18 | SER E Receive / GPIO |

## 2.5 Power Connections

The SoM-A5D35 requires a 3.3V supply for the Bus and I/O voltages. The 1.2V core voltage is regulated on module from the 3.3V. The on-processor RTC also requires 3.3V and supplied by either a battery or the 3.3V power rail. Unlike some other modules no other supply voltage other than 3.3V is required.

**Table 18: Power Connections**

| SODIMM Pin# | SoM Pin Name | Processor Pin Name(s) | Description |
|---|---|---|---|
| **3,4,141,142** | 3.3VCC | 3.3VCC | 3.3 Volt I/O voltage to the processor |
| **1,2,52,53,58,59,62, 63,68,69,143,144** | GND | GND | Ground |
| **119** | VSTBY | VDDBU Battery Backup | Voltage standby, this is the backup voltage provided to the internal RTC of the processor. If RTC readings are not important for the application; this can be attached to the 3.3V rail. |
| **118** | ALT_VCC | Not Used | Not Required |
| **101** | AV_VCC | Not Used | Analog power. This is not required for the SoM- A5D35 |
| **99** | V_REF | Not Used | No external Analog Reference voltage is required for the SoM-A5D35. |

## 2.6 Boot Options

The SoM specification provides two pins for boot time configuration. On the SoM-A5D35, these are BMS and Flash Disable. The Boot Mode Select (BMS) pin allows the SoM-A5D35 to be low-level booted from either its internal ROM or external (carrier-resident) NOR flash. The Flash Disable pin should be tied to GND to enable the Serial Flash and the NAND Flash (if present on carrier). The Module can high-level boot from either the Serial Flash or the eMMC (selected through the low-level bootloader). It is recommended to high-level boot from the Serial Flash.

**Table 19: Boot Options**

| SODIMM Pin# | SoM Pin Name | Processor Pin Name(s) | Description |
|---|---|---|---|
| **41** | BOOT_OPTION1 | BMS | Boot Mode Select |
| **74** | BOOT_OPTION2 | Flash Disable | Serial Flash Disable, Not Connected to Processor |

### 2.7 Serial Flash

The Serial Flash is connected to SPI0 and uses SPI0_NPCS0 to enable it. The Serial Flash also has a Write-Protect Provision. To Write-Protect the Serial Flash pull SoM pin# 85 low. SoM pin# 85 is pulled up by a 10K ohm resistor on the module. If this feature is required it would be implemented on the carrier as a jumper or an I/O line. The Serial flash may be disabled in order to force the processor to boot from the internal ROM by pulling BOOT_OPTION2 (SoM pin# 74) high.

## 3 Design Considerations

One of the goals of the SoM-A5D35 is to provide a modular, flexible and inexpensive solution capable of delivering high-end microcontroller performance with low power requirements.

### 3.1 EMAC SoM 144 Pin Carriers

EMAC provides off-the-shelf carriers for the SoM-A5D35 module, the SoM-112ES and the SoM-150ES provide power to SoM modules and provides them with an extended range of I/O. These carrier boards come with full schematics and BOM, and can be used as is, or as a reference for a customer's own design.

https://shop.emacinc.com/product/som-112es-carrier-board/

https://shop.emacinc.com/product/som-150es-carrier-board/

EMAC also offers a semi-custom engineering service. By modifying an existing design, EMAC can offer quick-turn, low-cost engineering, for your specific application.

### 3.2 Power

The SoM-A5D35 requires a voltage of 3.3V at 250mA. For a bare-bones population, users can get away with using only 3.3V, and simply provide this to all the voltage inputs listed in Power Connections section. This however, will not provide battery backup for the RTC.

#### 3.2.1 Legacy

ALT_VCC is a legacy connection, required to support the SoM-400EM and may be used in future SoM modules. If general SoM compatibility is not an issue, then this can be tied to 3.3V. The SoM-A5D35 does not use this connection.

#### 3.2.2 Shutdown Logic Pins

The SHDN is a digital output only with a logical high of 3.3V, which is driven by the Shutdown Controller on the processor. The WKUP pin has a Maximum input voltage of 3.3V. Both of these pins are connected directly to the processor.

### 3.2.3 Battery Backup

The SoM-A5D35 contains 3 potentially non-volatile memory areas, the eMMC flash, the real-time clock (RTC), and the serial flash of the processor. The flash is always non-volatile, the real-time clock requires a backup voltage to maintain its data. This backup voltage comes from the VSTBY pin, and should be connected to 3.3 volts.

The RTC will draw approximately 10 uA when the processor is not powered by the 3.3V supply. The Static current can rise to 18uA if the temperature increases to 85° C. When the module is powered, no current is drawn from the backup battery supply. If the RTC is not needed, this can be tied to 3.3V.

The SoM-112ES and SoM-150ES provide battery backup voltage through a socketed BR2032, which is a standard 3V 190mA/H 20MM coin battery that can be picked up from most electronics stores.

### 3.2.4 Analog Reference

No external Analog Reference voltage (VREF) is required for the SoM-A5D35. An on-module 2.5V reference is provided. Analog input range is therefore 0 to 2.5V. This pin is normally a No Connect on the Module. This Reference uses power and therefore can be turned off by setting GPIO Port Line PA25 as an input, thus conserving about 3 mA.

### 3.2.5 Analog Voltage

When designing power for the Analog subsystem there are 4 major considerations, range and accuracy output drive, and rise time.

- **Range**

  The AV_VCC pin normally provides the range. However, on the SoM-A5D35 the Analog VCC (VDDANA) is directly connected to filtered 3.3V. The power supplied to the analog subsystem limits the range of voltages that can be accurately measured. The internal analog converters cannot measure a voltage higher than the reference voltage provided on the SoM. The Analog input range is 0 to 2.5V.

- **Accuracy**

  The accuracy of the A/D converters is determined by the V_REF pin, which provides the reference voltage to the analog subsystem. The stability of the voltage between this pin and ground will affect the accuracy of the subsystem's measurements. No external Analog Reference voltage is required for the SoM-A5D35. An on-module 2.5V reference is provided. Analog input range is therefore 0 to 2.5V.

# 4 Software

The SoM-A5D35 offers a wide variety of software support from both open source and proprietary sources. The hardware core was designed to be software compatible with the Atmel AT91SAMA5D3x-EK reference design, which is supported by Linux.

For more information on Linux Software Support, please visit the EMAC Wiki Software Section at:
http://wiki.emacinc.com/wiki/Product_wiki

## 4.1 Das U-Boot

EMAC utilizes Das U-Boot for its ARM based products. U-Boot is an open source/cross-architecture platform independent bootloader. It supports reading and writing to the flash, auto-booting, environmental variables, and TFTP. Das U-boot can be used to upload and run and/or reflash the OS or to run stand- alone programs without an OS. Products are shipped with a valid MAC address installed in flash in the protected U-boot environmental variable “ethaddr”. At boot time U-Boot automatically stores this address in a register within the MAC, which effectively provides it to any OS loaded after that point.

## 4.2 Embedded Linux

EMAC Open Embedded Linux (EMAC OE Linux) is an open source Linux distribution for use in embedded systems. The EMAC OE Linux Build is based on the Open Embedded (www.openembedded.org) and Yocto (www.yoctoproject.org) Linux build systems. Open Embedded is a superior Linux distribution for embedded systems. Custom Linux builds are also available on request.

The distribution contains everything a user could expect from a standard Linux kernel: powerful networking features, advanced file system support, security, debugging utilities, and countless other features.

The basic root file system includes:

- Busybox
- Hotplugging support
- APM utilities for power management
- Openssh SSH server
- lighttpd HTTP server
- EXT4 file system with utilities

#### 4.2.1 Linux with PREEMPT RT

PREEMPT RT provides pseudo real time to the kernel and can be used to schedule tasks with hard deadlines and minimal latencies. The PREEMPT RT build is an option to the standard Linux build and is available for a one-time inexpensive support/installation fee.

#### 4.2.2 Linux Packages

EMAC provides support for many Linux Packages such as: PHP, SQLite, Perl, SNMP, DHCP Server, etc. As with the PREEMPT RT Option, other Packages can be added to the standard Linux file system and are available for a one-time inexpensive support/installation fee.

#### 4.2.3 Linux Patches

In addition to standard Embedded Linux support, EMAC has released a number of patches and device drivers from the open source community and from internal EMAC engineering into its standard distribution. Along with kernel patches, EMAC provides the binaries for the kernel and root file system.

### 4.3 Qt Creator

Qt Creator is a cross-platform IDE (Integrated Development Environment) tailored to the needs of Qt developers but works well for Headless applications as well. EMAC provides sample code as projects that can be imported into Qt Creator. Qt Creator supports remote deployment and source debugging.

http://wiki.qt.io/Main

### 4.4 ARM EABI Cross Compiler

The popular open source gcc compiler has a stable build for the ARM family. EMAC uses this compiler by defualt. The Embedded Linux kernel and EMAC Qt Creator projects use this compiler for building ARM stand alone, and OS specific binaries. The EMAC Qt Creator provides source level debugging over Ethernet or serial using gdbserver. The Linux binaries for the ARM EABI cross compiler are available online along with the SDK. See the EMAC wiki for further information.