SoM-3354M

User Manual

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(For Use with Rev 5 or higher)

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1 Introduction

This document describes the EMAC SoM-3354M System on Module. The SoM-3354M is designed to be compatible with EMAC's 200-pin SODIMM form factor. This module is built around the Texas Instruments AM3354 ARM Cortex-A8-based microprocessor, which provides several of its key features. The SoM-3354M has an onboard Ethernet PHY, 4 serial ports, eMMC, USB Switch, SPI flash, and DDR3 SDRAM. In addition to these standard SoM features, the SoM-3354M also features a fast 32-bit core, hardware graphics accelerators, open-source software support, and a wide range of controller IO pins.

1.1 Features

- **Small, 200-pin SODIMM form factor (2.66" x 2.375")**
- **Texas Instruments AM3354 ARM Cortex-A8 1Ghz processor (s-PBGA 324)**
- **10/100 BaseT Ethernet with on-board PHY**
- **4x Serial ports (1x with full handshake and 2x with RTS/CTS handshake)**
- **2x USB 2.0 (High Speed) Host ports (uses a USB Hub chip)**
- **1x USB 2.0 (High Speed) OTG Host/Device port**
- **512 MB of DDR3L SDRAM**
- **16 MB of SPI Flash**
- **4GB eMMC Flash**
- **External MMC/SD card interface with card detect**
- **Real-Time Clock Internal with battery-backed provision**
- **2x SPI ports**
- **I2C hardware port**
- **Synchronous I2S analog audio interface port**
- **1x CAN port (transceiver on carrier)**
- **4x Timer/Counter/PWM**
- **Internal Resistive Touchscreen Controller w/4-channel 12-bit Analog-to-Digital converter**
- **16-bit TFT LCD interface**
- **True Random Number Generator**
- **JTAG for debugging, including real-time trace**
- **FREE Qt Creator-based IDE**

2 Hardware

2.1 Specifications

- **CPU:** Texas Instruments AM3354 Processor running at 1 GHz
- **Flash:** 4GB of eMMC and 16MB
- **RAM:** 512MB of DDR3L SDRAM
- **Video:** 3D Accelerated 16 Bit LCD Video Interface with up to 2048 x 2048 resolution
- **Touchscreen:** 12-bit 4-wire analog resistive touchscreen interface
- **Flash Disk:** Up to 16GB eMMC Flash Upgrade
- **System Reset:** Processor Internal Reset Management with External Reset Provision
- **Timer/Counters/PWM:** 2x shared with GPIO, 2x shared with UART1 handshaking
- **Digital I/O:** 16 pins are allocated to be primarily GPIOs, many shared with other functions.
- **Analog I/O:** 8 Channels Total, 4 are shared by the resistive touchscreen
- **Power:** Power Management Controller allows for selective shutdown capability of processor I/O functionality
- **JTAG:** JTAG for debugging, including real-time trace
- **Clocks:** 2x Programmable Oscillator Outputs ranging from 2.5kHz to 200MHz

Serial Interfaces

- **UARTS:** 2x with RTS/CTS handshaking, 1x with full handshaking, 1x without handshaking
- **SPI:** 1x High-Speed SPI port, and 1x High-Speed SPI port shared with GPIO, 4x chip slave selects
- **Audio:** 1x I2S Synchronous Serial Controller with analog interface support
- **USB:** 2x USB 2.0 High-Speed Host Ports and 1 USB 2.0 High-Speed Host or Device (OTG) software configurable
- **I2C:** I2C hardware port

Ethernet Interface

- **MAC:** 1x MAC (MII) which connects to an onboard PHY
- **PHY:** Micrel KSZ8041NL with software PHY shutdown control
- **Interface:** IEEE 802.3u 10/100 BaseT Fast Ethernet (requires external magnetics and jack)

Bus Interface:

- ARM EBI accessible through SODIMM providing 11 address lines, 8 data lines and control lines

Mechanical and Environmental

- **Dimensions:** 200 pin SODIMM form factor with the length dimension extended (2.66" x 2.375")
- **Power Supply Voltage:** +3.3VDC +/-5%
- **Operating Temperature:** -40°C to 85°C (-40°F to 185°F), fanless operation
- **Operating Humidity:** 0% to 90% relative humidity, non-condensing

2.2 Real-Time Clock

The real-time clock is a precise timer that can generate interrupts at intervals specified by the user. The internal RTC on the AM3354 processor draws too much current for long-term use, so an external Maxim DS1337 I2C RTC is used.

2.3 Watchdog Timer

A 32 kHz clock drives the AM3354 internal watchdog timers. Each timer contains a free-running, 32-bit up counter. Each counter has an 8-bit, programmable clock divider. Timeout events can trigger reset and interrupt events.

2.4 External Connections

The SoM-3354M connects to a carrier board containing its connectors, power supply, and any expansion IO, through a standard gold-plated SODIMM 200-pin connection shown below.

The use of the DDR SODIMM form-factor for EMAC's SoMs is a sound choice that has been proven rugged and reliable in the laptop and embedded SBC markets.

The SoM model will fit any standard 200-pin DDR1 SODIMM socket (but not DDR2 sockets). These connections are designed according to the 200-pin SoM specification to be compatible with all EMAC 200-pin SoMs.

This section defines the signal mapping for the SODIMM pins. Notes about the signal descriptions that follow:

- Signals are 3.3V unless otherwise specified.
- Signals names that include "~" are active low, and are normally pulled high on the SOM.
- "NC" in the tables stands for Not Connected, which means that although a signal is defined in the 200-pin SOM specification, it is not used by this SOM.

2.4.1 System Control & External Bus

The SoM-3354M provides a flexible external bus for connecting peripherals. The CPLD of the SoM-200GS connects through a subset of these connections.

Table 1: System Control & External Bus

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
145	GP_CSA	GPMC_CSN0	GPIO 1_29	Gen Purpose Chip Select CS0
146	GP_CSB	GPMC_CSN4	GPIO 0_30	Gen Purpose Chip Select CS4
147	GP_CSC	GPMC_CSN5	GPIO 0_31	Gen Purpose Chip Select CS5
148	GP_CSD/Shutdown	GPMC_CSN6	GPIO 1_28	Gen Purpose Chip Select CS6
149	~WR	GPMC_WE	GPIO 2_4	Write Signal
150	~RD/TIP	GPMC_OE	GPIO 2_3	Read Signal
151	~RST_IN	SYS_RESETN		Processor Reset
152	~RST_OUT	SYS_RESETN		Processor Reset
153	~WAIT	GPMC_WAIT1	GPIO 2_1	Shutdown Control
154	~FLASH WP	NC		Flash Write Protect
54	WAKEUP	NC		Processor Wakeup Input
175-186	A0 – A11	GPMC_A0 – GPMC_A11	GPIO 1_16-1_27	Address Bus
159-166	D0 – D7	GPMC_AD0 – GPMC_AD7	GPIO 1_0-1_7	Data Bus
167-174	D8 – D15	NC		Data Bus
187-196	A12- A21	NC		Address Bus

2.4.2 JTAG

The SoM specification allows for access to the JTAG lines for the AM3354 processor. These connections will allow the Flash to be programmed in circuit via the processor and also the capability to debug software.

Table 2: Processor JTAG

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
139	JTAG_TCK	TCK	JTAG Clock
140	JTAG_TDI	TDI	JTAG Serial In
141	JTAG_TDO	TDO	JTAG Serial Out
142	JTAG_TMS	TMS	JTAG Operation Mode
143	JTAG_TRST	TRSTn	Test Reset Signal

2.4.3 Ethernet

The SoM-3354M provides a Microchip Technology KSZ8041 Ethernet 10/100 PHY IC onboard. Carrier designers need only to run these lines through the appropriate magnetics layer to have a functional Ethernet connection. Remember, the RX and TX lines are differential pairs and need to be routed as such.

The state of the LED/configuration pins at reset determines the Ethernet's configuration (10-baseT, 100-baseT, auto-config) and the function of the LEDs. The SoM-200ES pulls them all high, which configures the chip for network auto-config, with ETH_LED1 functioning as an active low link and ETH_LED2 functioning as an active low Activity status (Refer to Carrier schematics).

Table 3: 100 BaseT Ethernet

SODIMM Pin#	SoM Pin Name	{PHY} Pin Name	Description
12	GIG D-	NC	NC
14	GIG D+	NC	NC
13	GIG C-	NC	NC
15	GIG C+	NC	NC
16	Ethernet_Rx-/GIG B-	Rx-	Rx-
18	Ethernet_Rx+/GIG B+	Rx+	Rx+
17	Ethernet_Tx-/GIG A-	Tx-	Tx-
19	Ethernet_Tx+/GIG A+	Tx+	Tx+
38	LED_LINK/CFG_2	LED0/NWAYEN	LED 0 Output
39	LED_ACT/CFG_3	LED1/SPEED	LED 1 Output

2.4.4 I2C

The 200-pin SoM specification calls for a two-wire I2C port. The SoM-3354M has a native hardware I2C port. The I2C addresses used by SOM devices are as follows:

- PMIC (0x12 / 0x2D)
- Touch Screen Controller (0x48)
- Clock Generator (0x60)
- EEPROM (0x50)
- RTC (0x68)

Table 4: I2C Port

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
29	CLK	I2C0_SCL	GPIO 3_6	I2C Clock
30	DATA	I2C0_SDA	GPIO 3_5	I2C Data Line

2.4.5 USB

The 200-pin SoM specification provides for 2 USB hosts and 1 USB device or OTG port. The AM3354 provides a single USB 2.0 host port interface, which is connected to an onboard Hub to provide two host ports. The OTG port connects directly to the processor.

Table 5: USB

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
5	Host_A+	USBDP_DN1 (from Hub)	Host USB Switch Port0 + pin
7	Host_A-	USBDM_DN1 (from Hub)	Host USB Switch Port0 – pin
6	Host_B+	USBDP_DN2 (from Hub)	Host USB Switch Port1 + pin
8	Host_B-	USBDM_DN2 (from Hub)	Host USB Switch Port1 – pin
9	Host/Device/OTC_C-	USB0_DM	OTG USB 2.0 Port0 – pin
11	Host/Device/OTG_C+	USB0_DP	OTG USB 2.0 Port0 + pin
10	USB_OTG_VBUS	USB0_VBUS	OTG VBUS
40	USB_OTG_ID	USB0_ID	OTG ID

2.4.6 SPI

The AM3354 processor provides 4 SPI channels for communicating with peripheral devices. Two of the SPI channels have been provided via the SoM edge connector. The first table below lists the lines for the dedicated SPI channel. SPI1 is shared within the GPIO lines.

Table 6: SPI Channel 0

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
22	SPI_MI	SPI0_D0	GPIO 0_3	SPI0 serial data in
23	SPI_MO	SPI0_D1	GPIO 0_4	SPI0 serial data out
24	SPI_SCK	SPI0_SCLK	GPIO 0_2	SPI0 serial clock out
25	SPI_CS0	GPMC_AD15	GPIO 1_15	SPI0 slave select line 0
26	SPI_CS1	EMU1	GPIO 3_8	SPI0 slave select line 1
27	SPI_CS2	GPMC_AD14	GPIO 1_14	SPI0 slave select line 2
28	SPI_CS3	MCASP0_ACLKR	GPIO 3_18	SPI0 slave select line 3

Table 7: SPI Channel 1

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
125	GPIO11	UART0_CTSn	GPIO 1_8	SPI1 serial data in
126	GPIO12	UART0_RTSn	GPIO 1_9	SPI1 serial data out
127	GPIO13	ECAP0_IN_PWM0_OUT	GPIO 0_7	SPI1 serial clock out

2.4.7 SDIO/Multimedia Card

The AM3354 processor provides multiple 4-bit MMC/SD card interfaces using the MCI lines. The SoM-200ES & 210ES Carrier boards utilize this MMC/SD interface. An additional SD card interface is used for an onboard eMMC.

Table 8: MMC

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
31	SDCLK	GPMC_CSn1	GPIO 1_30	MCI Clock
32	CMD	GPMC_CSn2	GPIO 1_31	MCIA Command
33	DAT0	GPMC_AD8	GPIO 0_22	MCIA D0
34	DAT1	GPMC_AD9	GPIO 0_23	MCIA D1
35	DAT2	GPMC_AD10	GPIO 0_26	MCIA D2
36	DAT3	GPMC_AD11	GPIO 0_27	MCIA D3
37	Card_Detect	GPMC_AD12	GPIO 1_12	Card Detect

2.4.8 Serial Ports

The 200-pin SoM specification has the provision for 4 serial ports. The AM3354 processor provides full modem handshaking for COMA. The SoM-3354M uses a Dual UART chip to provide additional serial ports. The Si5351A clock generator chip provides the clock source for the onboard Dual UART (TL16C2550IPFB) chip.

Table 9: Serial Ports

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
95	COMA_TXD	EUART0_TX (Dual UART chip)		COMA TX/GPIO
96	COMA_RXD	EUART0_RX (Dual UART chip)		COMA RX/GPIO
97	COMA_CTS	EUART0_CTS (Dual UART chip)		COMA CTS/GPIO
98	COMA_RTS	EUART0_RTS (Dual UART chip)		COMA RTS/GPIO
99	COMA_DTR	EUART0_DTR (Dual UART chip)		COMA DTR/GPIO
100	COMA_DSR	EUART0_DSR (Dual UART chip)		COMA DSR /GPIO
101	COMA_RI	EUART0_RI (Dual UART chip)		COMA RING/GPIO
102	COMB_TXD	UART0_TXD	GPIO 1_11	COMB TX/GPIO
103	COMB_RXD	UART0_RXD	GPIO 1_10	COMB RX/GPIO
104	COMB_CTS	NC		COMB CTS/GPIO
105	COMB_RTS	NC		COMB RTS/GPIO
106	COMC_TXD	UART1_TXD	GPIO 0_15	COMC TX/GPIO
107	COMC_RXD	UART1_RXD	GPIO 0_14	COMC RX/GPIO
108	COMC_CTS	UART1_CTSn	GPIO 0_12	COMC CTS/GPIO
109	COMC_RTS	UART1_RTSn	GPIO 0_13	COMC RTS/GPIO
110	COMD_TXD	EUART1_TX (Dual UART chip)		COMD TX/GPIO
111	COMD_RXD	EUART1_RX (Dual UART chip)		COMD RX/GPIO
112	COMD_CTS	EUART1_CTS (Dual UART chip)		COMD CTS/GPIO
113	COMD_RTS	EUART1_RTS (Dual UART chip)		COMD RTS/GPIO

2.4.9 I2S

The AM3354 provides multiple I2S audio ports that are accommodated within the SoM specification. Note that there is no CODEC on the SoM and therefore must be provided on the Carrier. In addition, the CODEC will require either SPI or I2C for control. The Master clock is provided by a clock generator chip to drive the 12.288MHZ oscillator.

Table 10: I2S

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
86	AudioA_SCLK	MCASP0_ACLKX	GPIO 3_14	I2S Serial Clock
87	AudioA_LRCLK/Frame	MCASP0_FSX	GPIO 3_15	I2S Left / Right Clock
88	AudioA_MCLK	N/A	Si5351A (CLK_2)	I2S Master Clock
89	AudioA_DIN	MCASP0_AXR0	GPIO 3_16	I2S Data Input
90	AudioA_DOUT	MCASP0_AXR1	GPIO 3_20	I2S Data Output

2.4.10 CAN

The AM3354 provides a High-End CAN Controller (HECC) internally.

Table 11: CAN

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
93	CANTX	MII1_TXD3	GPIO 0_16	CAN Transmit
94	CANRX	MII1_TXD2	GPIO 0_17	CAN Receive

2.4.11 IRQs

The 200-pin SoM specification allocates three pins as IRQs. The AM3354 processor can use virtually any GPIO pin to trigger an interrupt. EMAC used the following GPIO lines for general-purpose IRQs.

Table 12: IRQs

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
129	IRQA	XDMA_EVENT_INTR0	GPIO 0_19	Interrupt A
130	IRQB	MCASP0_FSR	GPIO 3_19	Interrupt B
131	IRQC	MCASP0_AHCLKX	GPIO 3_21	Interrupt C

2.4.12 Oscillators

The 200-pin SoM specification provides for two general-purpose oscillators. These frequencies can vary slightly between modules depending on how they are generated and some modules may not provide 50% duty cycles. The AM3354 uses a clock generator chip (Si5351A) to generate these frequencies. The frequencies are programmable via software.

Table 13: Oscillators

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
132	OSC0	N/A	Si5351A (CLK0)	Clock
133	OSC1	N/A	Si5351A (CLK1)	Clock

2.4.13 Touchscreen / Analog-to-Digital Converter (ADC)

The 200-pin SoM specification allocates SoM pins that can be used as Touchscreen or ADC inputs. The AM3354 has a resistive touchscreen controller that utilizes SoM pins 45-48. The touchscreen controller is supplied by an on-board 3.3V reference. The ADC inputs on pins 49-52 can accept a range of 0 to 1.8V. The reference voltage for the ADC inputs on pins 49-52 is generated on the SOM, and not available from a SODIMM pin.

Table 14: Analog to Digital Converters

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
45	X+/Xr/ADC0	(Touchscreen Controller)	X+
46	X-/Xl/ADC1	(Touchscreen Controller)	X-
47	Y+/Yu/ADC2	(Touchscreen Controller)	Y+
48	Y-/Yd/ADC3	(Touchscreen Controller)	Y-
49	SX+/ADC4	AIN4	GP ADC Input 4
50	SX-/ADC5	AIN5	GP ADC Input 5
51	SY+/ADC6	AIN6	GP ADC Input 6
52	SY-/ADC7	AIN7	GP ADC Input 7

2.4.14 GPIO

This section provides for the SoM general purpose IO section. All of these pins can be configured to be general-purpose digital ports. They can also be configured to take advantage of several of the functions of the SoM-3354M's internal silicon. The additional SPI port is brought out here, as well as all of the available IRQs, and the pins for general-purpose timer/counters.

Table 15: General Purpose IO

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
114	GPIO0	GPMC_AD13	GPIO 1_13	GPIO/LCD Backlight On/Off
115	GPIO1	EGPIO0 (GPIO EXPANDER)		GPIO
116	GPIO2	EGPIO1 (GPIO EXPANDER)		GPIO
117	GPIO3	EGPIO2 (GPIO EXPANDER)		GPIO
118	GPIO4	EGPIO3 (GPIO EXPANDER)		GPIO
119	GPIO5	EGPIO4 (GPIO EXPANDER)		GPIO
120	GPIO6	EGPIO5 (GPIO EXPANDER)		GPIO
121	GPIO7	EGPIO6 (GPIO EXPANDER)		GPIO
122	GPIO8	EGPIO7 (GPIO EXPANDER)		GPIO
123	GPIO9	EMU0	GPIO 3_7	GPIO
124	GPIO10	USB0_DRVVBUS	GPIO 0_18	GPIO
125	GPIO11	UART0_CTSn	GPIO 1_8	GPIO/SPI_MISO
126	GPIO12	UART0_RTSn	GPIO 1_9	GPIO/SPI_MOSI
127	GPIO13	ECAP0_IN_PWM0_OUT	GPIO 0_7	GPIO/SPI_SCLK/ECAP/PWM
128	GPIO14	GPMC_ADVn_ALE	GPIO 2_2	GPIO/TIMER
134	GPIO15	XDMA_EVENT_INTR1	GPIO 0_20	GPIO/TIMER

2.4.15 LCD

The 200-pin SoM specification has provision for up to 16-bit LCDs (565 RBG mode). These lines can also be used to provide analog VGA connectivity for use with a conventional monitor by adding a video DAC to the Carrier. A Brightness PWM is also provided to allow for software control of the LCD's Brightness.

Table 16: LCD

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
57	LCD_BLUE0	LCD_DATA0	GPIO 2_6	LCD BLUE0
58	LCD_BLUE1	LCD_DATA0	GPIO 2_6	LCD BLUE1
59	LCD_BLUE2	LCD_DATA0	GPIO 2_6	LCD BLUE2
60	LCD_BLUE3	LCD_DATA0	GPIO 2_6	LCD BLUE3
61	LCD_BLUE4	LCD_DATA1	GPIO 2_7	LCD BLUE4
62	LCD_BLUE5	LCD_DATA2	GPIO 2_8	LCD BLUE5
63	LCD_BLUE6	LCD_DATA3	GPIO 2_9	LCD BLUE6
64	LCD_BLUE7	LCD_DATA4	GPIO 2_10	LCD BLUE7
65	LCD_GREEN0	LCD_DATA5	GPIO 2_11	LCD GREEN0
66	LCD_GREEN1	LCD_DATA5	GPIO 2_11	LCD GREEN1
67	LCD_GREEN2	LCD_DATA5	GPIO 2_11	LCD GREEN2
68	LCD_GREEN3	LCD_DATA6	GPIO 2_12	LCD GREEN3
69	LCD_GREEN4	LCD_DATA7	GPIO 2_13	LCD GREEN4
70	LCD_GREEN5	LCD_DATA8	GPIO 2_14	LCD GREEN5
71	LCD_GREEN6	LCD_DATA9	GPIO 2_15	LCD GREEN6
72	LCD_GREEN7	LCD_DATA10	GPIO 2_16	LCD GREEN7
73	LCD_RED0	LCD_DATA11	GPIO 2_17	LCD RED0
74	LCD_RED1	LCD_DATA11	GPIO 2_17	LCD RED1
75	LCD_RED2	LCD_DATA11	GPIO 2_17	LCD RED2
76	LCD_RED3	LCD_DATA11	GPIO 2_17	LCD RED3
77	LCD_RED4	LCD_DATA12	GPIO 0_8	LCD RED4
78	LCD_RED5	LCD_DATA13	GPIO 0_9	LCD RED5
79	LCD_RED6	LCD_DATA14	GPIO 0_10	LCD RED6
80	LCD_RED7	LCD_DATA15	GPIO 0_11	LCD RED7
81	LCD_HORZ/LP	LCD_HSYNC	GPIO 2_23	Horizontal Sync
82	LCD_VERT/FP/FLM	LCD_VSYNC	GPIO 2_22	Vertical Sync
83	LCD_ENABLE/DE/M	LCD_AC_BIAS_EN	GPIO 2_25	Enable
84	LCD_CLK/SFK/SHFCLK	LCD_PCLK	GPIO 2_24	LCD Clock
85	BCKLIGHT	MCASP0_AHCLKR	GPIO 3_17	Backlight Brightness Control

2.4.16 Power Connections

The SoM-3354M requires a 3.3V supply for the bus and I/O voltages. The 1.8V core voltage is regulated on module from the 3.3V. Unlike some other modules, no supply voltage other than 3.3V is required.

Table 17: Power Connections

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
3,4,43,44,135, 136,197,198	3.3VCC	3.3VCC	3.3 Volt SoM Supply Voltage
1,2,20,21,41,42, 91,92,137,138, 155,156,199,200	GND	GND	Digital Ground
53	Analog_GND	AGND	Analog Ground
56	VSTBY	Vstandby_3.3	Voltage standby, this is the backup voltage provided to the SoM's RTC. If RTC readings are not important for the application, this can be attached to the 3.3V rail.
55	AV_REF	NC	The analog reference used by the AM3354 (processor pin VREFP) is generated by an onboard 1.8V regulator, which is not available outside of the SOM. AV_REF from the card edge is not used.

2.4.17 Boot Options

The 200-pin SoM specification provides two pins for boot-time configuration. On the SoM-3354M, they are used to select between four boot modes. The SoM-3354M is capable of booting out of Serial, Ethernet, SPI Flash, or USB. Booting from eMMC is only possible with a custom-populated version. Contact EMAC for more details.

Table 18: Boot Options

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
157	BOOT_OPTION0	SYS_BOOT[4:0]	Boot0 Option Select
158	BOOT_OPTION1	SYS_BOOT[4:0]	Boot1 Option Select

BOOT1	BOOT0	SYS_BOOT[4.0]	Boot Mode	Description
0	0	10110	SPI0	Boot from SPI Flash
0	1	10111	MMC0	Boot from on-board eMMC
1	0	10110	UART0/EMAC1	Boot from Serial/Ethernet
1	1	10111	UART0/USB0	Boot from Serial/USB

2.5 Module Status LED

The SoM-3354M provides a user-programmable, green, status LED. To control this LED, use GPIO port line GPIO3_4. Setting the port line high will turn on the LED.

3 Design Considerations

One of the goals of the SoM-3354M is to provide a modular, flexible, and inexpensive solution capable of delivering high-end microcontroller performance with low power requirements.

3.1 Off-the-Shelf Carriers

Many SoM-3354M applications can make use of EMAC's many 200-pin off-the-shelf carriers, Links have provided for two such carriers. These carriers provide power to the SoM as well as a wealth of connectors and interfaces to access peripheral I/O including audio and LCD.

3.1.1 SoM-200GS

This is a Half-EBX mounting hole form factor (4.37" x 6.00") carrier that comes with a 4.3" LCD interface as well as full schematics and a BOM, and can be used as is, or as a reference for a customer's own design.

- 10/100/1000 BaseT Ethernet with Status LEDs
- 3 serial RS232 ports and 1 RS232/422/485 port
- Resistive Touchscreen interface
- 480 x 272 Graphic LCD with Touchscreen
- Battery for nonvolatile RAM and Real Time Clock
- Micro SD Card Socket
- 2 USB Host & 1 USB OTG ports
- 1 I2S Audio port with Line-In/Line-Out
- 5 VDC Power Requirement

http://emacinc.com/products/system_on_module/SoM-200GS

3.1.2 SoM-250GS

This is a 6.55" x 4.15" carrier designed as a basis for a 7" or 10" Panel PC.

- 10/100/1000 BaseT Ethernet with onboard Magnetics and RJ45
- 3 serial RS232 ports and 1 RS232/422/485 port
- Resistive Touchscreen interface
- 800 x 480 (WVGA) or 1024 x 600 (WSVGA) Graphic LCD with Touchscreen
- Battery for nonvolatile RAM and Real Time Clock
- Micro SDHC/MMC Flash Card Socket

- 2 USB Host & 1 USB OTG ports
- 1 I2S Audio port with Line-In/Line-Out
- 1 Audio Beeper
- Timer/Counters and Pulse Width Modulation (PWM) ports
- Operating Voltage of 12 to 28 Vdc.
- Graphic LCD Interface

http://emacinc.com/products/system_on_module/SoM-250GS

3.2 Power

The SoM-3354M requires a voltage of 3.3V at 650mA. For a bare-bones population, users can get away with using only 3.3V, and simply provide this to all the voltage inputs listed in the Power Connections section. This, however, will not provide battery backup for the RTC.

3.2.1 Legacy

ALT_VCC is a legacy connection, required to support the SoM-400EM and may be used in future SoM modules. The SoM-3354M does not use this connection, so If general SoM compatibility is not an issue, then this can be tied to 3.3V in a carrier designed for this SoM.

3.2.2 Shutdown Logic Pins

The SHDN is a digital output only with a logical high of 3.3V, which is driven by the Shutdown Controller on the processor. The WKUP pin has a Maximum input voltage of 3.3V. Both of these pins are connected directly to the processor.

3.2.3 Battery Backup

The SoM-3354M real-time clock (RTC) requires a backup voltage to maintain its data. This backup voltage comes from the VSTBY pin and should be connected to 3.0 to 3.3 volts.
The SoM-250GS provides battery backup voltage through a socketable CR2032, which is a standard 3V 220mA/H 20MM coin battery that can be picked up from most electronics stores.

The VSTBY pin will draw approximately 0.45uA when the processor is not powered by the 3.3V supply. Be aware that the static current can rise as the temperature rises toward 85° C. When the module is powered, no current is drawn from the backup battery supply. If RTC backup is not needed, this can be tied to 3.3V.

4 Software

The SoM-3354M offers a wide variety of software support from both open-source and proprietary sources. The hardware core utilizes the AM3354 ARM Cortex-A8, which is supported by Linux. For more information on Linux Software Support, please visit the EMAC Wiki Software Section at:

http://wiki.emacinc.com/wiki/Product_wiki

4.1 Das U-Boot

EMAC utilizes Das U-Boot for its ARM-based products. U-Boot is an open-source/cross-architecture platform independent bootloader. It supports reading and writing to the flash, auto-booting, environmental variables, and TFTP. Das U-boot can be used to upload and run and/or reflash the OS or to run stand-alone programs without an OS. Products are shipped with a valid MAC address installed in flash in the protected U-boot environmental variable “ethaddr”. At boot time U-Boot automatically stores this address in a register within the MAC, which effectively provides it to any OS loaded after that point.

4.2 Embedded Linux

EMAC Open Embedded Linux (EMAC OE Linux) is an open-source Linux distribution for use in embedded systems. The EMAC OE Linux Build is based on the Open Embedded (www.openembedded.org) and Yocto (www.yoctoproject.org) Linux build systems. Open Embedded is a superior Linux distribution for embedded systems. Custom Linux builds are also available on request.

The distribution contains everything a user could expect from a standard Linux kernel: powerful networking features, advanced file system support, security, debugging utilities, and countless other features.

The basic root file system includes:

- Busybox
- Hotplugging support
- APM utilities for power management
- Openssh SSH server
- lighttpd HTTP server
- EXT4 file system with utilities

4.2.1 Linux with PREEMPT RT

PREEMPT RT provides pseudo real time to the kernel and can be used to schedule tasks with hard deadlines and minimal latencies. The PREEMPT RT build is an option to the standard Linux build and is available for a one-time inexpensive support/installation fee.

4.2.2 Linux Packages

EMAC provides support for many Linux Packages such as: PHP, SQLite, Perl, SNMP, DHCP Server, Chromium, etc. As with the PREEMPT RT Option, other Packages can be added to the standard Linux file system and are available for a one-time inexpensive support/installation fee.

4.2.3 Linux Patches

In addition to standard Embedded Linux support, EMAC has released several patches and device drivers from the open-source community and from internal EMAC engineering into its standard distribution. Along with kernel patches, EMAC provides the binaries for the kernel and root file system.

4.3 Qt Creator

Qt Creator is a cross-platform IDE (Integrated Development Environment) tailored to the needs of Qt developers but works well for Headless applications as well. EMAC provides sample code as projects that can be imported into Qt Creator. Qt Creator supports remote deployment and source debugging.

http://wiki.qt.io/Main

4.4 ARM EABI Cross Compiler

The popular open-source GCC compiler has a stable build for the ARM family. EMAC uses the 4.9.1 version of the ARM EABI compiler. The Embedded Linux kernel and EMAC Qt Creator projects use this compiler for building ARM stand-alone, and OS-specific binaries. The EMAC Qt Creator provides source-level debugging over Ethernet or serial using gdbserver. The Linux binaries for the ARM EABI cross compiler are available online along with the SDK. See the EMAC wiki for further information.