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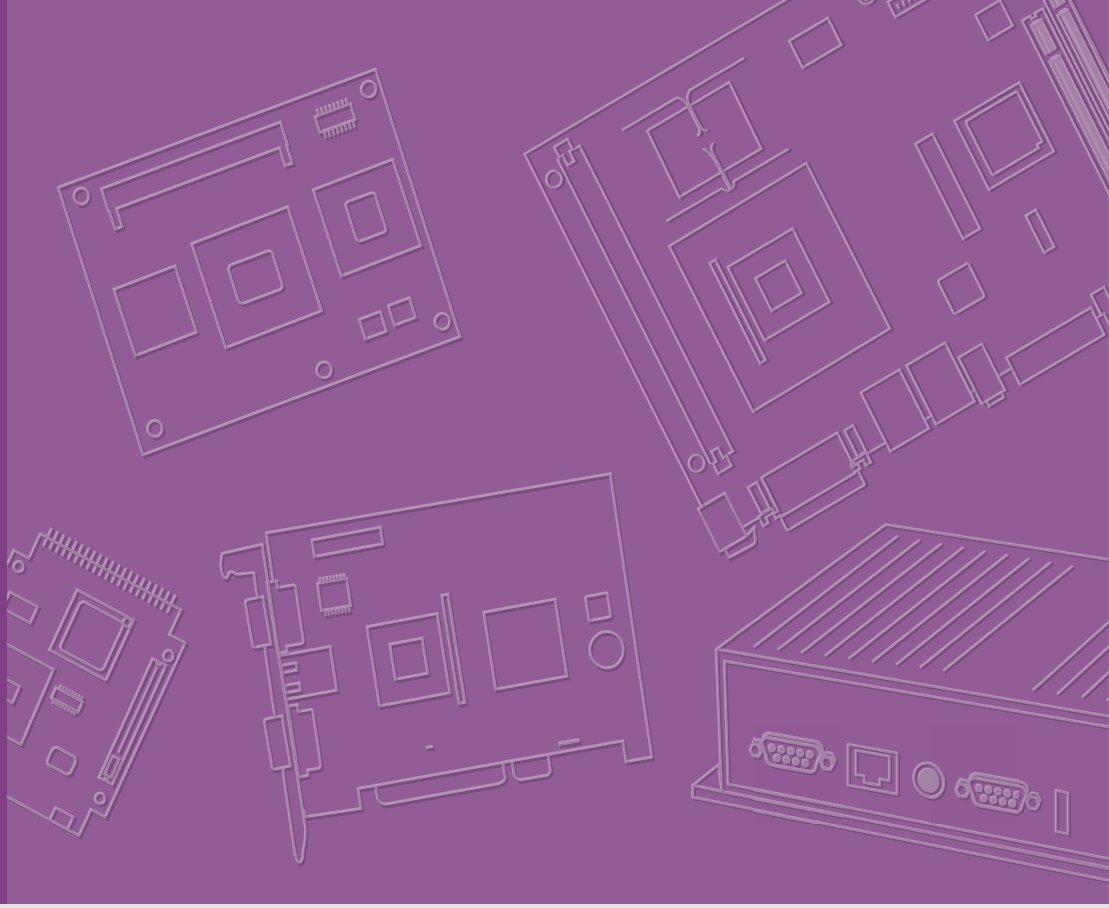

User Manual

MIO-5154

Intel® Core™ i3-N305 Processor, Intel® Processor N-series 3.5" SBC (Code name: Alder Lake N)

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Part No. 2006515400 Edition 1

Printed in China January 2024

Product Warranty (2 Years)

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This warranty does not apply to any products that have been repaired or altered by persons other than repair personnel authorized by Advantech, or products that have been subject to misuse, abuse, accident, or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

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1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages displayed when the problem occurs.
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4. Carefully pack the defective product, a completed Repair and Replacement Order Card, and a proof of purchase date (such as a photocopy of your sales receipt) into a shippable container. Products returned without a proof of purchase date are not eligible for warranty service.
5. Write the RMA number clearly on the outside of the package and ship the package prepaid to your dealer.

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Declaration of Conformity

CE

This product has passed the CE test for environmental specifications. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by ESD (Electrostatic Discharge) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

FCC Class B

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Caution! *There is a danger of a new battery exploding if it is incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.*

Technical Support and Assistance

1. Visit the Advantech web site at www.advantech.com/support where you can find the latest information about the product.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

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Packing List

Before you begin installing your card, please make sure that the following materials have been shipped:

- 1 x MIO-5154 SBC
- 1 x SATA Cable 30cm (p/n: 1700006291)
- 1 x SATA Power Cable 35cm (p/n: 1700031583-01)
- 1 x USB 3.0 Cable 35cm (p/n: 1700032181-01)
- 1 x Audio Cable 20cm (p/n: 1700019584-01)
- 2 x COM RS-232/422/485 Cable 20cm (p/n: 1700030404-01)
  - 1 x Heatsink for 15W/12W CPU (p/n: 1970005854T001)
  - 1 x Heatsink for 6W CPU (p/n: 1960064228T021)
- 1 x Startup Manual (p/n: 2046515400)

If any of these items are missing or damaged, contact your distributor or sales representative immediately.

Optional Accessories

Part No.	Description
TBU	CPU Heat spreader for MIO-5154

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Chapter 1

General Information

This chapter gives background information on the MIO-5154.

Sections include:

- Introduction
- Specifications
- Block Diagram

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1.1 Introduction

MIO-5154 is very similar to the 3.5" SBC form factor (compact series, 146 x 102 mm) and is powered by Intel® Core™ i3-N305 and Intel® Processor N-Series processors. MIO-5154 offers embedded iManager 3.0, SUSI 4.0, and WISE-DeviceOn created by Advantech to monitor and control system operation effectively and remotely.

MIO-5154 supports single-channel DDR5-4800 up to 16GB, three independent displays via LVDS, DP 1.4, and HDMI 2.0 up to 4K@60Hz, Dual GbE, 6 x USB, 6 x UART, and TPM 2.0.

1.2 Specifications

Table 1.1: Specifications

Platform	**Processor**	i3-N305	N97	N50
	Max. Frequency	3.80 GHz	3.60 GHz	3.40 GHz
	Base Frequency	TBU	TBU	TBU
	Core/Thread	8/8	4/4	2/2
	LLC	6MB	6MB	6MB
	CPU TDP	15W	12W	6W
	Chipset	Intel® 300 Series Chipset (SoC Integrated)		
	BIOS	AMI EFI 256 Mbit		
Memory	**Technology**	DDR5-4800		
	Max. Capacity	Up to 16GB		
	Channel/Socket	Single Channel / One Socket		
	ECC Support	No	No	No
Graphics	**Controller**	Intel® UHD Graphics		
	Max. Frequency	1.25 GHz	1.20 GHz	750 MHz
	Execution Unit	32	24	16
	3D/HW Acceleration	DX12, OGL4.0, OCL1.2, HW Encode: HEVC/H265, AVC/H264, VP9, HW Decode: HEVC/H265, AVC/H264, VP9		
Display I/F	**LCD**	1 x LVDS, Dual Channel 18/24-bit, up to 1920 x 1080		
	HDMI/DP	1 x HDMI 2.0, up to 4096 x 2160 x 24bpp@48-60Hz 1 x DP1.4a, up to 4096 x 2304 x 36bpp@60Hz		
	Triple Display	3 simultaneous displays via LVDS + HDMI + DP		
Ethernet	**Controller**	LAN: Realtek RTL8111K		
	Speed	2 x GbE		
External I/O	**Ethernet**	2 x RJ-45		
	VGA/HDMI/DP	-/1/1		
	USB 3.2 / USB 2.0	2/2		

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Table 1.1: Specifications				
Internal I/O	**SATA**	1 x SATA Gen III, 6.0 Gbps		
	USB 3.0	2		
	Serial Bus	I2C (Optional to SMBus)		
	COM Port	2 x RS-232/422/485, 4 x RS-232		
	GPIO	8-bit general purpose input output I/O		
	Audio	Realtek ALC888s, Line-in/Line-out/Mic		
	Inverter	5V @2A		
	Smart Fan	12V, 2A (4-wire)		
	Front Panel Control	Power-on, Reset, Buzzer, SATA LED, Power LED, Case Open		
Board Features	**Watchdog Timer**	65536 levels, 0~65535 sec		
	TPM	fTPM supported by Intel® Platform Trust Technology Discrete TPM 2.0 (*optional)		
	iManager 3.0	SW API for Hardware Monitor, Smart Fan Control, Brightness Control, I2C, GPIO, WDT		
Expansion	**M.2 E-Key**	1 x E-Key 2230 (PCIe x1, USB 2.0)		
	M.2 B-Key	1 x B-Key 2280 (SATA or PCIe x1) 1 x B-Key 3052 (USB 3.2, USB 2.0 or *optional PCIe x1) w/ Nano-SIM		
Power	**Supply Voltage**	Vin: DC 12V +/- 10%; RTC Battery: Lithium 3V/ 210mAH, support w/o CMOS Battery		
	Connector	ATX 2-pin 180D, optional ATX 2-pin 90D or DC Jack		
	Power Management	AT, ATX		
	Max. Consumption	30.57W (12V)	27.88W(12V)	18.65W (12V)
	Idle Consumption	9.93W (12V)	20.71W(12V)	13.26W (12V)
Environment	**Temperature**	Operating: Standard: 0 ~ 60°C (32 ~ 140°F)		
		Storage: -40 ~ 85°C (-40 ~ 185°F)		
	Humidity	Operating: 40°C @ 95% relative humidity, non-condensing		
		Storage: 60°C @ 95%relative humidity, non-condensing		
	Vibration Resistance	3.5 Grms		
Certification	**EMC**	CE, FCC Class B, ESD 8KV/15KV Criteria A		
Mechanical	**Dimensions**	146 x 102 mm (5.7" x 4")		
	Net Weight	145 g		

*Note: Support by request

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1.3 Block Diagram

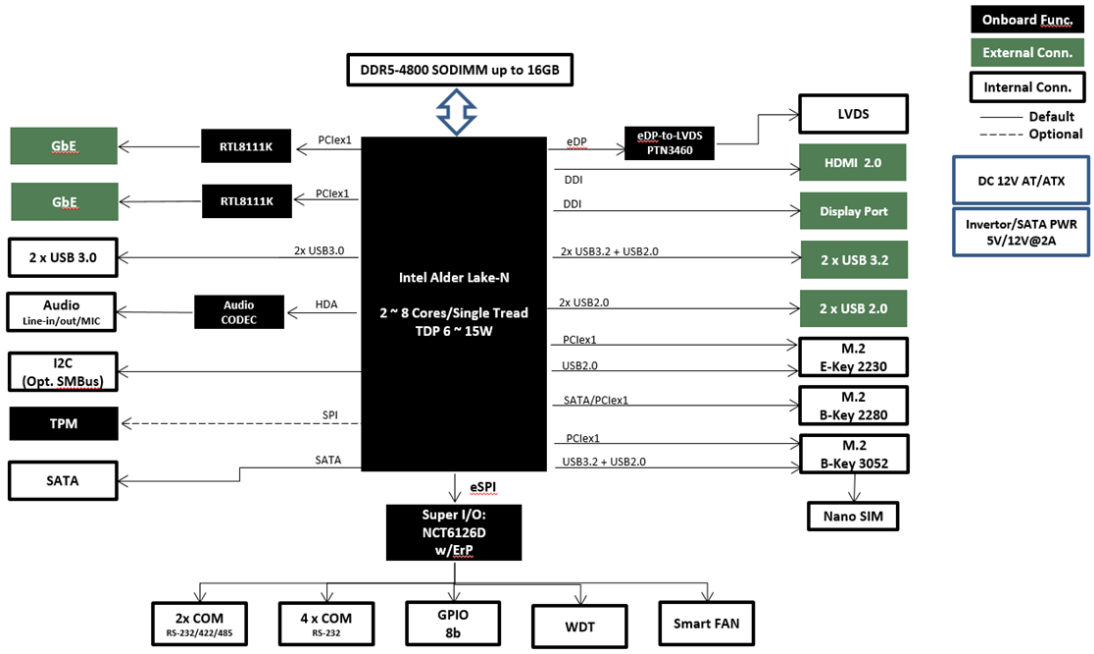

Figure 1.1 Block Diagram

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Chapter 2

Mechanical

This chapter gives mechanical information on the MIO-5154. Sections include:

- Mechanical Drawing
- Assembly Drawing

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This chapter includes board dimensions and the standard thermal solution.

2.1 Board Layout: Dimensions

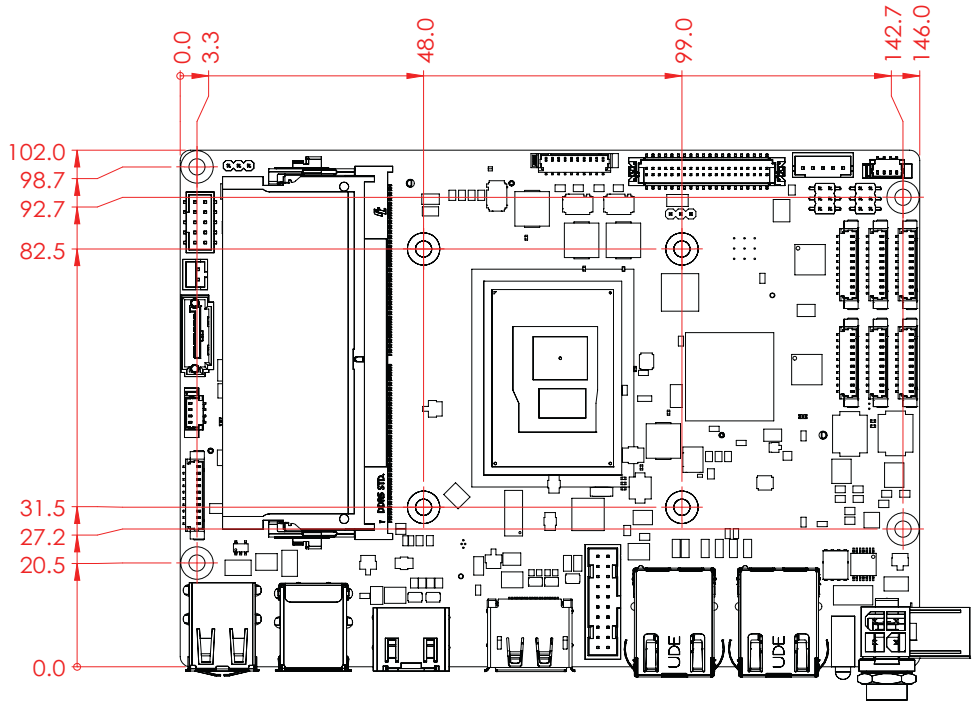

Figure 2.1 MIO-5154 Mechanical Drawing (Top Side)

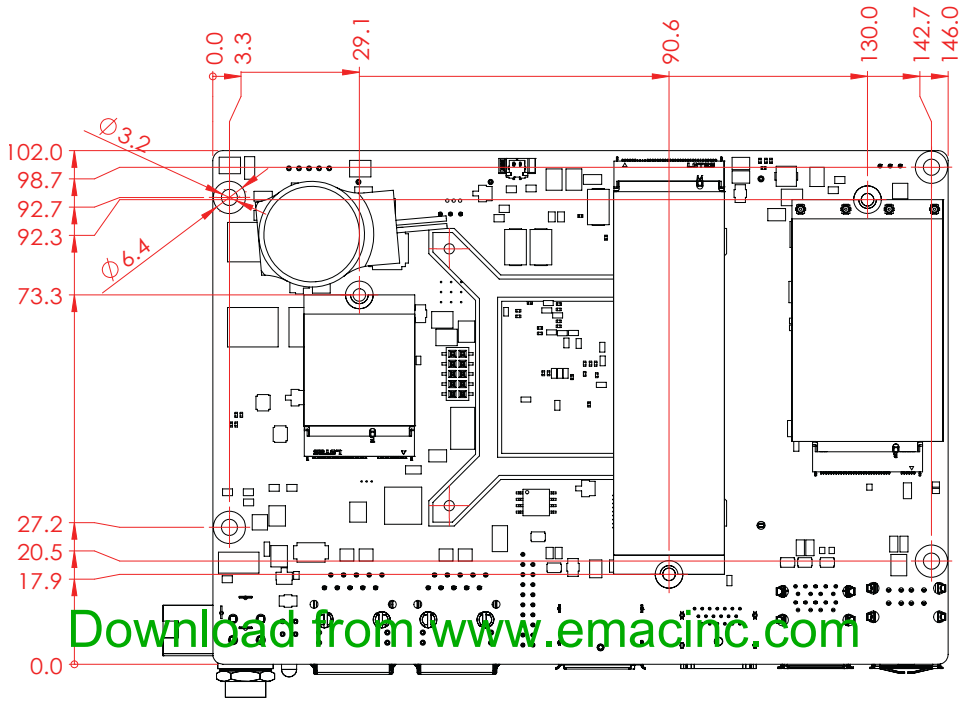

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Figure 2.2 MIO-5154 Mechanical Drawing (Bottom Side)

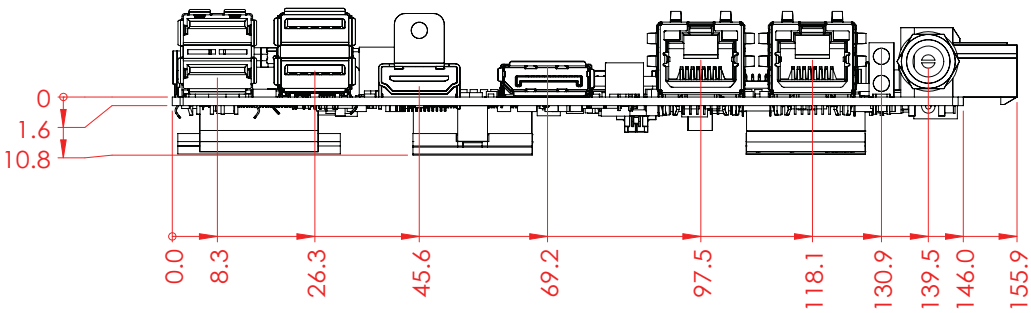

Figure 2.3 MIO-5154 Mechanical Drawing (Coastline)

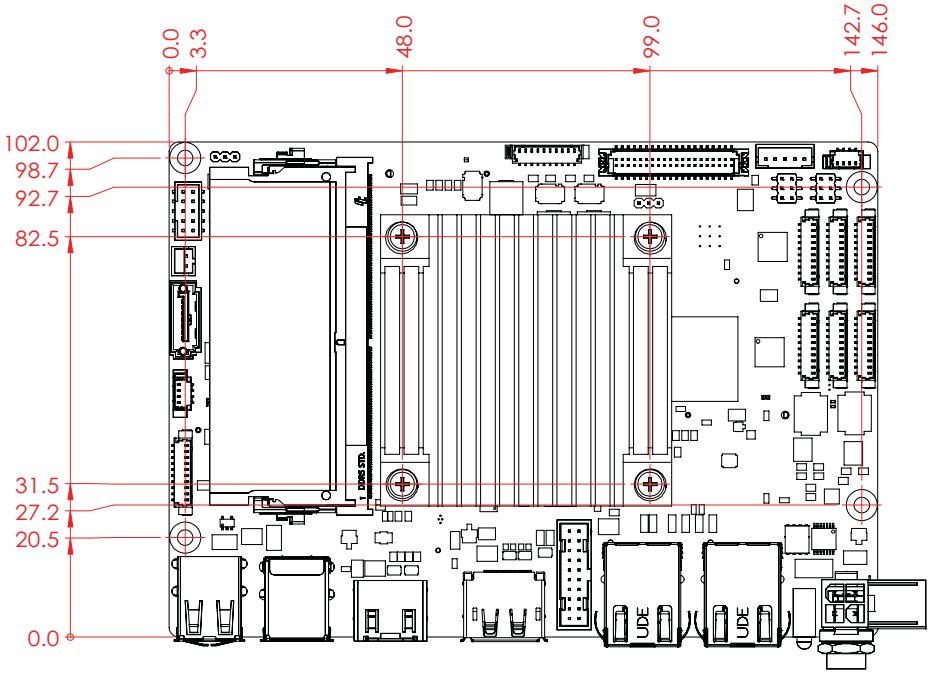

Figure 2.4 MIO-5154 Mechanical Drawing with CPU Heatsink (Top Side)

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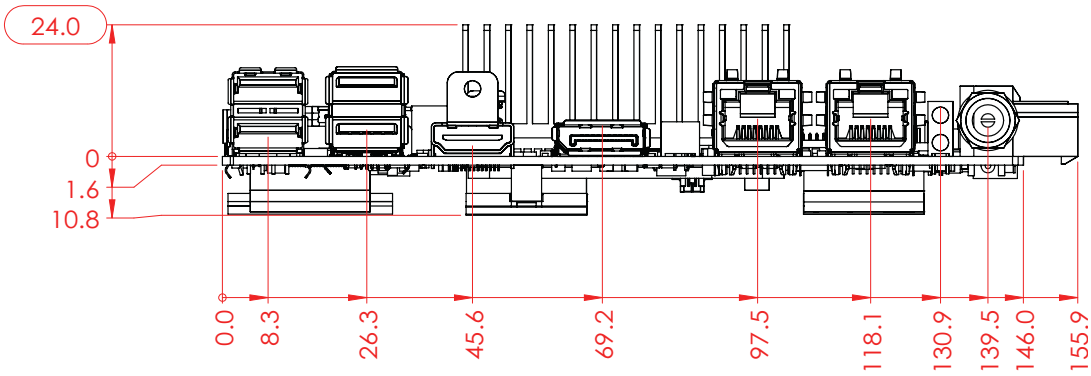

Figure 2.5 MIO-5154 Mechanical Drawing with 15W/12W CPU Heatsink (Coastline)

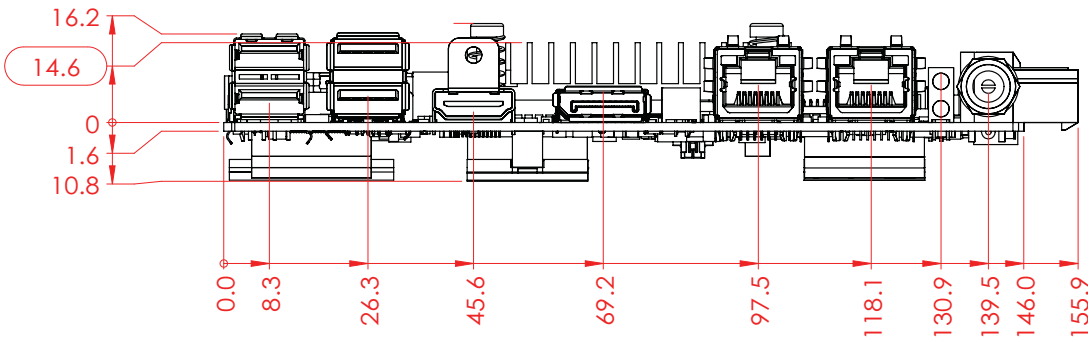

Figure 2.6 MIO-5154 Mechanical Drawing with 6W CPU Heatsink (Coastline)

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Chapter 3

Installation

This chapter explains the setup procedures of the MIO-5154 hardware, including instructions on setting jumpers and connecting peripherals, switches, and indicators. Be sure to read all safety precautions before you begin the installation procedure.

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3.1 Jumpers & Switches

The MIO-5154 has a number of jumpers that allow you to configure your system to suit your application. The table below lists the functions of the various jumpers.

Table 3.1: Jumpers & Switches	
JCMOS1	CMOS Clear Switch
VDD1	Panel Voltage Selection
RI_VDD1	COM RI# pin 5V/12V Selection
AT_ATX1	ATX/AT Mode Selection

3.2 Connectors

Onboard connectors link the MIO-5154 to external devices such as hard disk drives and a keyboard. The table below lists the function of each of the board's connectors.

Table 3.2: Connector and Header List	
Description	**Location Name**
DC Input Connector	DCIN2
DC Input Connector (Adapter)	DCIN1
Internal USB3.1 Gen1 Connector	USB1
COM Port Connector (RS232+RS422+RS485)	COM1
COM Port Connector (RS232+RS422+RS485)	COM2
COM Port Connector (RS232 only)	COM3
COM Port Connector (RS232 only)	COM4
COM Port Connector (RS232 only)	COM5
COM Port Connector (RS232 only)	COM6
Audio Connector	AUDIO1
LVDS Connector	LVDS1
SMB Bus Connector	I2C_SMB1
FAN Connector	FAN1
SATA Power Connector	SATAP1
Inverter Connector	BL1
GPIO Connector	GPIO1
Power / LED / Case Open / Buzzer Connector	FP1
M.2 B-Key (PCIe x1 / USB 2.0)	M2_B1
M.2 B-Key (SATA / PCIe x1)	M2_B2
M.2 E-Key (PCIe x1 / USB 2.0)	M2_E1
RTC Battery Connector	BAT1
Nano SIM Connector	SIM1

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3.3 Locating Connectors

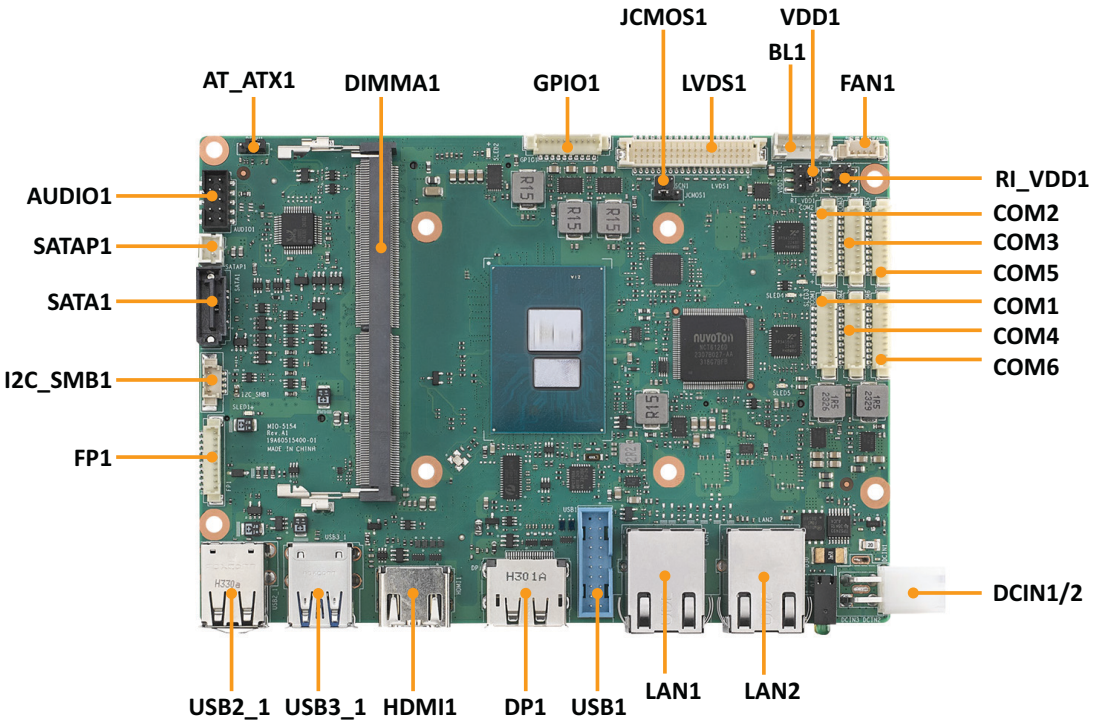

Figure 3.1 MIO-5154 Connector Locations (Top Side)

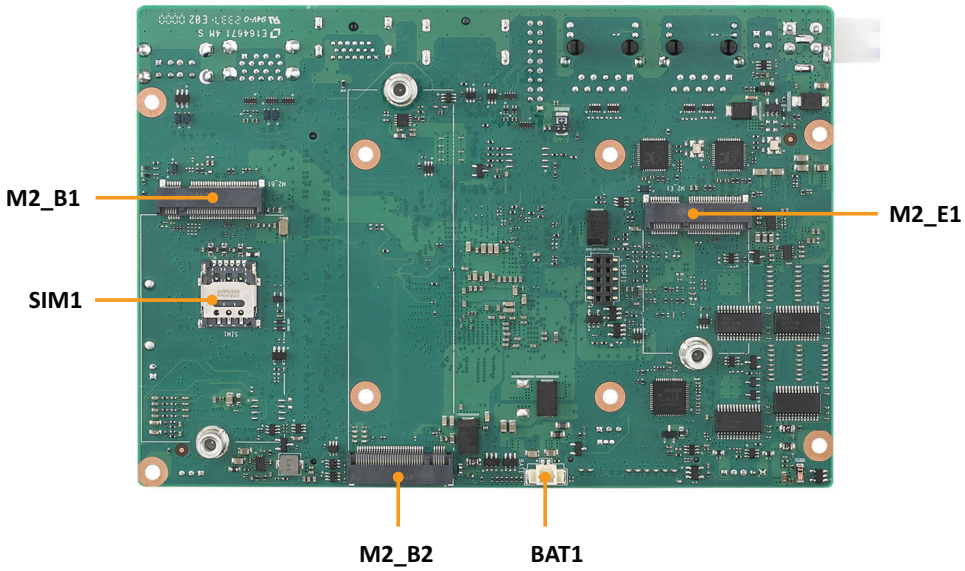

Figure 3.2 MIO-5154 Connector Locations (Bottom Side)

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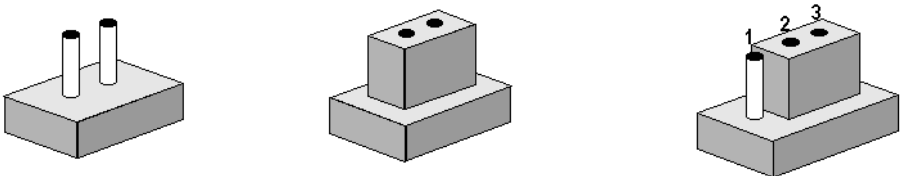
3.4 Setting Jumpers

You may configure your card to match the needs of your application by setting jumpers. A jumper is a metal bridge used to close an electric circuit. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper, you connect the pins with the clip. To “open” a jumper, you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2, and 3. In this case you would connect either pins 1 and 2, or 2 and 3.

The jumper settings are schematically depicted in this manual as follows:

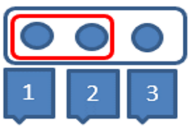
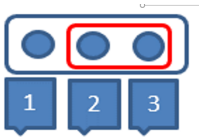


open closed closed 2-3

A pair of needle-nose pliers may be helpful when working with jumpers. If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes. Generally, you simply need a standard cable to make most connections.

3.4.1 CMOS Clear Switch (JCMOS1)

Table 3.3: CMOS Clear Switch

Function	Jumper Setting
Keep COMS Data (Default)	
Load CMOS Date	

Pin	Signal Pin Definition
1	NC
2	FAILSAFE_BIOS
3	GND

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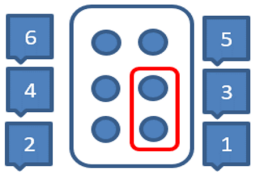
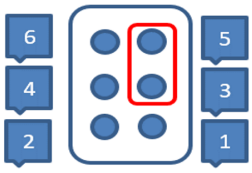
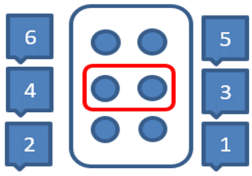
3.4.2 Panel Voltage Selection (VDD1)

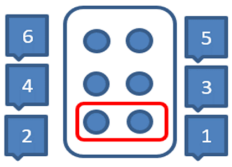
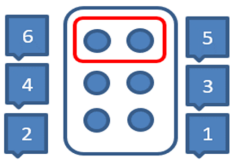
Table 3.4: Panel Voltage Selection

Function	Jumper Setting
Panel Voltage Setting: +V3.3 (Default)	
Panel Voltage Setting: +V5	
Panel Voltage Setting: +V12	

Pin	Signal Pin Definition
1	+V3.3
2	NC
3	+V_LVDS_LCD
4	+V12
5	+V5
6	NC

3.4.3 COM RI# pin 5V/12V Selection (RI_VDD1)

Table 3.5: COM RI# pin 5V/12V Selection

Function	Jumper Setting
RI# Voltage Setting: +V5	
RI# Voltage Setting: +V12	
RI# Voltage Setting: RI# (Default)	

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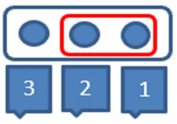
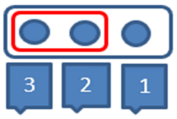
Pin	Signal Pin Definition
1	VCCAT
2	PU to 3.3V suspend
3	VCCATX

3.4.4 ATX/AT Mode Selection

Table 3.6: ATX/AT Mode Selection

Function	Jumper Setting
BIOS setting to AT mode (Default)	
BIOS setting to ATX mode	

Pin	Signal Pin Definition
1	VCCAT
2	PU to 3.3V suspend
3	VCCATX

3.4.5 DC Input Connector

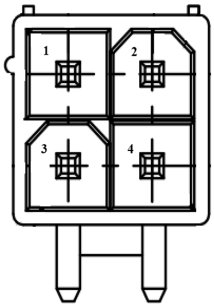


Table 3.7: DC Input Connector

Pin	Signal Pin Definition
1	GND
2	GND
3	+V12_DC_IN
4	+V12_DC_IN

3.4.6 DC Input Connector (Adapter)

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Table 3.8: DC Input Connector (Adapter)

Pin	Signal Pin Definition
1	+V12_DC_IN
2	GND
3	NCN49400609

3.4.7 Internal USB 3.1 Gen1 Connector

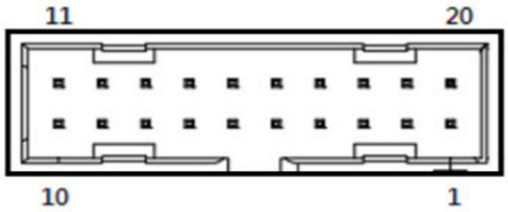

Table 3.9: Internal USB 3.1 Gen1 Connector

Pin	Signal Pin Definition
1	Vbus
2	IntA_P1_SSRX-
3	IntA_P1_SSRX+
4	GND
5	IntA_P1_SSTX-
6	IntA_P1_SSTX+
7	GND
8	IntA_P1_D-
9	IntA_P1_D+
10	NC
11	IntA_P2_D+
12	IntA_P2_D-
13	GND
14	IntA_P2_SSTX+
15	IntA_P2_SSTX-
16	GND
17	IntA_P2_SSRX+
18	IntA_P2_SSRX-
19	Vbus
20	No Pin

3.4.8 COM Port Connector (RS232+RS422+RS485)

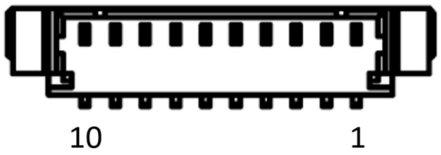

Table 3.10: COM Port Connector (RS232+RS422+RS485)

Pin	Signal Pin Definition
1	NC
2	COM1_z_RI#
3	COM1_DTR#
4	COM1_CTS#
5	COM1_TXD
6	COM1_RTS#
7	COM1_RXD
8	COM1_DSR#

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Table 3.10: COM Port Connector (RS232+RS422+RS485)	
9	COM1_DCD#
10	GND

3.4.9 COM Port Connector (RS232+RS422+RS485)

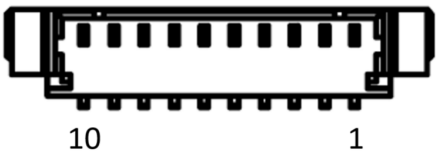

Table 3.11: COM Port Connector (RS232+RS422+RS485)	
Pin	**Signal Pin Definition**
1	NC
2	COM2_RI#
3	COM2_DTR#
4	COM2_CTS#
5	COM2_TXD
6	COM2_RTS#
7	COM2_RXD
8	COM2_DSR#
9	COM2_DCD#
10	GND

3.4.10 COM Port Connector (RS232)

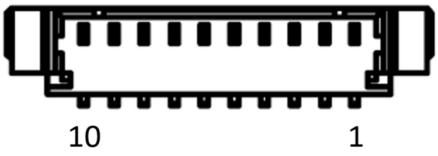

Table 3.12: COM Port Connector (RS232)	
Pin	**Signal Pin Definition**
1	NC
2	COM3_RI#
3	COM3_DTR#
4	COM3_CTS#
5	COM3_SOUT
6	COM3_RTS#
7	COM3_SIN
8	COM3_DSR#
9	COM3_DCD#
10	GND

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3.4.11 COM Port Connector (RS232)

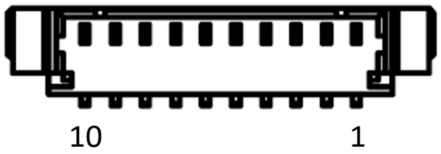

Table 3.13: COM Port Connector (RS232)	
Pin	**Signal Pin Definition**
1	NC
2	COM4_RI#
3	COM4_DTR#
4	COM4_CTS#
5	COM4_SOUT
6	COM4_RTS#
7	COM4_SIN
8	COM4_DSR#
9	COM4_DCD#
10	GND

3.4.12 COM Port Connector (RS232)

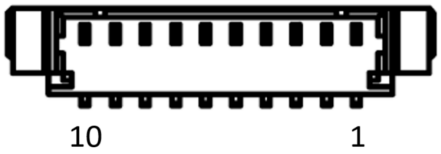

Table 3.14: COM Port Connector (RS232)	
Pin	**Signal Pin Definition**
1	NC
2	COM5_RI#
3	COM5_DTR#
4	COM5_CTS#
5	COM5_SOUT
6	COM5_RTS#
7	COM5_SIN
8	COM5_DSR#
9	COM5_DCD#
10	GND

3.4.13 COM Port Connector (RS232)

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Table 3.15: COM Port Connector (RS232)	
Pin	**Signal Pin Definition**
1	NC
2	COM6_RI#
3	COM6_DTR#
4	COM6_CTS#
5	COM6_SOUT
6	COM6_RTS#
7	COM6_SIN
8	COM6_DSR#
9	COM6_DCD#
10	GND

3.4.14 Audio Connector

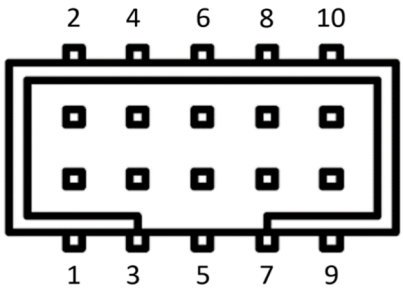

Table 3.16: Audio Connector	
Pin	**Signal Pin Definition**
1	LOUTR
2	LINR
3	GND
4	GND
5	LOUTL
6	LINL
7	GND
8	NC
9	MIC1R
10	MIC1L

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3.4.15 LVDS Connector

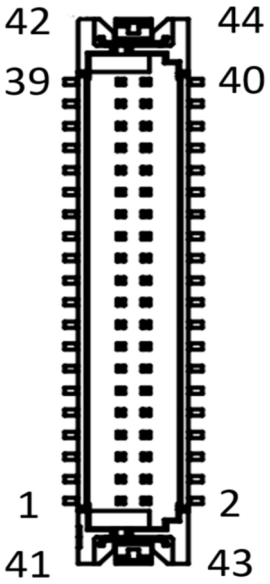

Table 3.17: LVDS Connector

Pin	Signal Pin Definition
1	+V_LCD
2	+V_LCD
3	GND
4	GND
5	+V_LCD
6	+V_LCD
7	LVDS1_0_D0-
8	LVDS1_1_D0-
9	LVDS1_0_D0+
10	LVDS1_1_D0+
11	GND
12	GND
13	LVDS1_0_D1-
14	LVDS1_1_D1-
15	LVDS1_0_D1+
16	LVDS1_1_D1+
17	GND
18	GND
19	LVDS1_0_D2-
20	LVDS1_1_D2-
21	LVDS1_0_D2+
22	LVDS1_1_D2+
23	GND
24	GND
25	LVDS1_0_CLK-
26	LVDS1_1_CLK-
27	LVDS1_0_CLK+

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Table 3.17: LVDS Connector	
28	LVDS1_1_CLK+
29	GND
30	GND
31	LVDS0_DDCCLK_AUX+
32	LVDS0_DDCDAT_AUX-
33	GND
34	GND
35	LVDS1_0_D3-
36	LVDS1_1_D3-
37	LVDS1_0_D3+
38	LVDS1_1_D3+
39	NC
40	LVDS1_VCON

3.4.16 SMB Connector

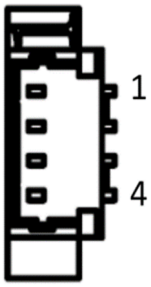

Table 3.18: SMB Connector	
Pin	**Signal Pin Definition**
1	GND
2	EC_SMB0_z_DAT
3	EC_SMB0_z_CLK
4	+V3.3_DUAL

3.4.17 Fan Connector

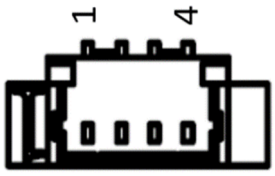

Table 3.19: Fan Connector	
Pin	**Signal Pin Definition**
1	GND
2	+V12
3	FAN_SPEED
4	FAN_V5_PWM

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3.4.18 SATA Power Connector

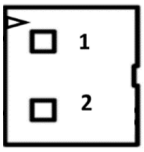

Table 3.20: SATA Power Connector	
Pin	**Signal Pin Definition**
1	5V
2	GND

3.4.19 Panel Inverter Connector

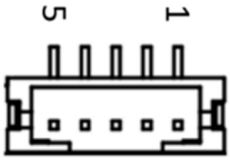

Table 3.21: Panel Inverter Connector	
Pin	**Signal Pin Definition**
1	+V12_1_INVERTER_0
2	GND
3	LVDS1_Z_ENABKL
4	EC_LVDS1_Z_PWM
5	+V5_1_INVERTER_0

3.4.20 GPIO Connector

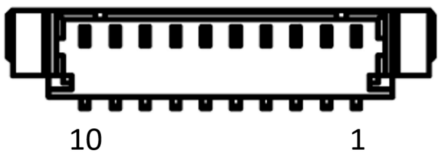

Table 3.22: GPIO Connector	
Pin	**Signal Pin Definition**
1	GND
2	SIO_GPIO7
3	SIO_GPIO2
4	SIO_GPIO6
5	SIO_GPIO1
6	SIO_GPIO5
7	SIO_GPIO0
8	SIO_GPIO4
9	+V5A_GPIO
10	SIO_GPIO3

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3.4.21 Power / LED / Case Open / Buzzer Connector

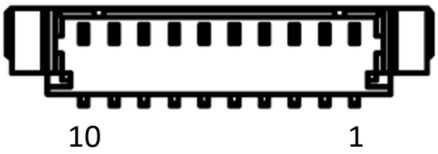

Table 3.23: Power / LED / Case Open / Buzzer Connector	
Pin	**Signal Pin Definition**
1	GND
2	BUZZER-
3	BUZZER+
4	RDC_CASEOPEN
5	SATA_EXT_LED#
6	FP_A_PSIN#
7	FP_A_RST#
8	+3.3V
9	NC
10	+5V

3.4.22 M.2 B-Key (PCIe x1 / USB 2.0)

Table 3.24: M.2 B-Key (PCIe x1 / USB 2.0)			
Pin	**Signal Pin Definition**	**Pin**	**Signal Pin Definition**
74	3.3V (Suspend)	75	CONFIG_2 (Pull up 10K to 3.3V)
72	3.3V (Suspend)	73	GND
70	3.3V (Suspend)	71	GND
68	SUSCLK (3.3V)	69	CONFIG_1 (Pull up 10K to 3.3V)
66	NC	67	RESET# (1.8V)
64	NC	65	NC
62	NC	63	NC
60	NC	61	NC
58	NC	59	NC
56	NC	57	GND
54	PEWAKE# (3.3V)	55	REFCLKp
52	CLKREQ# (3.3V)	53	REFCLKn
50	PERST# (3.3V)	51	GND
48	NC	49	PERp0
46	NC	47	PERn0
44	NC	45	GND
42	NC	43	PETp0

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Table 3.24: M.2 B-Key (PCIe x1 / USB 2.0)			
40	NC	41	PETn0
38	NC	39	GND
36	UIM_PWR	37	USB3.1-Rx+
34	UIM_DATA	35	USB3.1-Rx-
32	UIM_CLK	33	GND
30	UIM_RESET	31	USB3.1-Tx+
28	NC	29	USB3.1-Tx-
26	NC	27	GND
24	NC	25	NC
22	NC	23	NC
20	NC	21	CONFIG_0 (Pull up 10K to 3.3V)
29	NC	29	NC
30	M2B1_SATA_DEVSLP_R	30	M2B1_SATA_DEVSLP_R
31	GND	31	GND
32	NC	32	NC
10	LED_1# (3.3V)	11	GND
8	W_DISABLE1# (3.3V)	9	USB_D-
6	FULL_CARD_POW-ER_OFF# (1.8V)	7	USB_D+
4	3.3V (Suspend)	5	GND
2	3.3V (Suspend)	3	GND
		1	CONFIG_3 (Pull up 10K to 3.3V)

3.4.23 M.2 B-Key (SATA / PCIe x1)

Table 3.25: M.2 B-Key (SATA / PCIe x1)			
Pin	**Signal Pin Definition**	**Pin**	**Signal Pin Definition**
74	3.3V (Suspend)	75	CONFIG_2 (Pull up 10K to 3.3V)
72	3.3V (Suspend)	73	GND
70	3.3V (Suspend)	71	GND
68	SUSCLK (3.3V)	69	CONFIG_1 (Pull up 10K to 3.3V)
66	NC	67	NC
64	NC	65	NC
62	NC	63	NC
60	NC	61	NC
58	NC	59	NC
56	NC	57	GND
54	PEWAKE# (3.3V)	55	REFCLKp
52	CLKREQ# (3.3V)	53	REFCLKn
50	PERST# (3.3V)	51	GND

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Table 3.25: M.2 B-Key (SATA / PCIe x1)			
48	NC	49	PERp0 / SATA-A+
46	NC	47	PERn0 / SATA-A-
44	NC	45	GND
42	NC	43	PETp0 / SATA-B-
40	NC	41	PETn0 / SATA-B+
38	NC	39	GND
36	NC	37	NC
34	NC	35	NC
32	NC	33	GND
30	NC	31	NC
28	NC	29	NC
26	NC	27	GND
24	NC	25	NC
22	NC	23	NC
20	NC	21	CONFIG_0 (Pull up 10K to 3.3V)
29	NC	29	NC
30	M2B1_SATA_DEVSLP_R	30	M2B1_SATA_DEVSLP_R
31	GND	31	GND
32	NC	32	NC
10	LED_1# (3.3V)	11	GND
8	W_DISABLE1# (3.3V)	9	NC
6	FULL_CARD_POW-ER_OFF# (1.8V)	7	NC
4	3.3V (Suspend)	5	GND
2	3.3V (Suspend)	3	GND
		1	CONFIG_3 (Pull up 10K to 3.3V)

3.4.24 M.2 E-Key (PCIe x1 / USB 2.0)

Table 3.26: M.2 E-Key (PCIe x1 / USB 2.0)			
Pin	**Signal Pin Definition**	**Pin**	**Signal Pin Definition**
74	3.3V (Suspend)	75	GND
72	3.3V (Suspend)	73	NC
70	NC	71	NC
68	NC	69	GND
66	NC	67	NC
64	NC	65	NC
62	NC	63	GND
60	NC	61	NC
58	NC	59	NC

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Table 3.26: M.2 E-Key (PCIe x1 / USB 2.0)			
56	W_DISABLE1# (3.3V)	57	GND
54	W_DISABLE2# (3.3V)	55	PEWAKE0# (3.3V)
52	PERST0# (3.3V)	53	CLKREQ0# (3.3V)
50	SUSCLK (3.3V)	51	GND
48	NC	49	REFCLKn0
46	NC	47	REFCLKp0
44	NC	45	GND
42	NC	43	PETn0
40	NC	41	PETp0
38	NC	39	GND
36	NC	37	PERn0
34	NC	35	PERp0
32	NC	33	GND
29	NC	29	NC
30	M2B1_SATA_DEVSLP_R	30	M2B1_SATA_DEVSLP_R
31	GND	31	GND
32	NC	32	NC
22	NC	23	NC
20	NC	21	NC
18	GND	19	NC
16	NC	17	NC
14	NC	15	NC
12	NC	13	NC
10	NC	11	NC
8	NC	9	NC
6	NC	7	GND
4	3.3V (Suspend)	5	USB_D-
2	3.3V (Suspend)	3	USB_D+
		1	GND

3.4.25 RTC Battery Connector

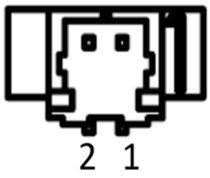

Table 3.27: RTC Battery Connector	
Pin	**Signal Pin Definition**
1	+VBAT_b1
2	GND

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3.4.26 Nano SIM Connector

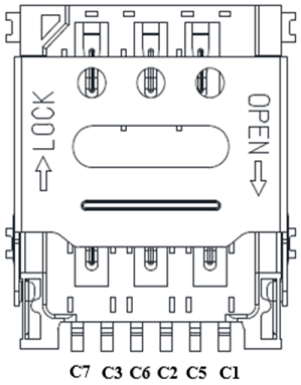

Table 3.28: Nano SIM Connector

Pin	Signal Pin Definition
C1	VCC
C2	RESET
C3	Clock
C5	GND
C6	VPP
C7	Data

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Chapter 4

AMI BIOS Setup

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AMIBIOS has been integrated into a plethora of motherboards for decades. With the AMIBIOS Setup program, you can modify BIOS settings and control various system features. This chapter describes the basic navigation of the MIO-5154 BIOS setup screens.

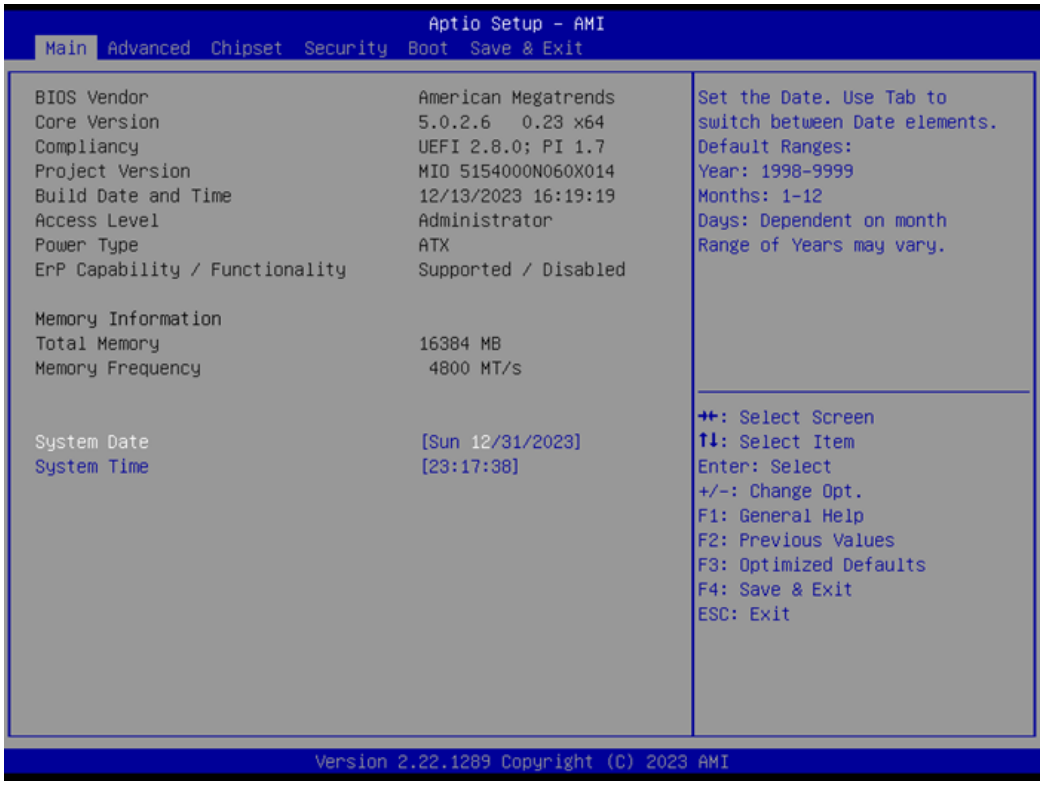

Figure 4.1

AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This information is stored in battery-backed CMOS so it retains the setup information when the power is turned off.

4.1 Entering Setup

Turn on the computer and check for the patch code. If there is a number assigned to the patch code, it means that the BIOS supports your CPU. If there is no number assigned to the patch code, please contact an Advantech application engineer to obtain an up-to-date patch code file. This will ensure that your CPU's system status is valid. After ensuring that you have a number assigned to the patch code, press <DEL> and you will immediately be allowed to enter Setup.

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4.1.1 Main Setup

When you first enter the BIOS Setup Utility, you will encounter the Main setup screen.

You can always return to the Main setup screen by selecting the Main tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.

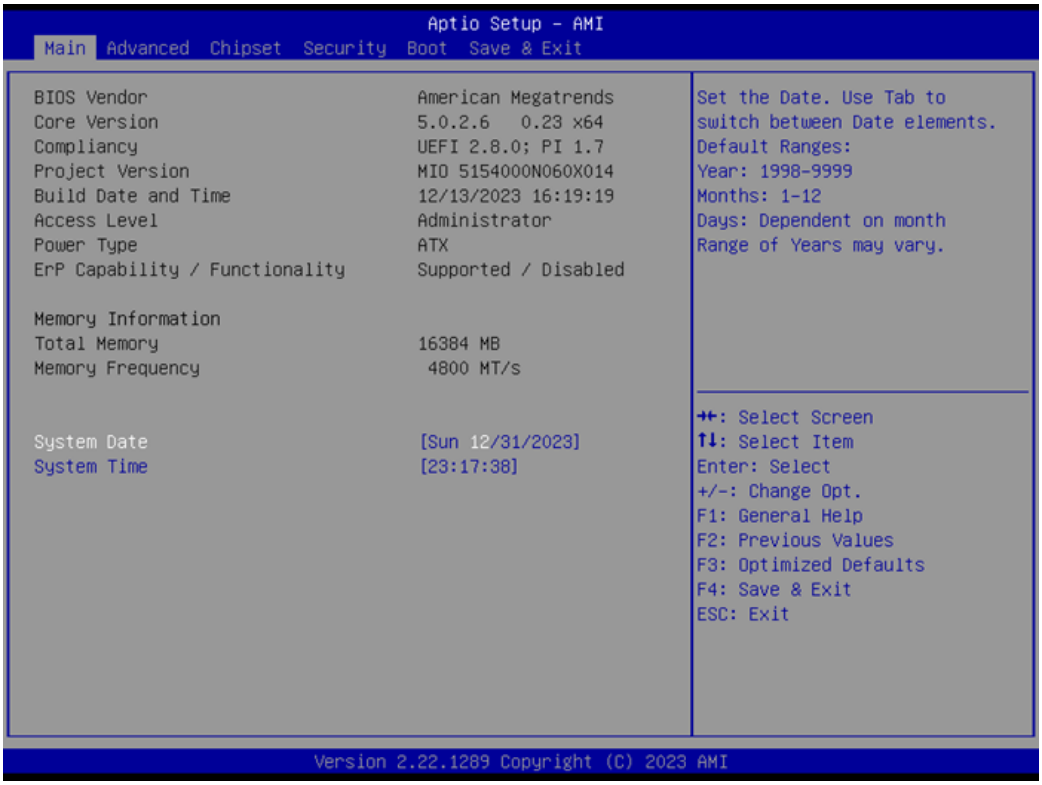

Figure 4.2

The Main BIOS setup screen has two main frames. The left frame displays all the options that can be configured. Grayed-out options cannot be configured; options in blue can. The right frame displays the key legend.

Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

- **System Time / System Date**

  Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard.

  Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time must be entered in HH:MM:SS format.

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4.1.2 Advanced BIOS Features Setup

Select the Advanced tab from the MIO-5154 setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as CPU Configuration, to go to the sub-menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screens are shown below. The sub-menus are described on the following pages.

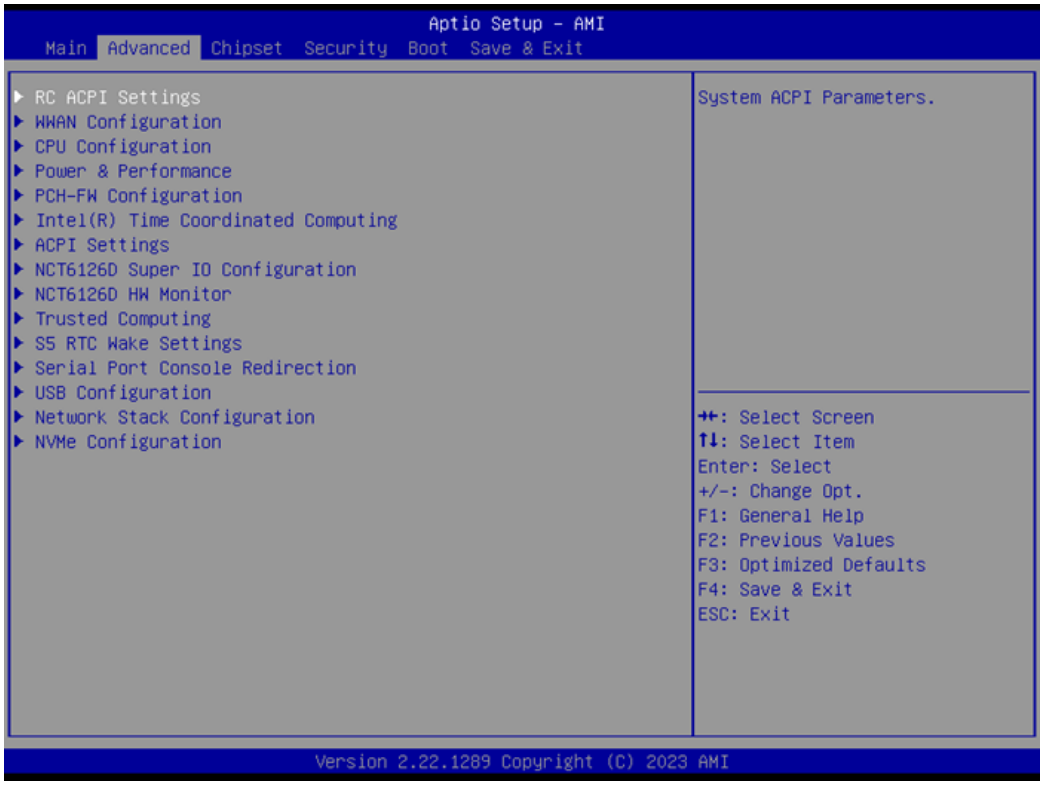

Figure 4.3

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4.1.3 RC ACPI Settings

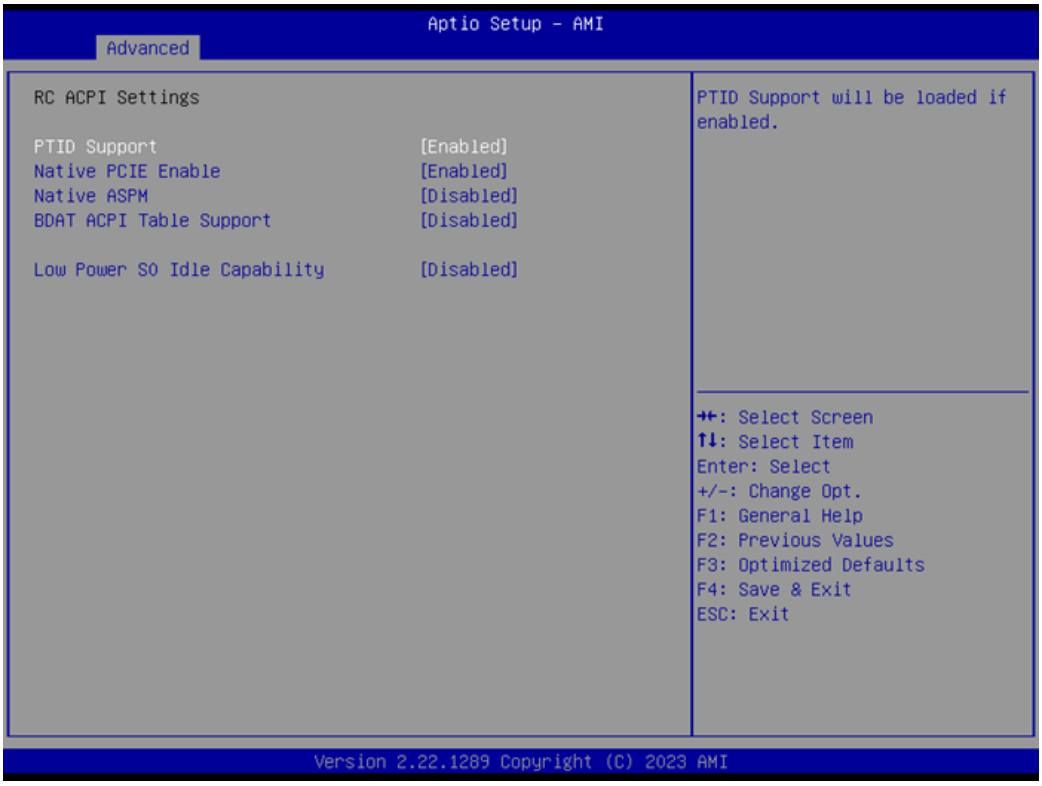

Figure 4.4

- **PTID Support**
  Enable/Disable to load the PTID Table.
- **Native PCIE Enable**
  Enable/Disable PCIE Native Control reported in the ACPI Table.
- **Native ASPM**
  Choose if the ASPM feature is controlled by the OS or BIOS.
- **BDAT ACPI Table Support**
  Enable/Disable support for the BDAT ACPI Table.
- **Low Power S0 Idle Capability**
  Enable/Disable ACPI Low Power S0 Idle Capability under the OS.

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4.1.3.1 WWAN Configuration

Figure 4.5

- **WWAN Device**
  Select the M.2 WWAN Device options to enable 5G-M80 (MediaTek) Modems.

4.1.3.2 CPU Configuration

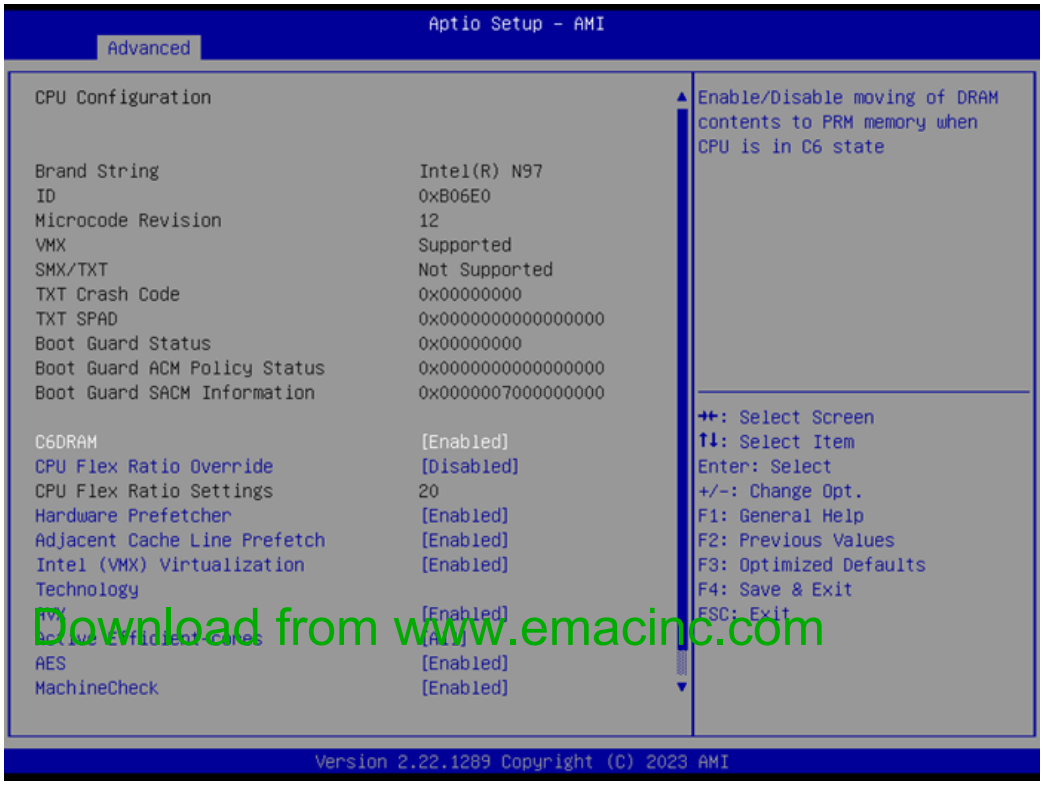

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Figure 4.6

- **C6DRAM**
  Enable/Disable moving of DRAM contents to PRM memory when the CPU is in C6 state.
- **CPU Flex Ratio Override**
  Enable/Disable CPU Flex Ratio Programming.
- **Hardware Prefetcher**
  This item allows users to enable or disable the hardware prefetcher feature.
- **Adjacent Cache Line Prefetch**
  This item allows users to enable or disable the adjacent cache line prefetch feature.
- **Intel® (VMX) Virtualization Technology**
  When Enabled, a VMM can utilize the additional hardware capability provided by Vanderpool Technology.
- **AVX**
  Enable/Disable the AVX 2/3 Instructions.
- **Active Efficient-cores**
  Number of E-cores to enable in each processor package.
- **AES**
  Enable/Disable AES (Advanced Encryption Standard).
- **MachineCheck**
  Enable/Disable Machine Check.
- **MonitorMWait**
  Enable/Disable MonitorMWait.
- **Intel® Trusted Execution Technology**
  Enables utilization of additional hardware capability provided by Intel® Trusted Execution Technology.

4.1.3.3 Power & Performance

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Figure 4.7

- **CPU – Power Management Control**
  CPU – Power Management Control Options.
- **GT – Power Management Control**
  GT – Power Management Control Options.

CPU - Power Management Control

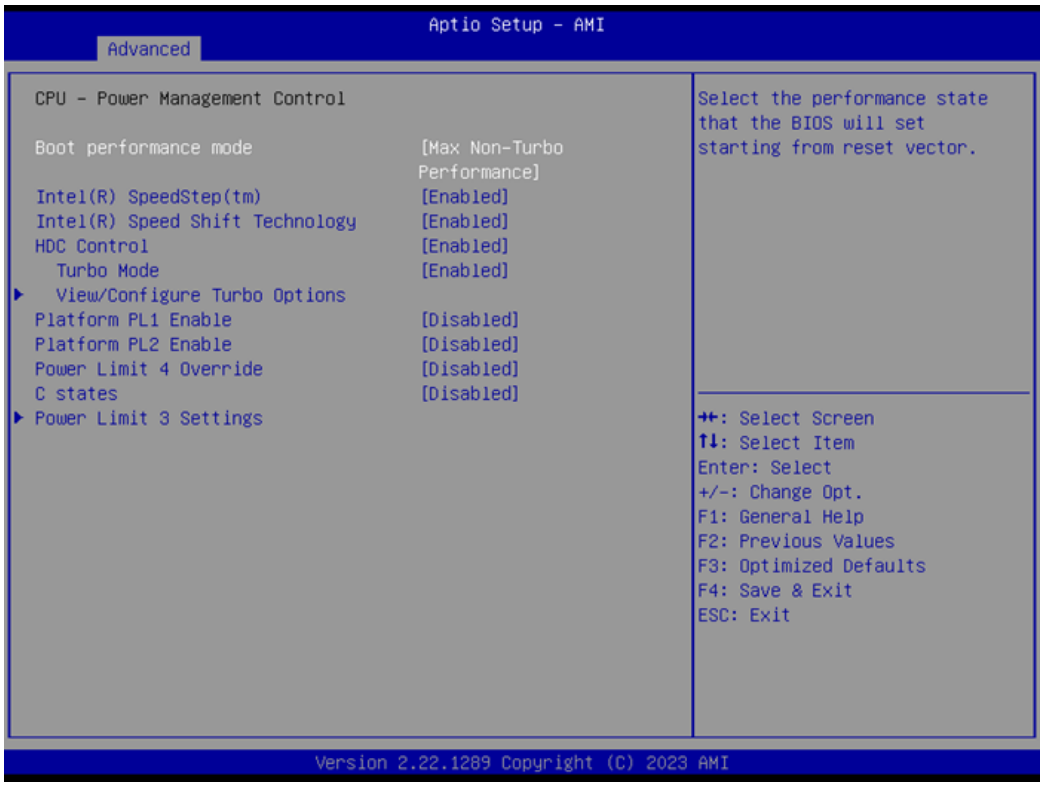

Figure 4.8

- **Boot Performance mode**
  Select the performance state that the BIOS will set before OS handoff.
- **Intel® SpeedStep™**
  Allows more than two frequency ranges to be supported.
- **Intel® Speed Shift Technology**
  Enable/Disable Intel® Speed Shift Technology support.
- **HDC Control**
  Enable/Disable Intel HDC.
- **Turbo Mode**
  Enable/Disable processor turbo mode.
- **View/Configure Turbo Options**
  View and Configure Turbo Options.
- **Platform PL1 Enable**
  Enable/Disable Platform Power Limit 1 programming.
- **Platform PL2 Enable**
  Enable/Disable Platform Power Limit 1 programming.
- **Power Limit 4 Override**
  Enable/Disable Power Limit 4 override.
- **C states**

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Enable/Disable CPU Power Management.

- **PowerLimit 3 Settings**
  Power Limit 3 Settings.

View/Configure Turbo Options

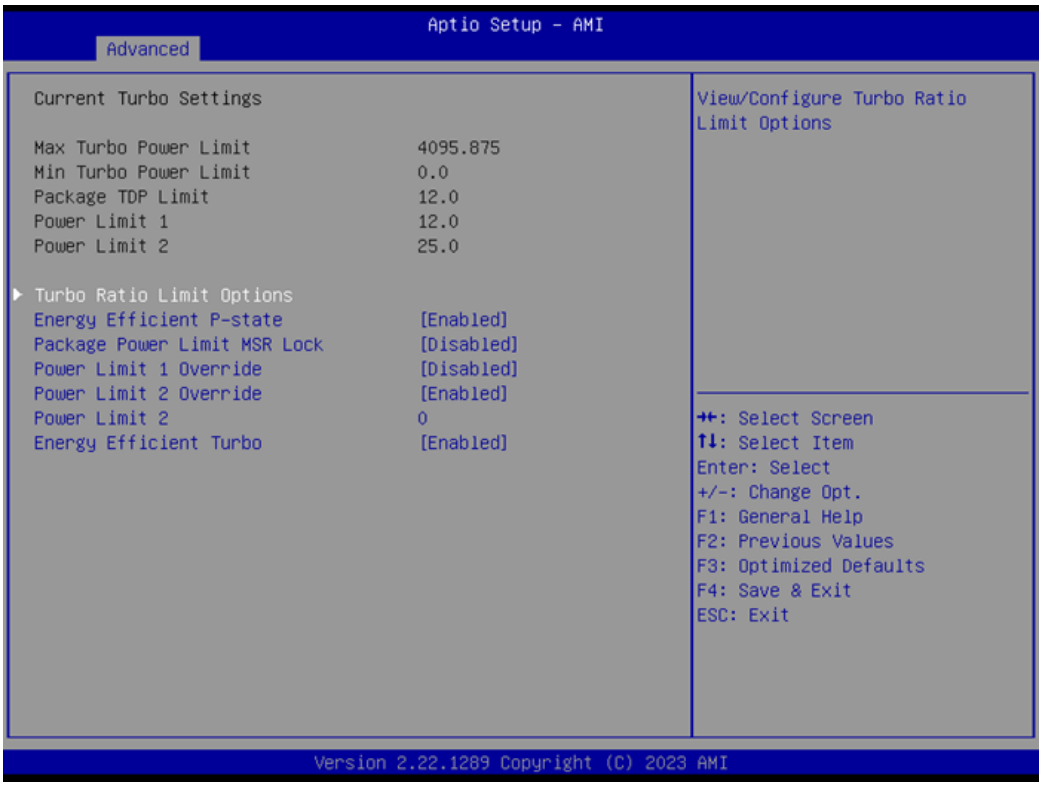

Figure 4.9

- **Turbo Ratio Limit Option**
  View/Configure Turbo Ratio Limit Options.
- **Energy Efficient P-state**
  Enable/Disable Energy Efficient P-state feature.
- **Package Power Limit MSR Lock**
  Enable/Disable locking of Package Power Limit settings.
- **Power Limit 1 Override**
  Enable/Disable Power Limit 1 override.
- **Power Limit 2 Override**
  Enable/Disable Power Limit 2 override.
- **Power Limit**
  Power Limit 2 value in milliwatts; BIOS will round to the nearest 1/8W when programming.
- **Energy Efficient Turbo**
  Enable/Disable the Energy Efficient Turbo feature.

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TDP Configurations

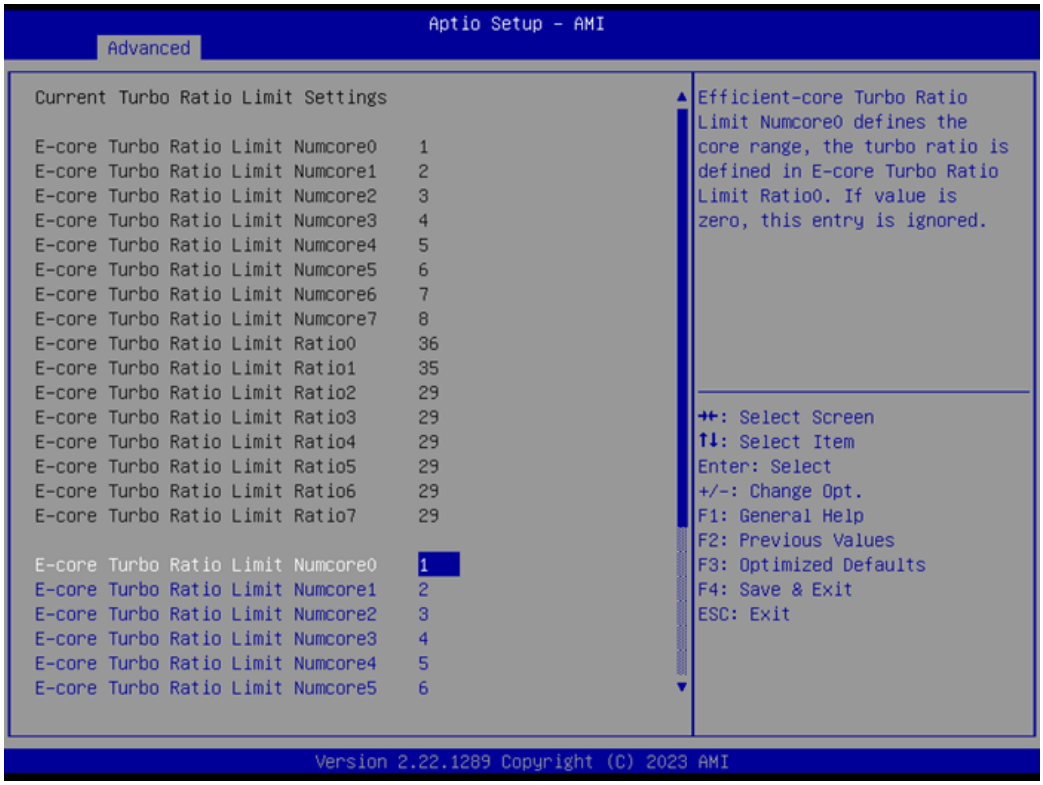

Figure 4.10

- **E-core Turbo Ratio Limit Numcore x**
  Efficient-core Turbo Ratio Limit Numcore x defines the core range.

Power Limit 3 Settings

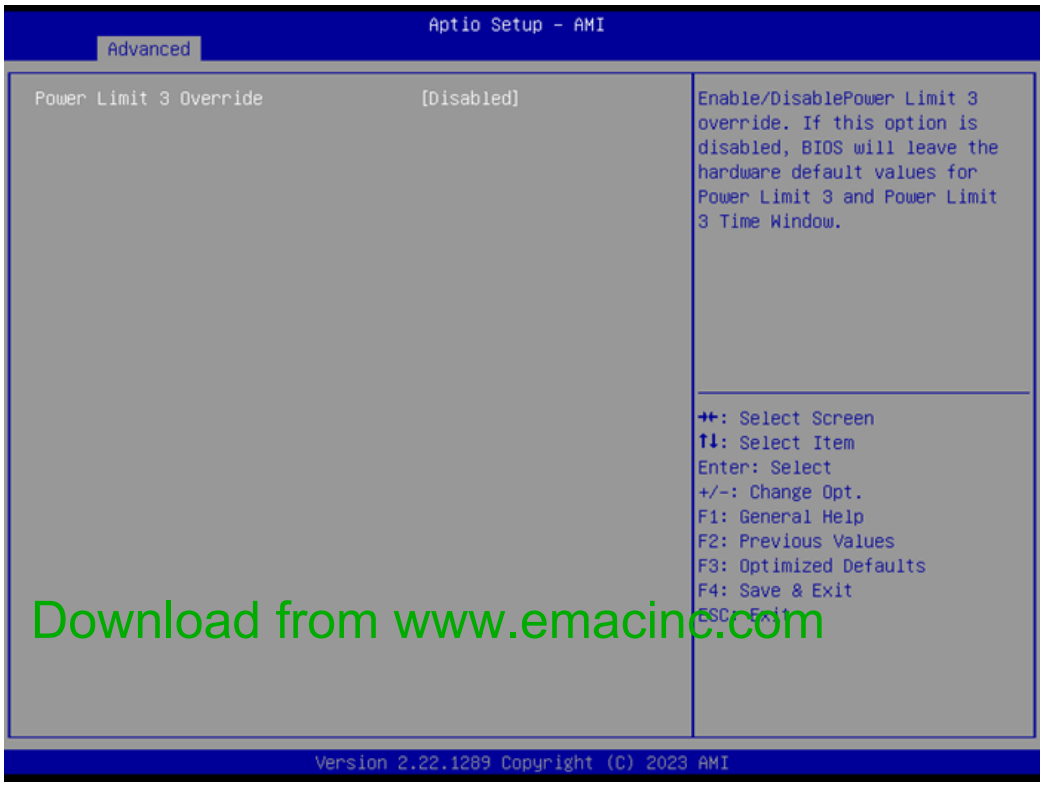

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Figure 4.11

- **Power Limit 3 Override**
  Enable/Disable Power Limit 3 override.

GT - Power Management Control

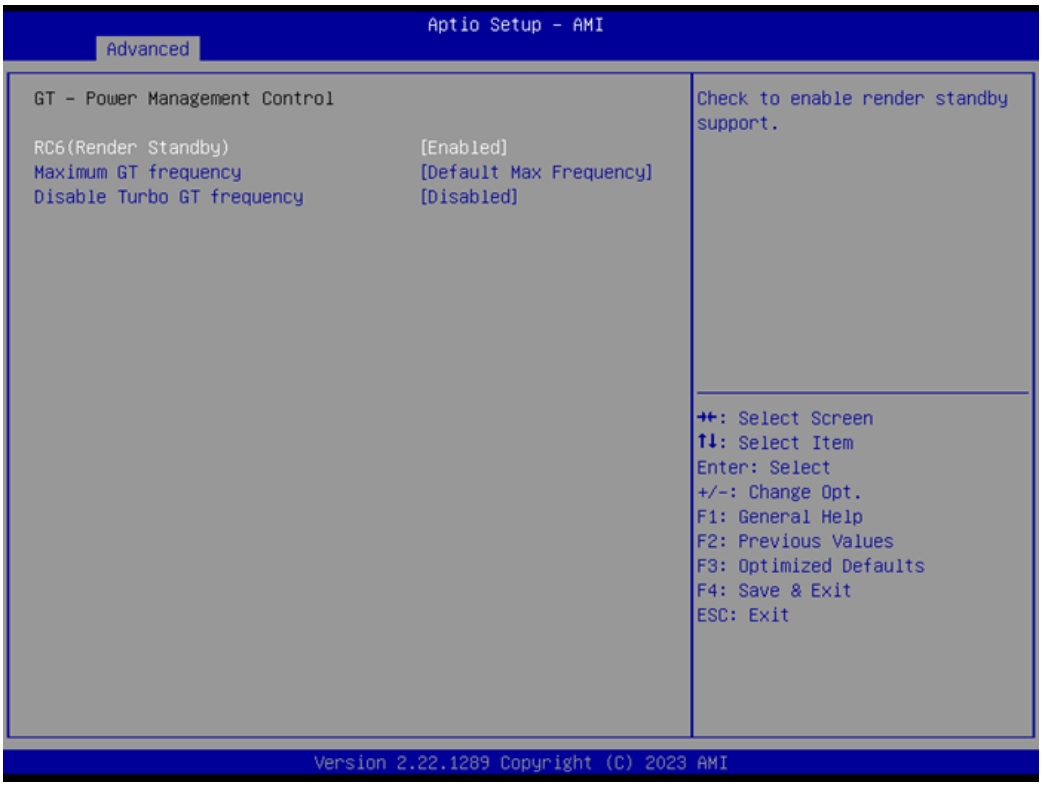

Figure 4.12

- **RC6(Render Standby)**
  Check to enable render standby support.
- **Maximum GT frequency**
  Maximum GT frequency limited by user.
- **Disable Turbo GT frequency**
  Enable/Disable Turbo GT frequency.

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4.1.3.4 PCH-FW Configuration

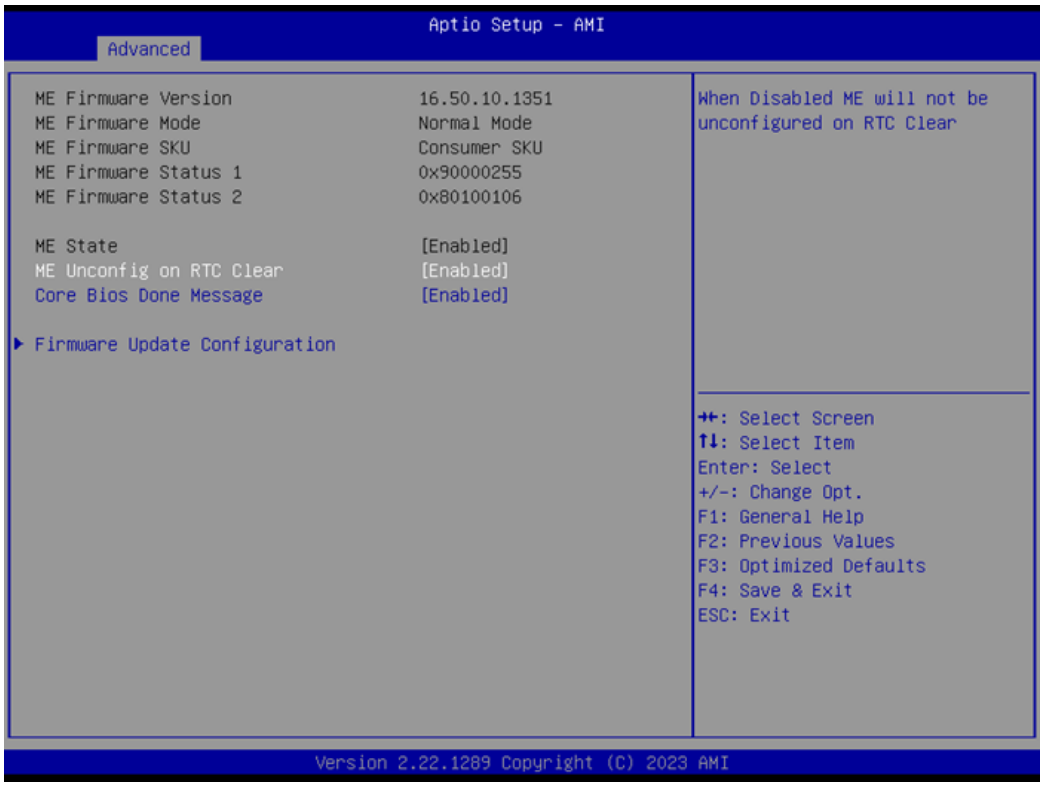

Figure 4.13

- **ME State**
  When Disabled, ME will be put ME into Temporarily Disabled Mode.
- **ME Unconfig on RTC Clear**
  When Disabled, ME will not be unconfigured on RTC Clear.
- **Core BIOS Done Message**
  Enable/Disable Core BIOS Done message sent to ME.
- **Firmware Update Configuration**
  Configure Management Engine Technology Parameters.

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4.1.3.5 ACPI Settings

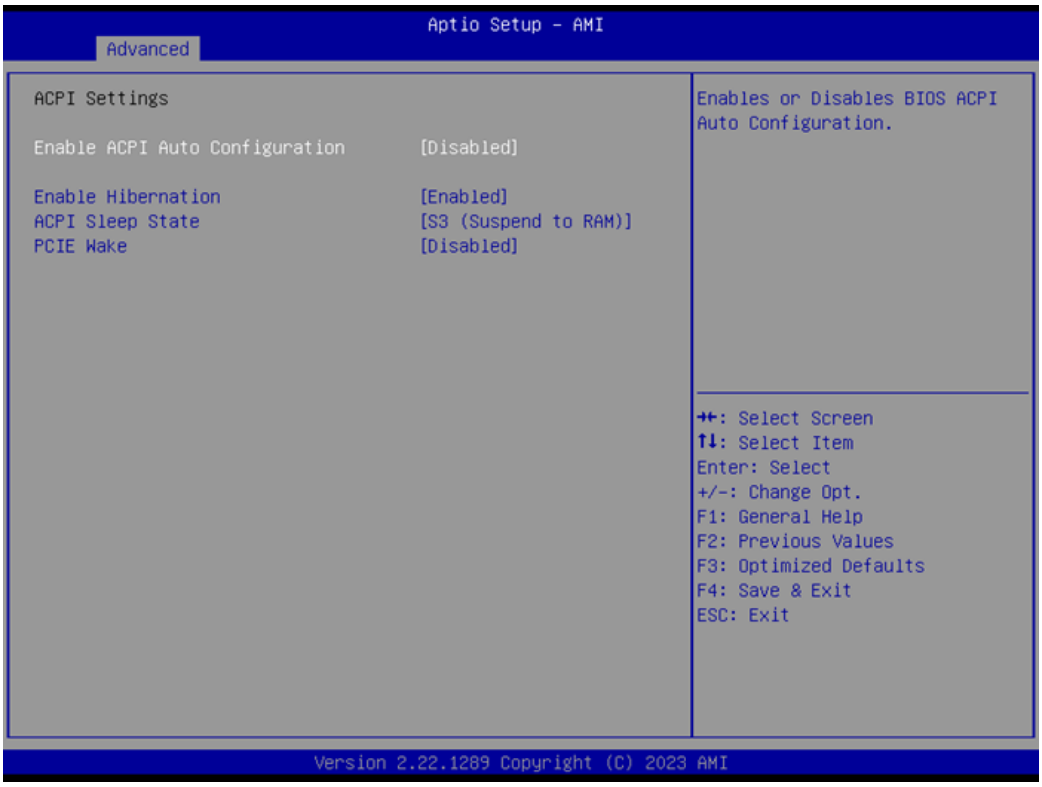

Figure 4.14

- **Enable ACPI Auto Configuration**
  Enable or disable BIOS ACPI auto configuration.
- **Enable Hibernation**
  Enables or Disables the system ability to hibernate (OS/S4 Sleep State). This option may not be effective with some OS.
- **ACPI Sleep State**
  Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.
- **PCIE Wake**
  Enable or disable PCIE to wake the system from S5.

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4.1.3.6 NCT6126D Super IO Configuration

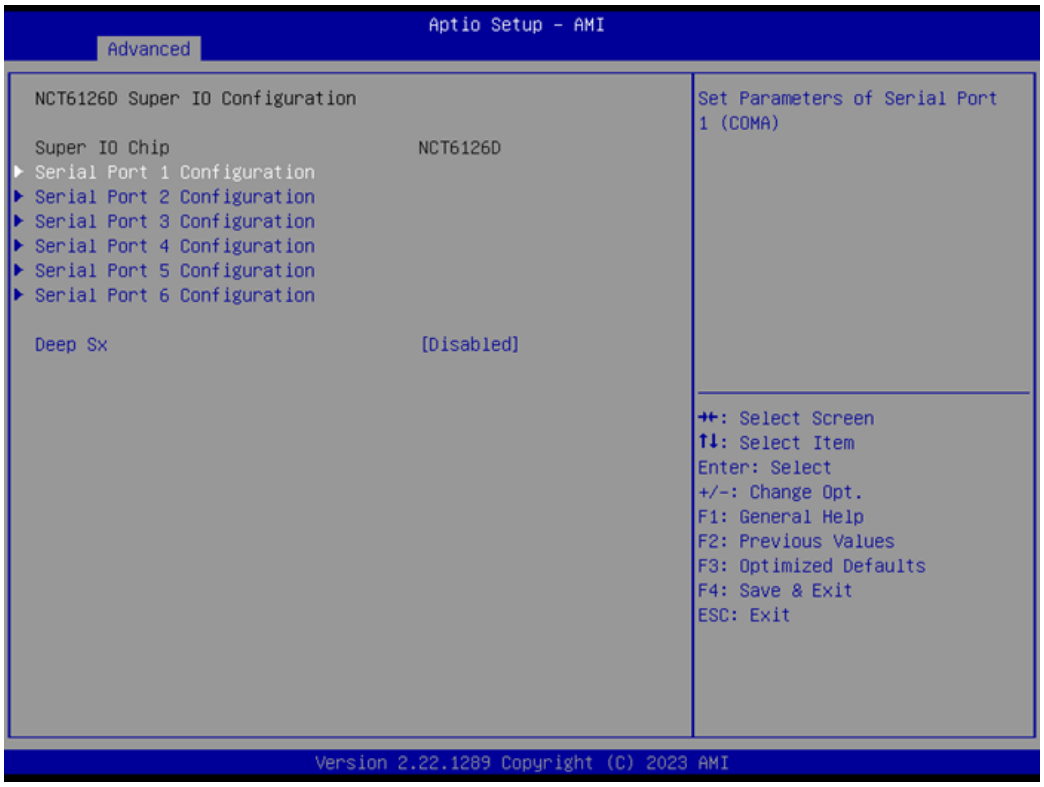

Figure 4.15

- **Serial Port 1 Configuration**
  Set Parameters of Serial Port 1.
- **Serial Port 2 Configuration**
  Set Parameters of Serial Port 2.
- **Serial Port 3 Configuration**
  Set Parameters of Serial Port 3.
- **Serial Port 4 Configuration**
  Set Parameters of Serial Port 4.
- **Serial Port 5 Configuration**
  Set Parameters of Serial Port 5.
- **Serial Port 6 Configuration**
  Set Parameters of Serial Port 6.
- **Deep Sx**
  Enable or Disable the Deep Sx function.

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Serial Port 1 Configuration

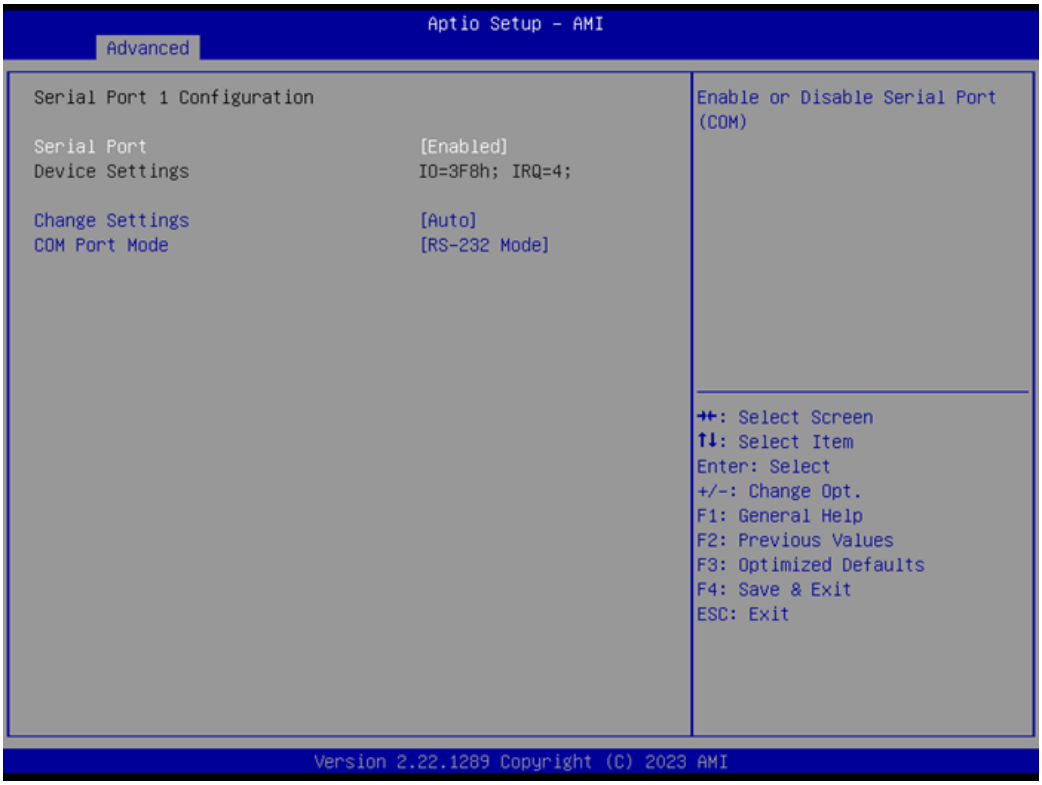

Figure 4.16

- **Serial Port**
  Enable or Disable Serial Port (COM).
- **Change Settings**
  Select an optimal settings for a Super IO device.
- **COM Port Mode**
  COM Port Mode Select.

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Serial Port 2 Configuration

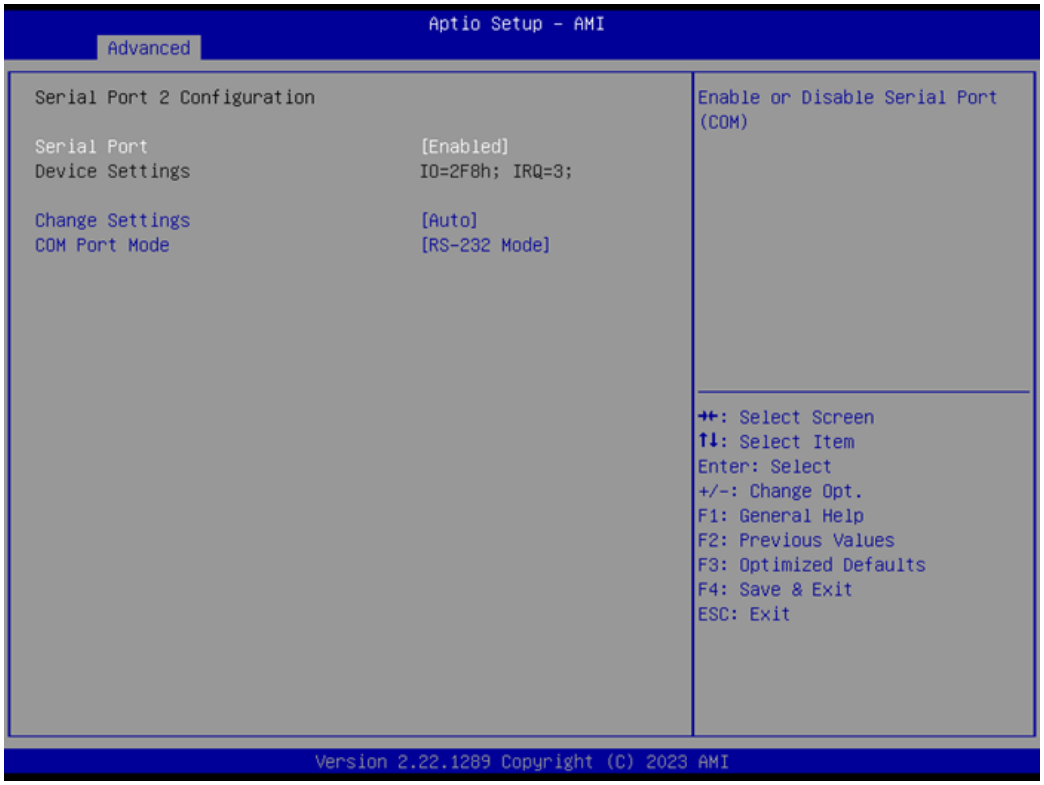

Figure 4.17

- **Serial Port**
  Enable or Disable Serial Port (COM).
- **Change Settings**
  Select an optimal setting for a Super IO device.
- **COM Port Mode**
  COM Port Mode Select.

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Serial Port 3 Configuration

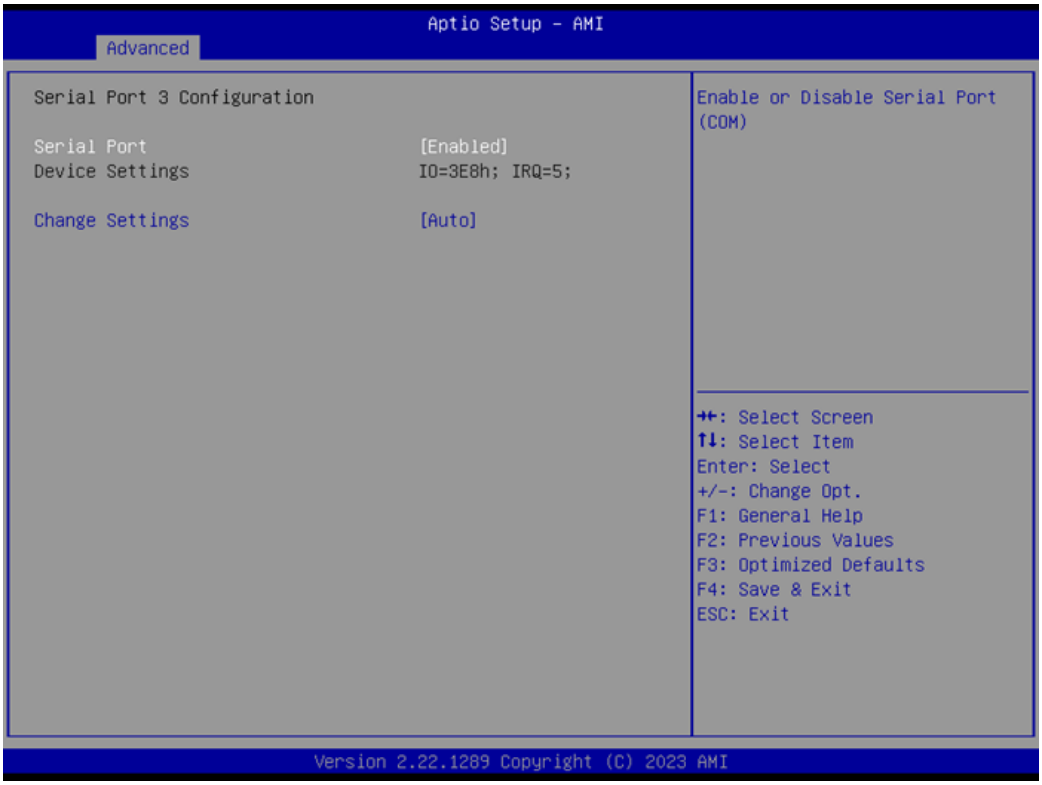

Figure 4.18

- **Serial Port**
  Enable or Disable Serial Port (COM).
- **Change Settings**
  Select optimal settings for a Super IO device.

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Serial Port 4 Configuration

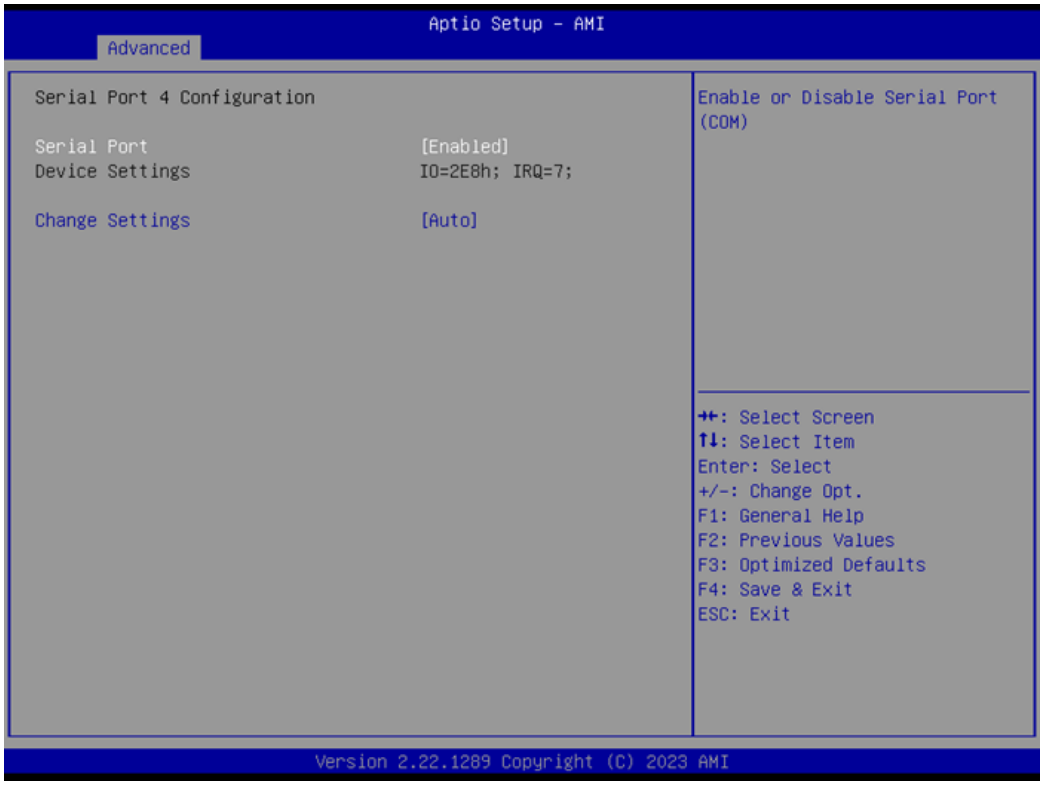

Figure 4.19

- **Serial Port**
  Enable or Disable Serial Port (COM).
- **Change Settings**
  Select optimal settings for a Super IO device.

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Serial Port 5 Configuration

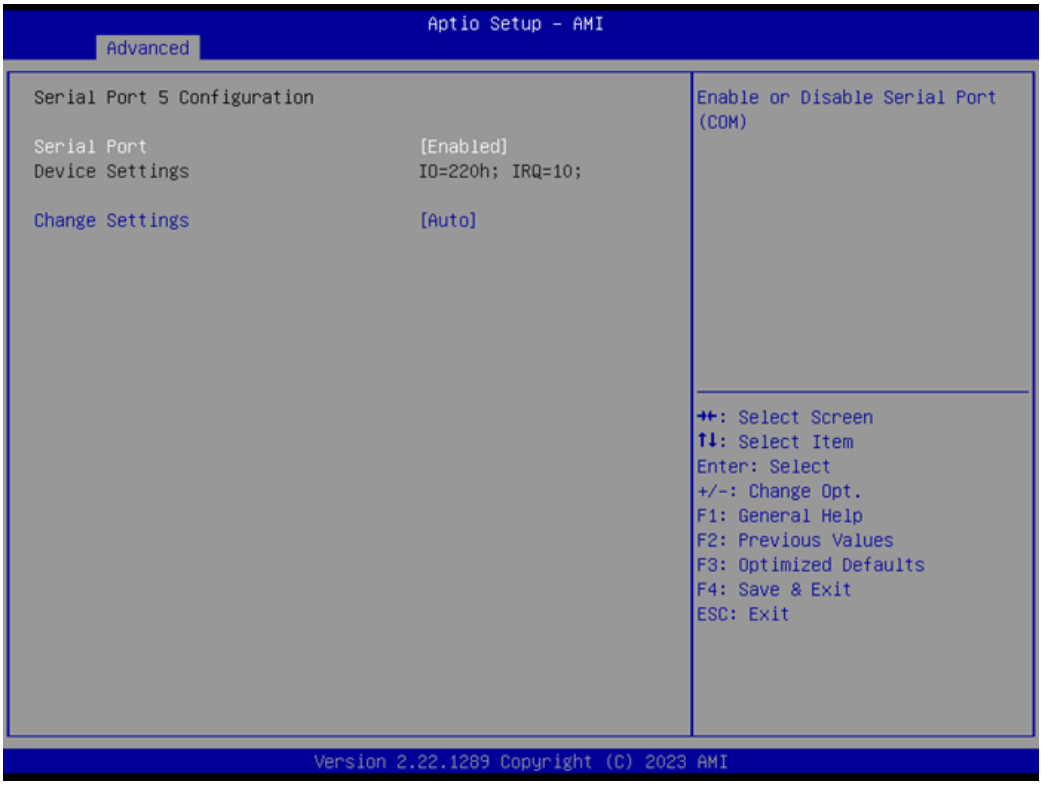

Figure 4.20

- **Serial Port**
  Enable or Disable Serial Port (COM).
- **Change Settings**
  Select optimal settings for a Super IO device.

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Serial Port 6 Configuration

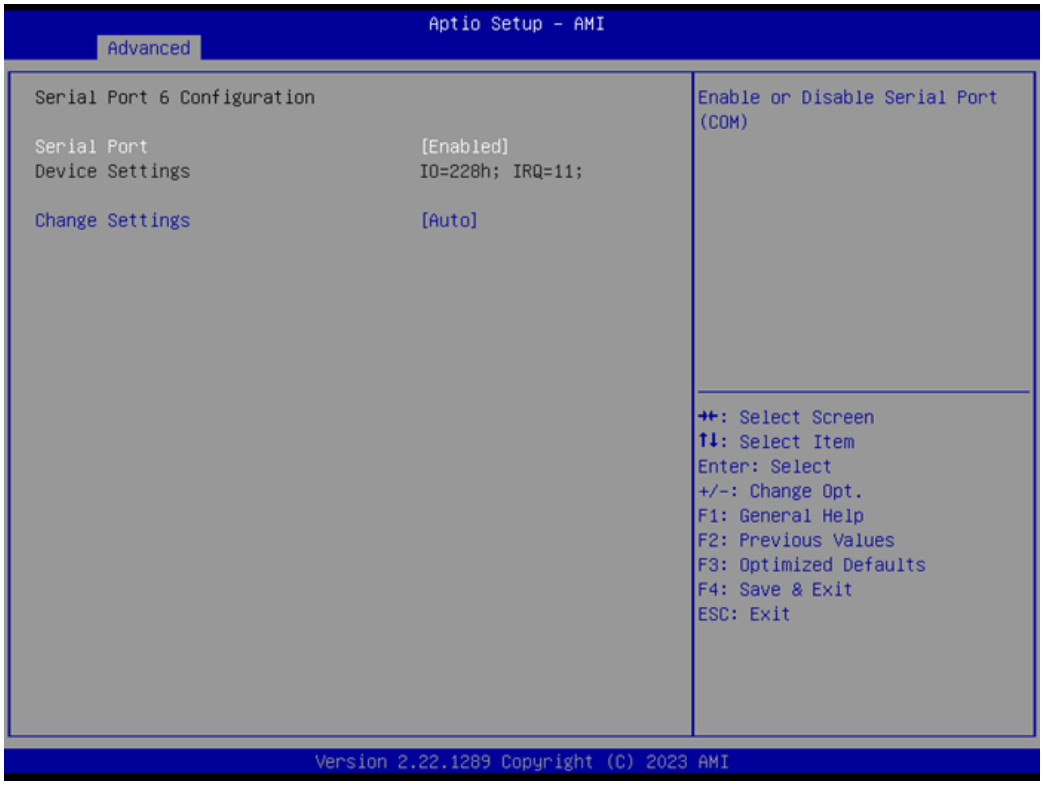

Figure 4.21

- **Serial Port**
  Enable or Disable Serial Port (COM).
- **Change Settings**
  Select optimal settings for a Super IO device.

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4.1.3.7 NCT6126D HW Monitor

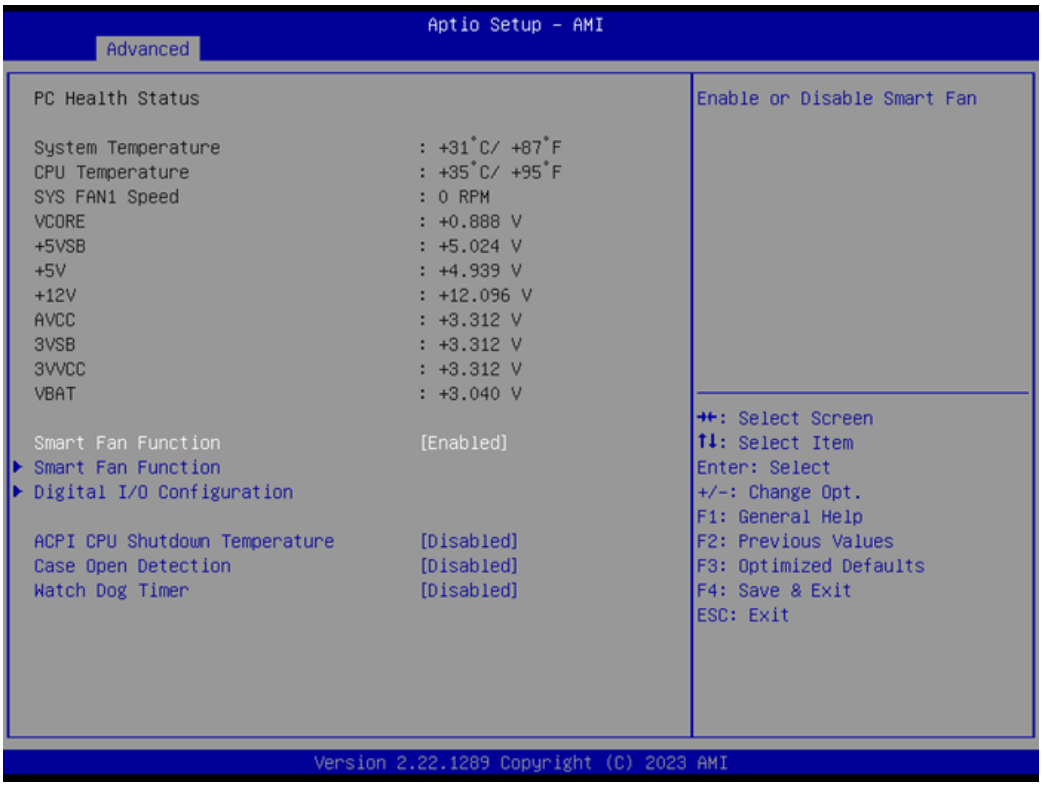

Figure 4.22

- **Smart Fan Function**
  Enable or Disable Smart Fan.
- **Digital I/O Configuration**
  Configure the digital I/O pins.
- **ACPI CPU Shutdown Temperature**
  Select the Critical Temperature value where OSPM must shut down the system.
- **Case Open Detection**
  Enable or Disable the Case Open Detect function.
- **Watch Dog Timer**
  Enable or Disable the Watch Dog Timer function.

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Smart Fan Function

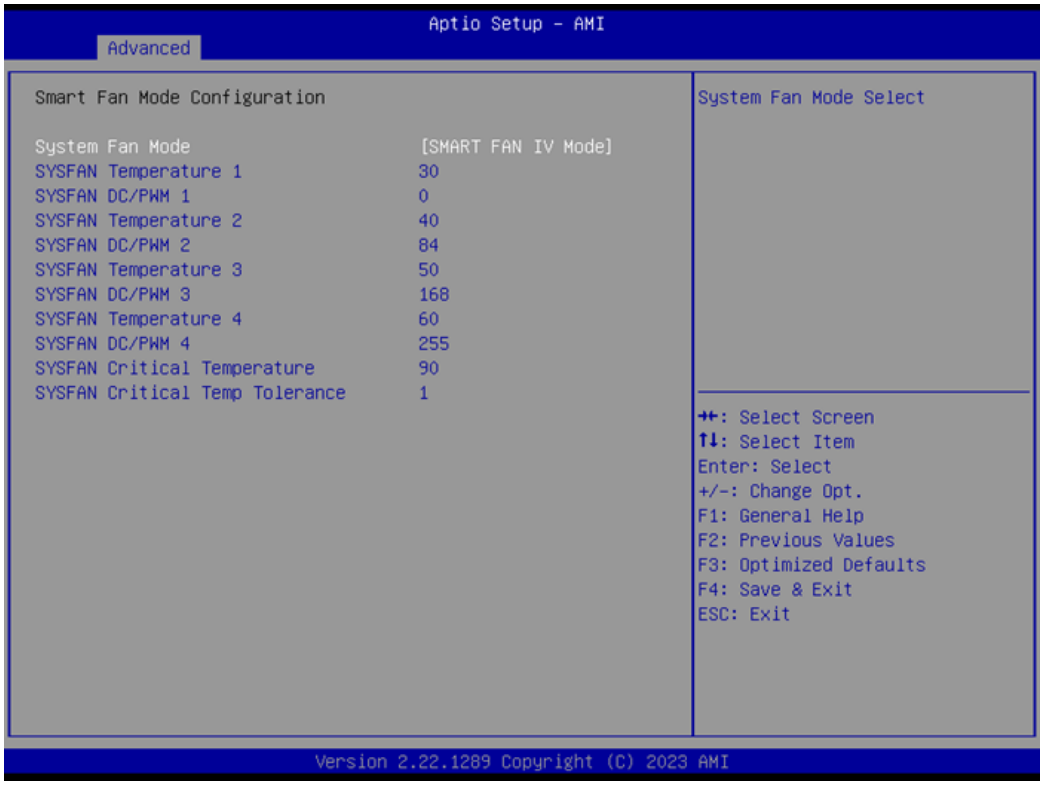

Figure 4.23

- **System Fan Mode**
  System Fan Mode Select.
- **SYSFAN Temperature 1**
  Input the System Smart Fan IV Temperature 1.
- **SYSFAN DC/PWM 1**
  Input the System Smart Fan IV DC/PWM 1 Value.
- **SYSFAN Temperature 2**
  Input the System Smart Fan IV Temperature 2.
- **SYSFAN DC/PWM 2**
  Input the System Smart Fan IV DC/PWM 2 Value.
- **SYSFAN Temperature 3**
  Input the System Smart Fan IV Temperature 3.
- **SYSFAN DC/PWM 3**
  Input the System Smart Fan IV DC/PWM 3 Value.
- **SYSFAN Temperature 4**
  Input the System Smart Fan IV Temperature 4.
- **SYSFAN DC/PWM 4**
  Input the System Smart Fan IV DC/PWM 4 Value.
- **SYSFAN Critical Temperature**
  Input the System Smart Fan IV Critical Temperature.
- **SYSFAN Critical Temp Tolerance**
  Input Tolerance of Critical Temperature (Range:0 - 7).

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Digital I/O Configuration

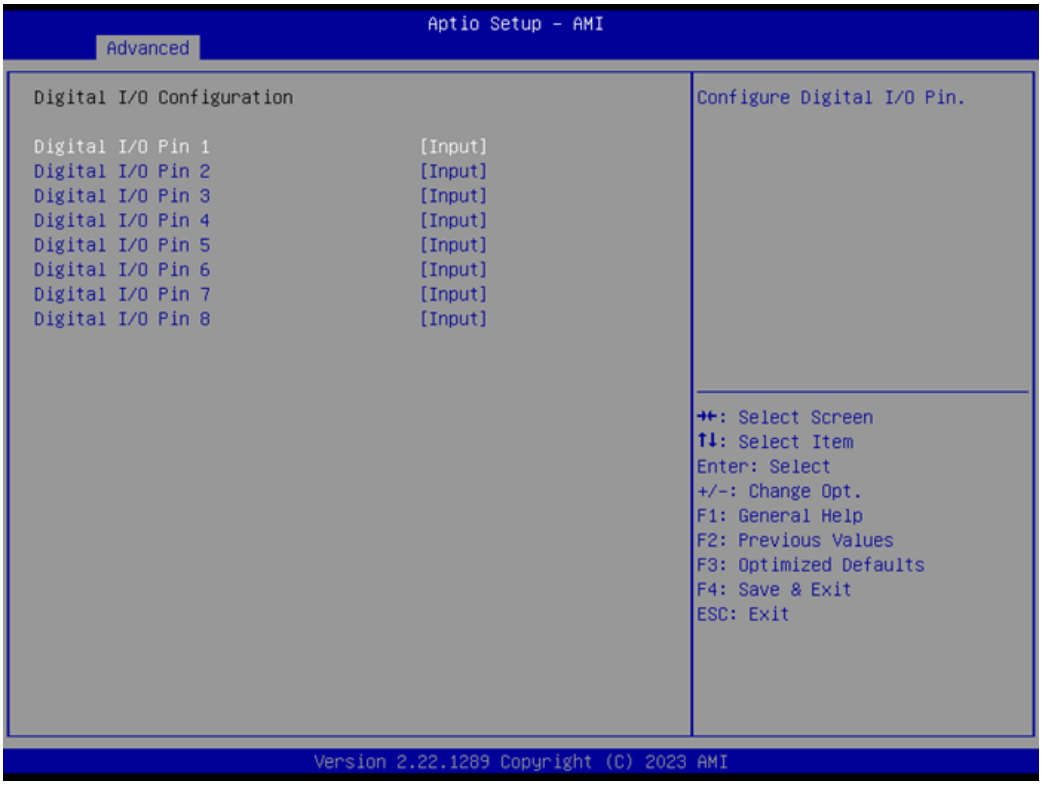

Figure 4.24

- **Digital I/O Pin 1/2/3/4/5/6/7/8**
  Configure Digital I/O Pins.

4.1.3.8 Trusted Computing

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Figure 4.25

- **TPM Device Selection**
  Select TPM device: fTPM or dTPM.
- **Security Device Support**
  Enable or disable BIOS support for a security device.
- **SHA-1 PCR Bank**
  Enable or Disable SHA-1 PCR Bank.
- **SHA256 PCR Bank**
  Enable or Disable SHA256 PCR Bank.
- **SHA384 PCR Bank**
  Enable or Disable SHA384 PCR Bank.
- **Pending operation**
  Schedule an Operation for the Security Device.
- **Platform Hierarchy**
  Enable or Disable Platform Hierarchy.
- **Storage Hierarchy**
  Enable or Disable Storage Hierarchy.
- **Endorsement Hierarchy**
  Enable or Disable Endorsement Hierarchy.
- **TPM 2.0 UEFI Spec Version**
  Select the TCG2 Spec Version Support.
- **Physical Presence Spec Version**
  Select to tell the OS to support PPI Spec Version 1.2 or 1.3.
- **Device Select**
  TPM 1.2 will restrict support to TPM 1.2 devices. TPM 2.0 will restrict support to TPM 2.0 devices.

4.1.3.9 S5 RTC Wake Settings

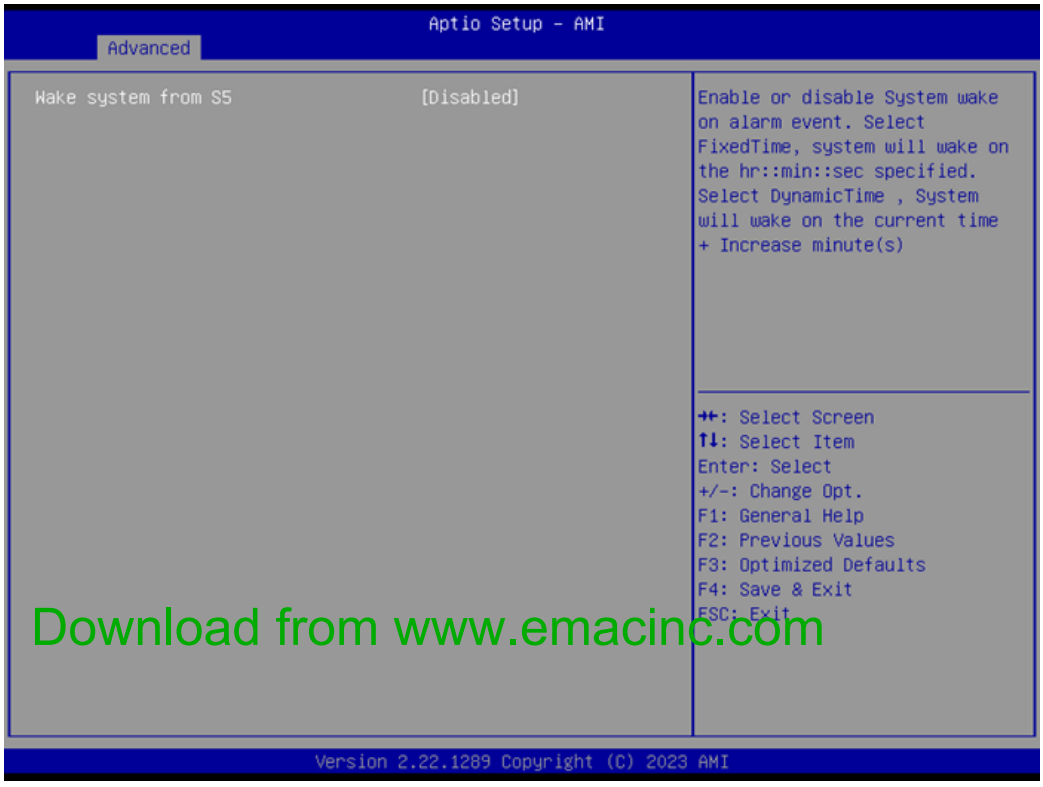

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Figure 4.26

- **Wake system from S5**
  Enable/Disable System wake-on-alarm event. Select FixedTime for the system to wake at the hr:min:sec specified.

4.1.3.10 Serial Port Console Redirection

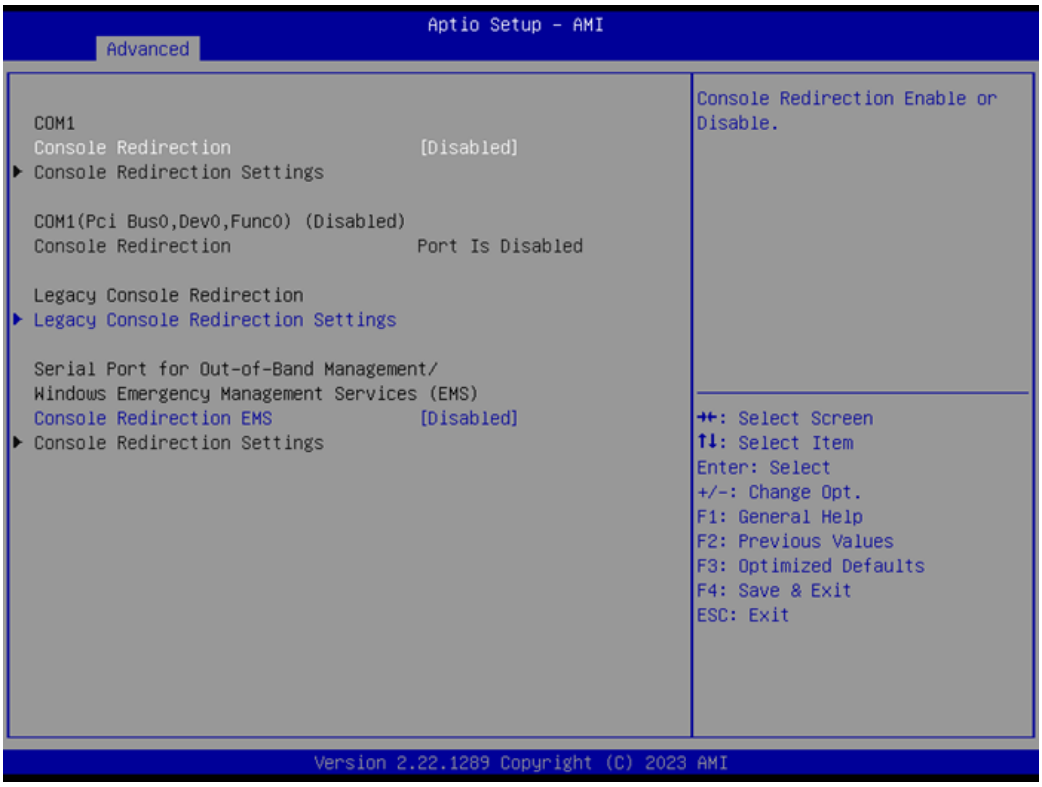

Figure 4.27

- **Console Redirection**
  This item allows users to enable or disable console redirection for Microsoft Windows Emergency Management Services (EMS).
- **Console Redirection**
  This item allows users to configure console redirection detail settings.

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4.1.3.11 USB Configuration

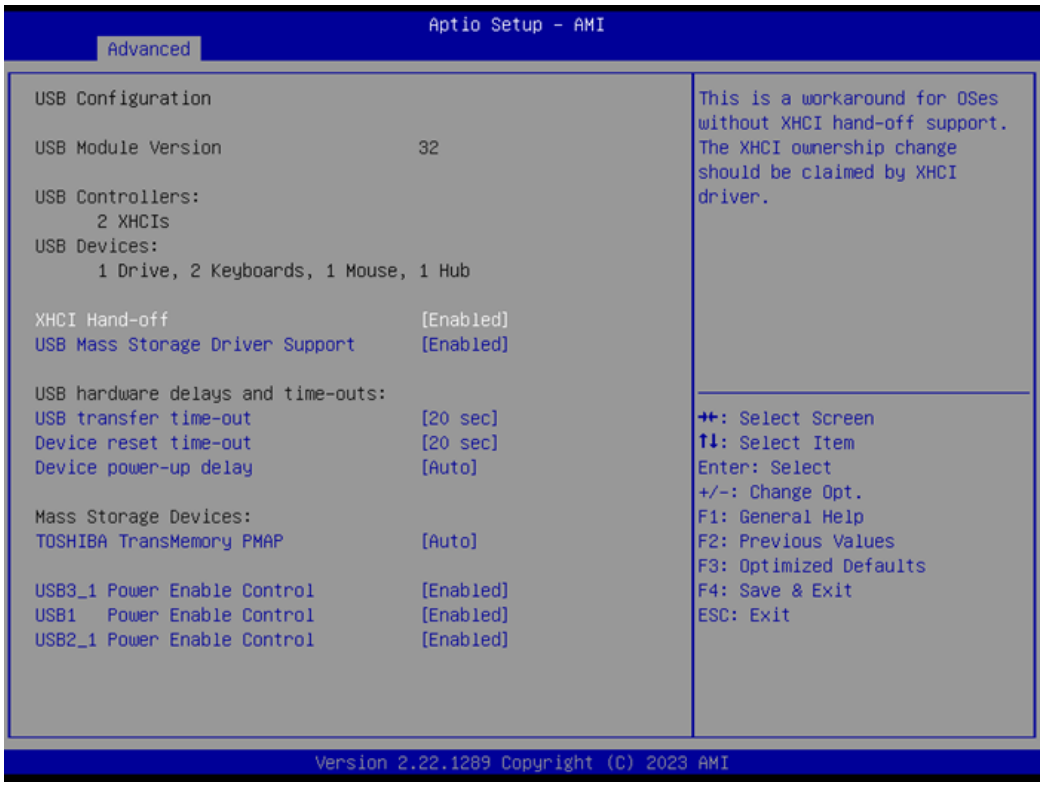

Figure 4.28

- **XHCI Hand-off**
  This is a workaround for OS without XHCI hand-off support. The XHCI ownership change should be claimed by the XHCI driver.
- **USB Mass Storage Driver Support**
  Enable/Disable USB Mass Storage Driver Support.
- **USB transfer time-out**
  Time-out value for control, bulk, and interrupt transfers.
- **Device reset time-out**
  USB mass storage device start unit command time-out.
- **Device power-up delay**
  Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses the default value: for a Root port it is 100 ms, for a Hub port the delay is taken from the Hub descriptor.
- **USB3_1 Power Enable Control**
  Enable/Disable power off USB3_1 Rear port in S4/S5.
- **USB1 Power Enable Control**
  Enable/Disable power off USB1 Internal port in S4/S5.
- **USB2_1 Power Enable Control**
  Enable/Disable power off USB2_1 Rear port in S4/S5.

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4.1.3.12 Network Stack Configuration

Figure 4.29

- **Network Stack**
  Enable/Disable UEFI Network Stack.

4.1.3.13 NVMe Configuration

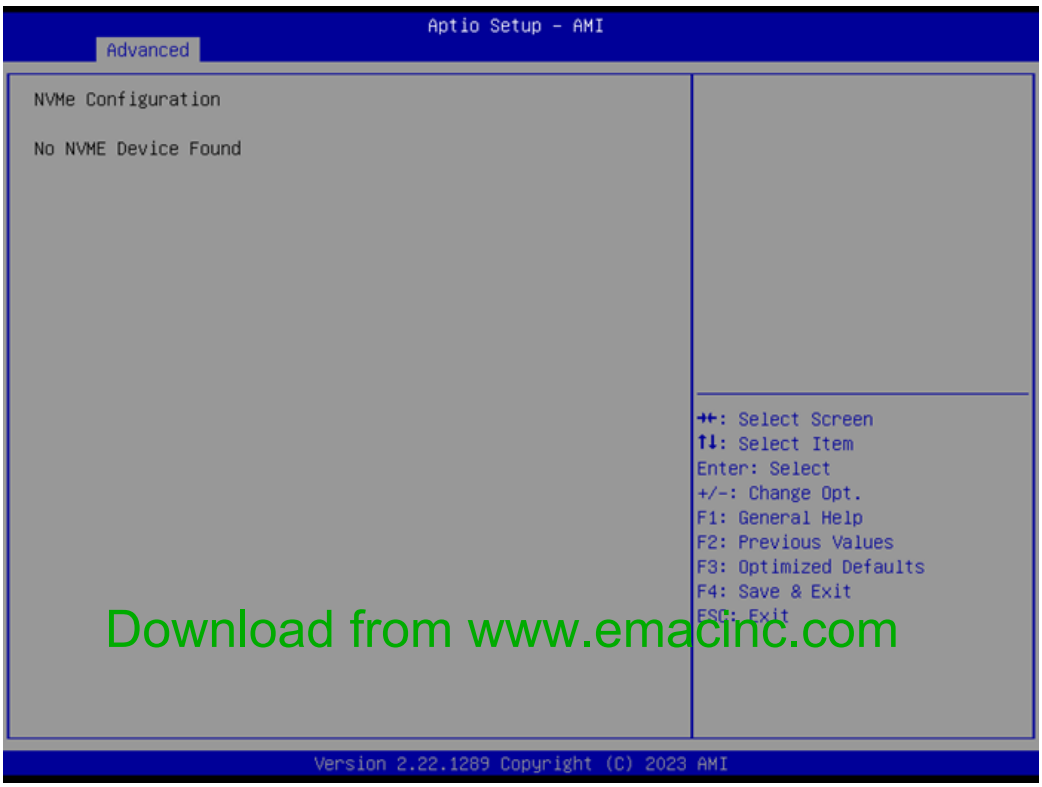

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Figure 4.30

4.1.4 Chipset Configuration

Select the Chipset tab from the MIO-5154 setup screen to enter the Chipset BIOS Setup screen. You can display a Chipset BIOS Setup option by highlighting it using the <Arrow> keys. All Plug and Play BIOS Setup options are described in this section. The Plug and Play BIOS Setup screen is shown below.

Figure 4.31

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4.1.4.1 System Agent (SA) Configuration

Figure 4.32

- **Memory Configuration**
  Memory Configuration Parameters.
- **Graphics Configuration**
  Graphics Configuration Parameters.
- **DMI/OPI Configuration**
  Control various DMI functions.
- **Display Setup Menu**
  Display Configuration settings.
- **Stop Grant Configuration**
  Automatic/Manual stop grant configuration.
- **VT-d**
  VT-D capability.
- **Control Iommu Pre-Boot Behavior**
  Enable IOMMU in the Pre-boot environment.
- **X2APIC Opt Out**
  Enable/Disable X2APIC Opt Out Bit.
- **Above 4GB MMIO BIOS assignment**
  Enable/Disable above 4GB Memory Mapped IO BIOS assignment.

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Memory Configuration

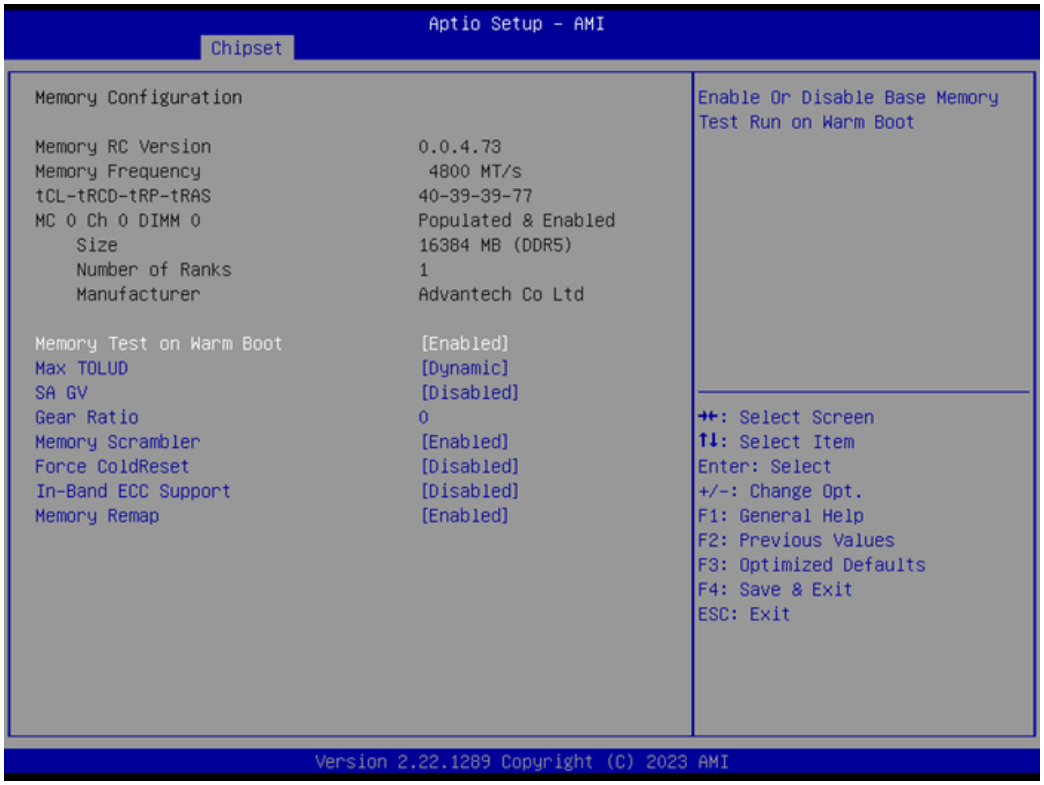

Figure 4.33

- **Memory Test on Warm Boot**
  Enable/Disable Base Memory Test Run on Warm Boot.
- **Max TOLUD**
  Maximum Value of TOLUD.
- **SA GV**
  System Agent Geyserville.
- **Gear Ratio**
  Gear ratio when SAGV is disabled.
- **Memory Scrambler**
  Enable/Disable Memory Scrambler support.
- **Force ColdReset**
  Force ColdReset OR Choose MrcColdBoot mode.
- **In-Band ECC Support**
  Enable/Disable In-Band ECC.
- **Memory Remap**
  Enable/Disable Memory Remap above 4GB.

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Graphics Configuration

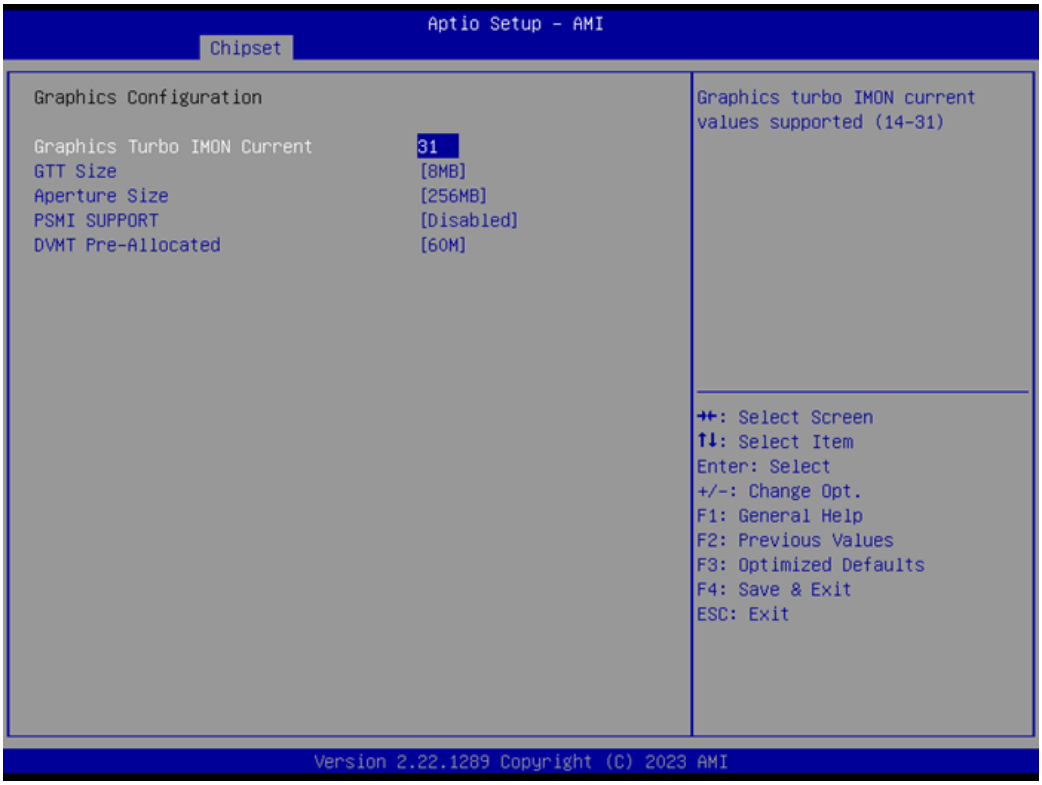

Figure 4.34

- **Graphics Turbo IMON Current**
  Graphics turbo IMON current values supported.
- **GTT Size**
  Select the GTT Size.
- **Aperture Size**
  Select the Aperture Size.
- **PSMI Support**
  Enable/Disable PSMI.
- **DVMT Pre-Allocated**
  Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.

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LVDS

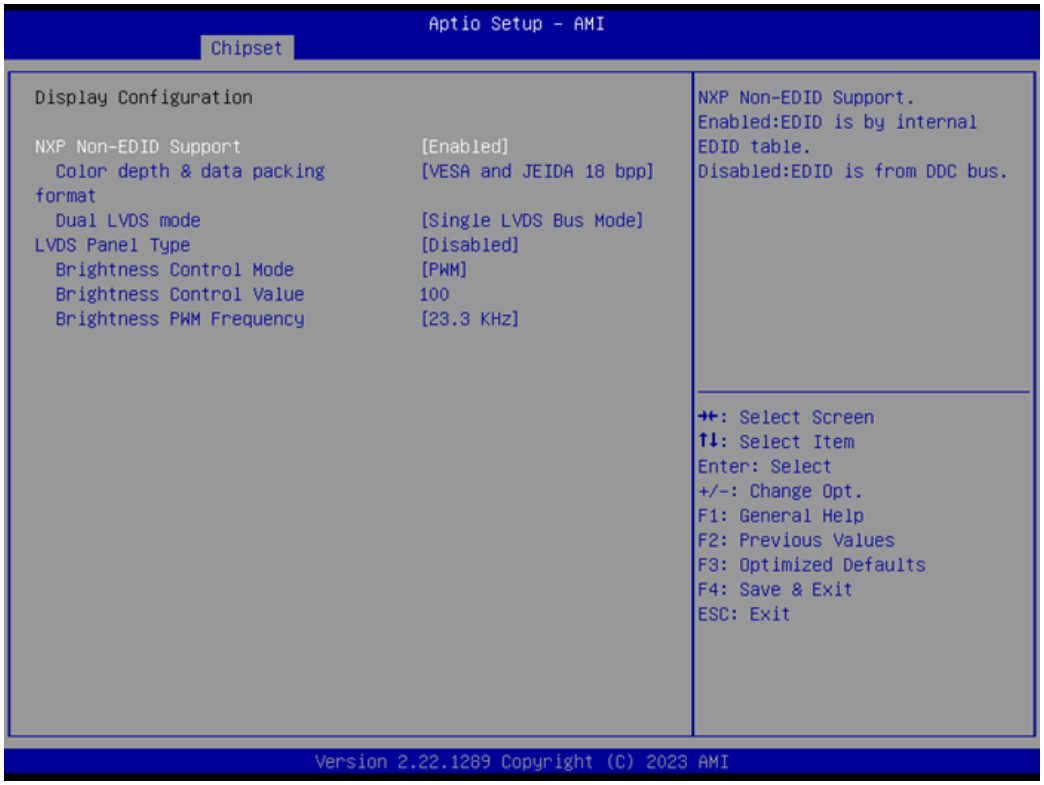

Figure 4.35

- **NXP Non-EDID Support**
  Non-EDID Support.
- **Color Depth & Data Packing**
  Color depth and data packing format for Non-EDID Support.
- **Dual LVDS Mode**
  Select LVDS bus to Single bus mode or Dual bus mode.
- **LVDS Panel Type**
  This item allows the user to select the LVDS panel resolution type.
- **Brightness Control Mode**
  Switch Brightness Control to Linear or PWM mode.
- **Brightness Control Value**
  Choose to override the LVDS brightness value during POST stage. Value from 0 ~ 100.
- **Brightness PWM Frequency**
  Adjust LVDS Brightness PWM Frequency.

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DMI/OPI Configuration

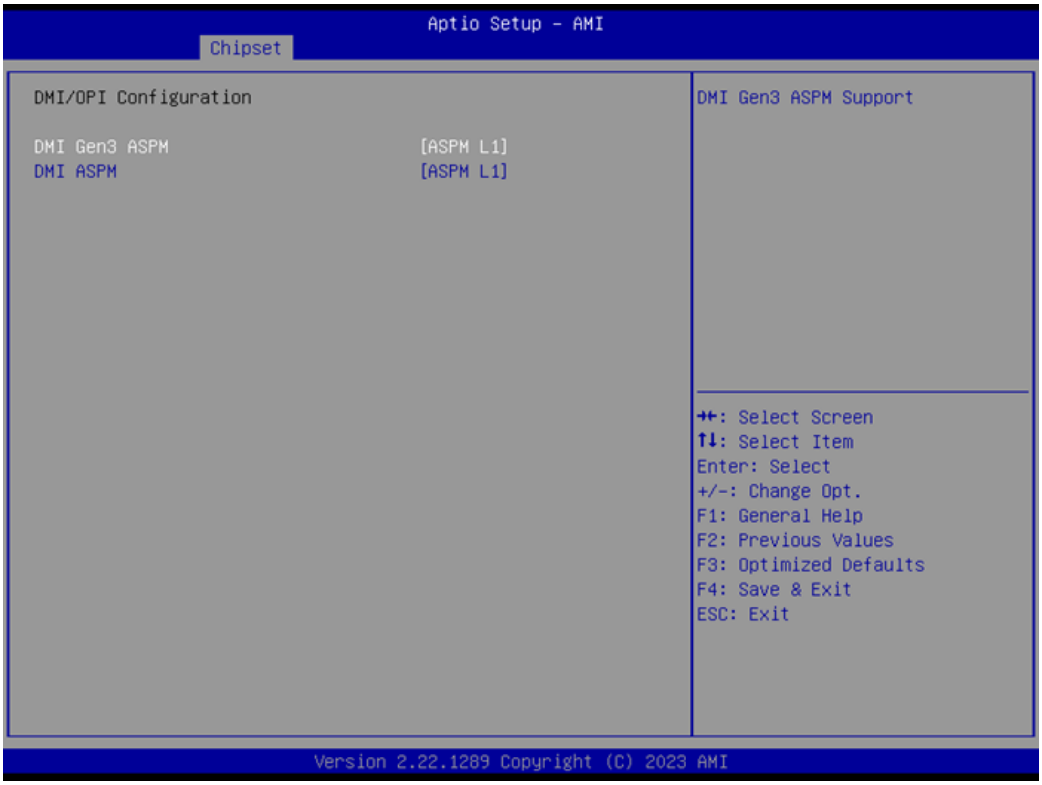

Figure 4.36

- **DMI Gen3 ASPM**
  DMI Gen3 ASPM Support.
- **DMI ASPM**
  DMI ASPM Support.

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4.1.4.2 PCH-IO Configuration

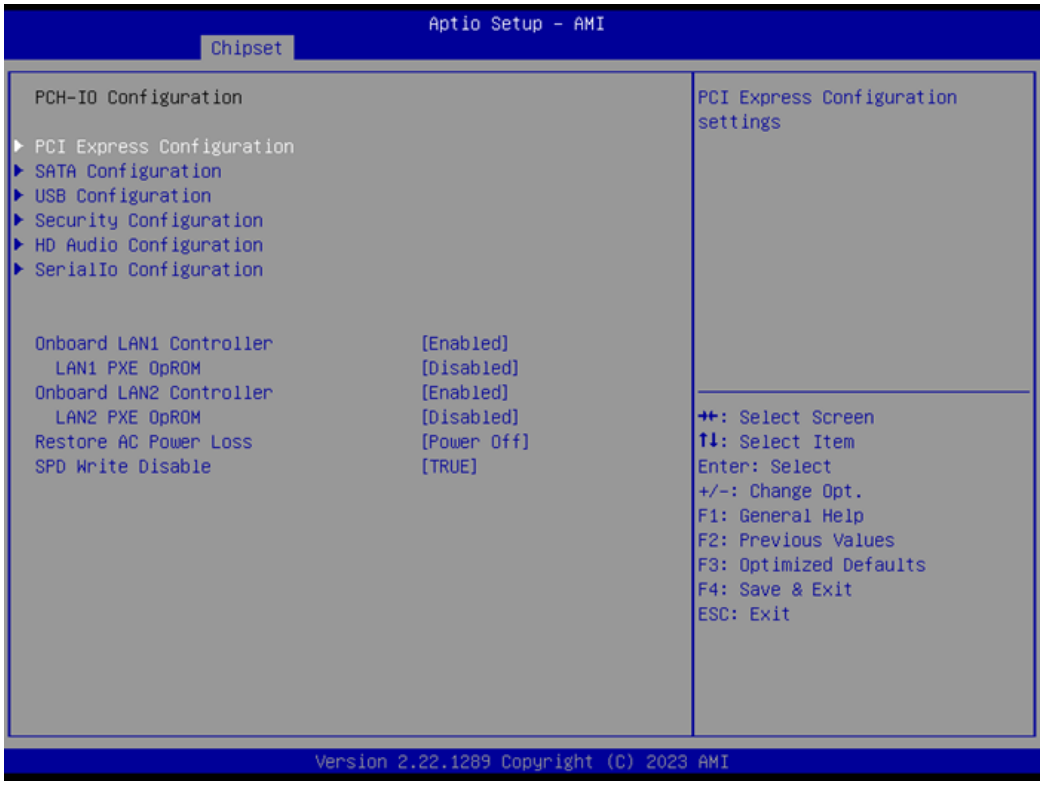

Figure 4.37

- **PCI Express Configuration**
  PCI Express Configuration Settings.
- **SATA Configuration**
  SATA Device Options Settings.
- **USB Configuration**
  USB Configuration Settings.
- **Security Configuration**
  Security Configuration Settings.
- **HD Audio Configuration**
  HD Audio Subsystem Configuration Settings.
- **Serial IO Configuration**
  Serial IO Configuration Settings.
- **Onboard LAN1 Controller**
  Select to Enable or Disable onboard LAN1 Controller.
- **LAN1 PXE ROM**
  Enable or Disable onboard LAN1's PXE option ROM.
- **Onboard LAN2 Controller**
  Select to Enable or Disable onboard LAN2 Controller.
- **LAN2 PXE ROM**
  Enable or Disable onboard LAN2's PXE option ROM.
- **Restore AC Power Loss**
  Specify what state to go to when power is re-applied after a power failure (G3 state).
- **SPD Write Disable**
  Enable/Disable setting SPD Write Disable.

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PCI Express Configuration

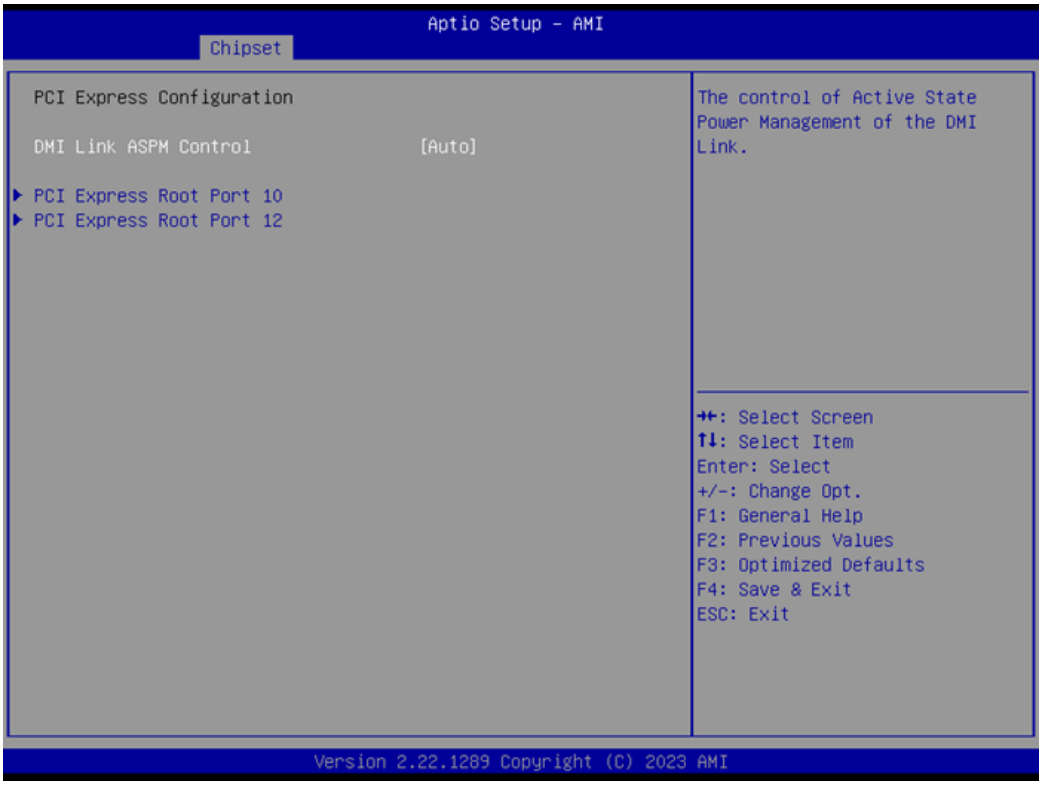

Figure 4.38

- **DMI Link ASPM Control**
  This item controls Active State Power Management of the DMI Link.
- **PCI Express Root Port 10/12**
  PCI Express Port 10/12 Settings.

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PCI Express Root Port 10

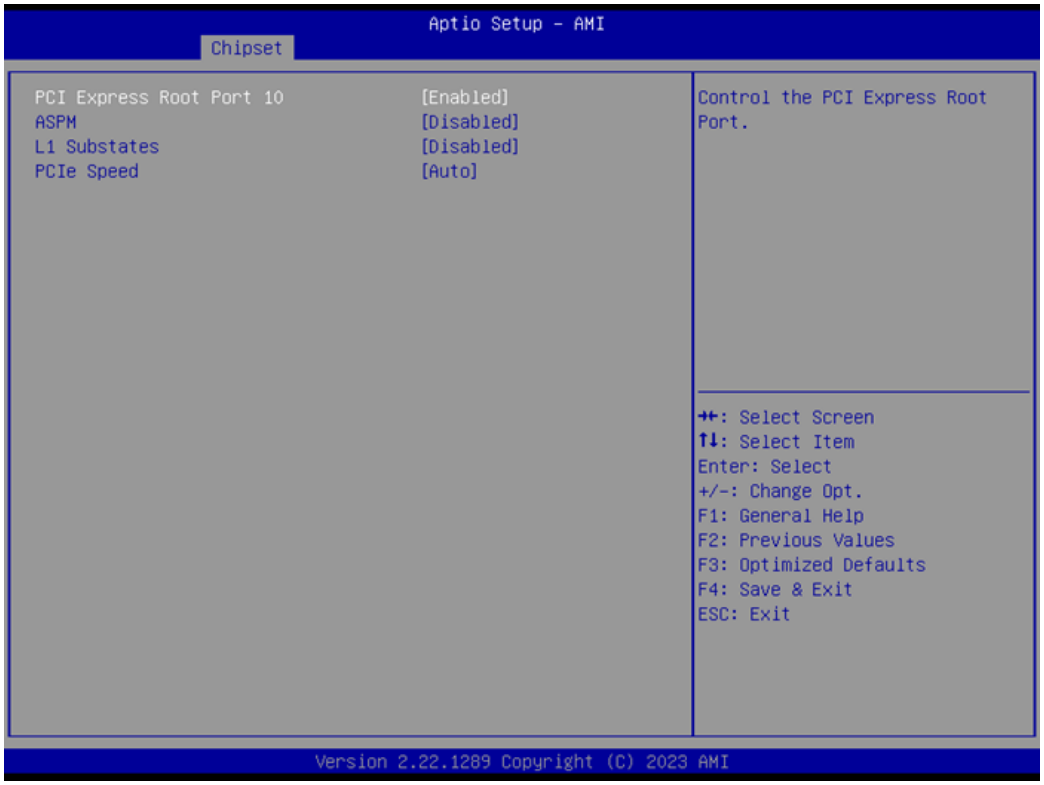

Figure 4.39

PCI Express Root Port 12

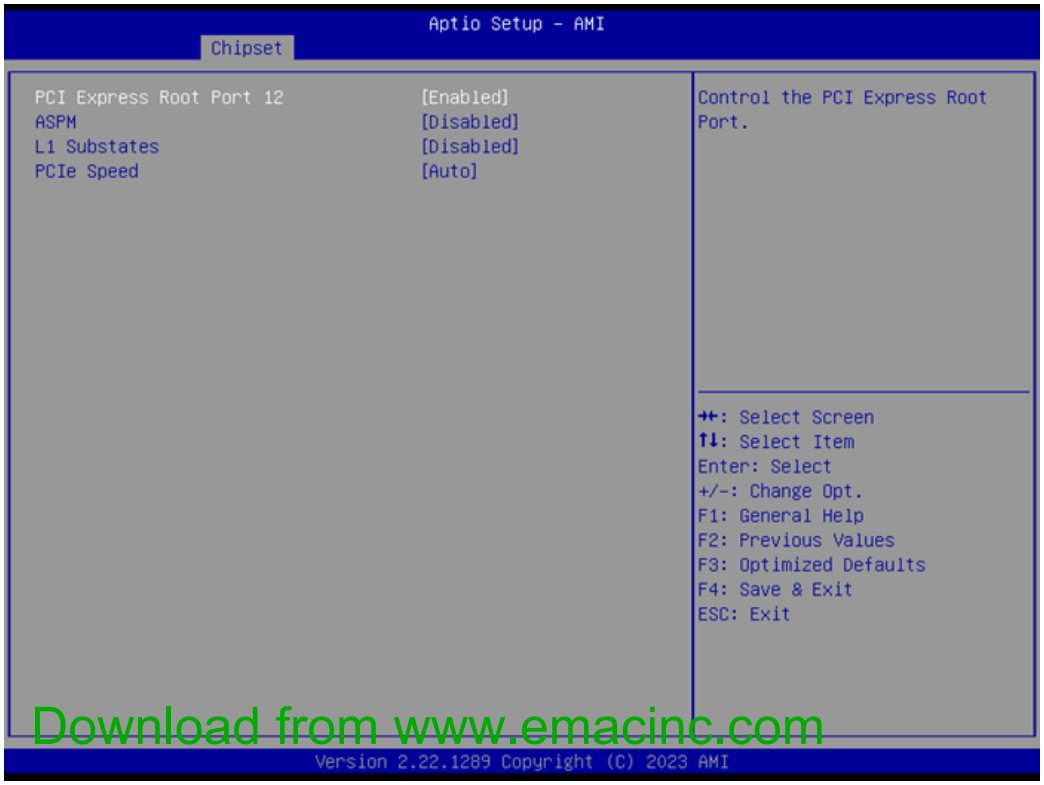

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Figure 4.40

SATA Configuration

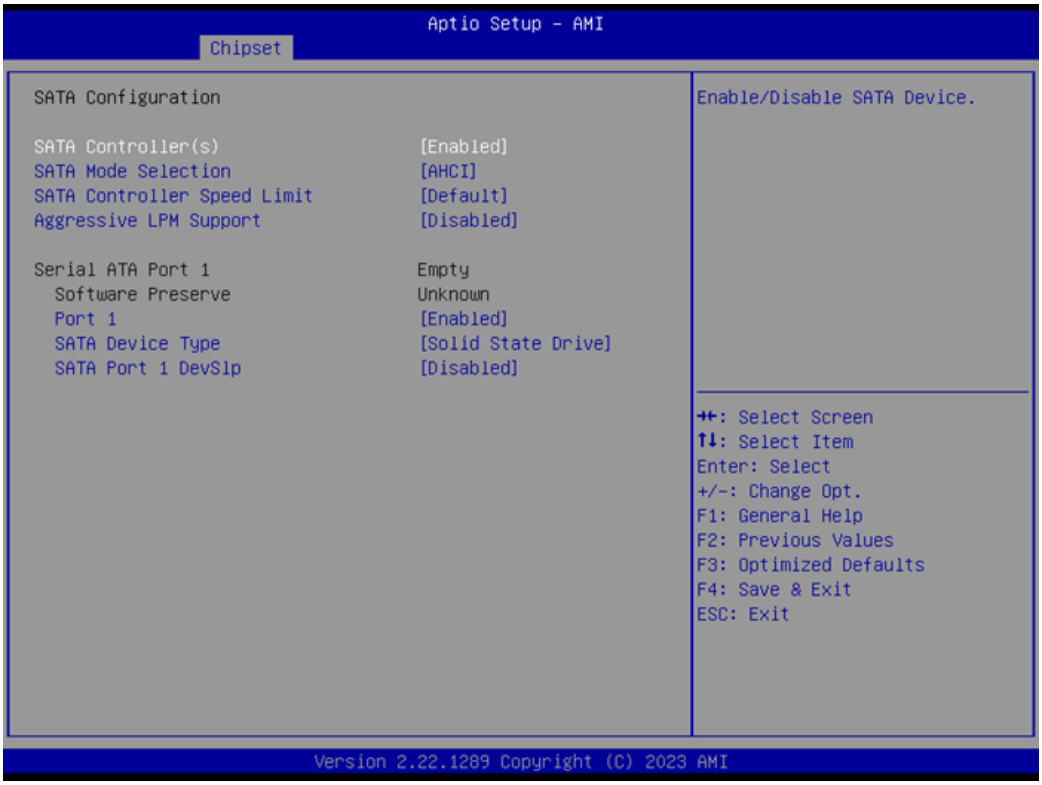

Figure 4.41

- **SATA Controller(s)**
  Enable/Disable SATA Device.
- **SATA Mode Selection**
  Determine how the SATA controller operates.
- **SATA Controller Speed Limit**
  Indicates the maximum speed the SATA controller can support.
- **Aggressive LPM Support**
  Enable PCH to aggressively enter link power state.

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USB Configuration

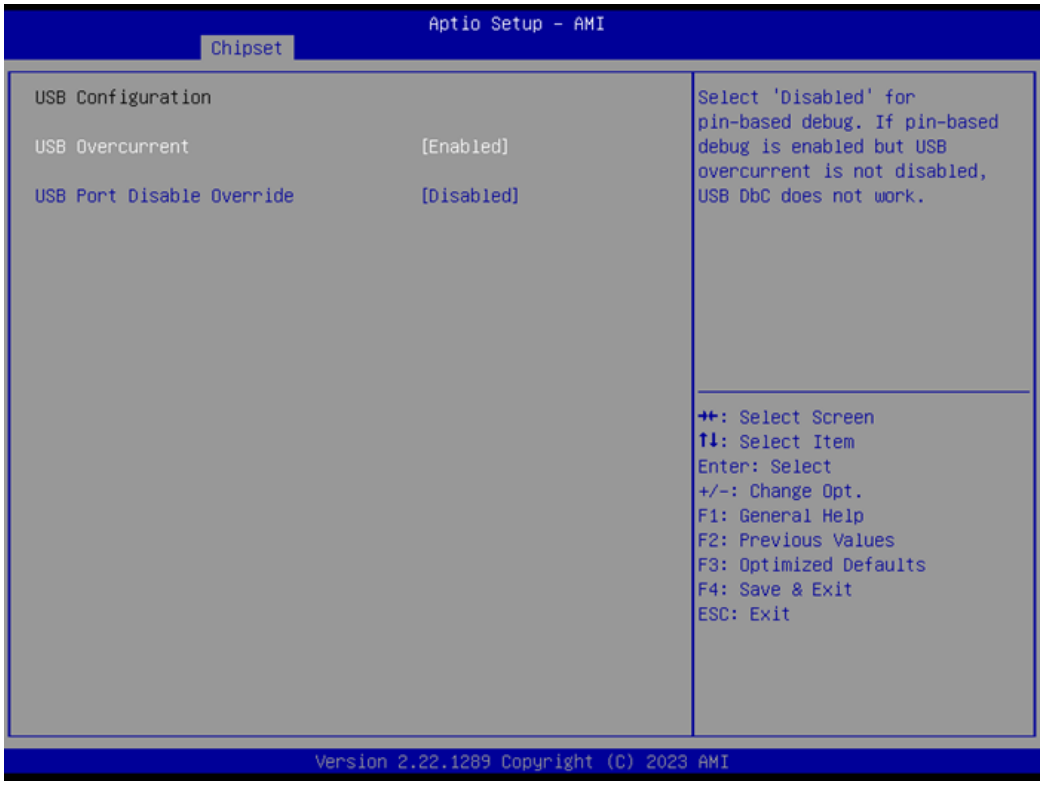

Figure 4.42

- **USB Overcurrent**
  Select "Enabled" if Overcurrent functionality is used.
- **USB Port Disable Override**
  Selectively Enable/Disable the corresponding USB Port from reporting a device connection to the controller.

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Security Configuration

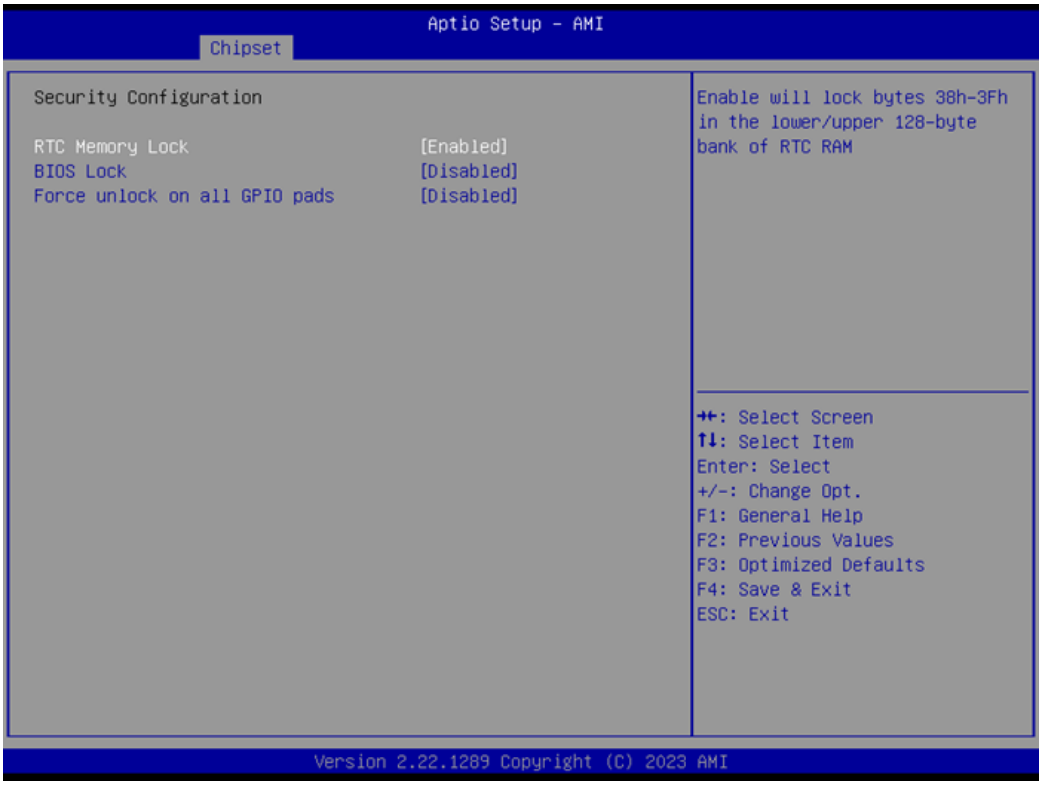

Figure 4.43

- **RTC Memory Lock**
  Enable will lock bytes 38h-3Fh in the lower/upper 128-byte bank of RTC RAM.
- **BIOS Lock**
  Enable or Disable the PCH BIOS Lock Enable feature.
- **Force unlock on all GPIO pads**
  If Enabled, BIOS will force all GPIO pads to be in the unlock state.

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HD Audio Configuration

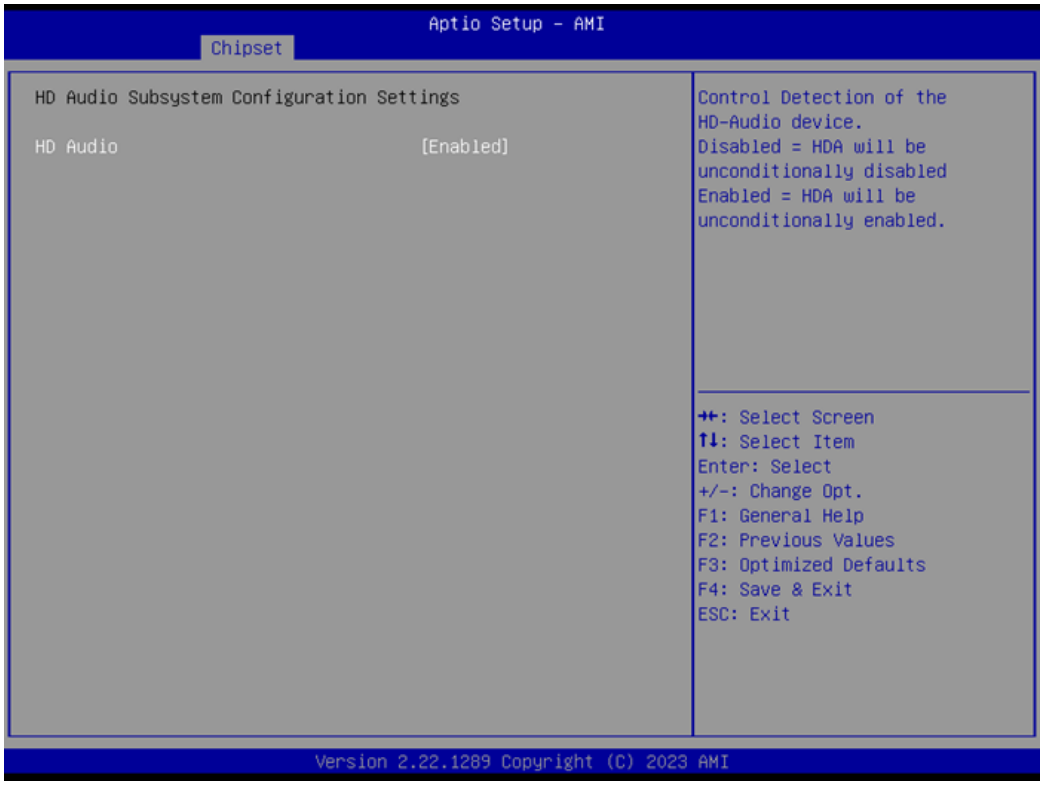

Figure 4.44

- **HD Audio**
  Control Detection of the HD-Audio device. Disabled = HDA will be uncondition-ally disabled. Enabled = HDA will be unconditionally enabled.

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Serial IO Configuration

Figure 4.45

- **I2C0 Controller**
  Enable/Disable Serial IO Controller.
- **Serial IO I2C0 Settings**
  Configure Serial IO Controller.

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Serial IO I2C0 Settings

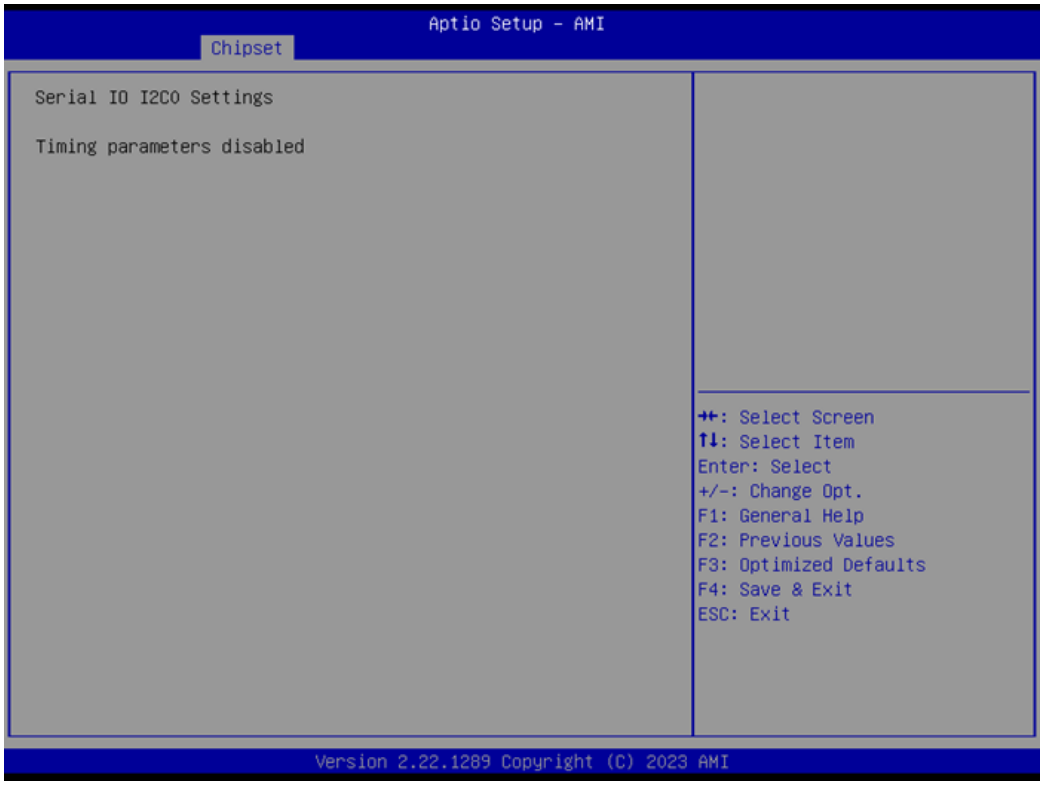

Figure 4.46

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4.1.5 Security

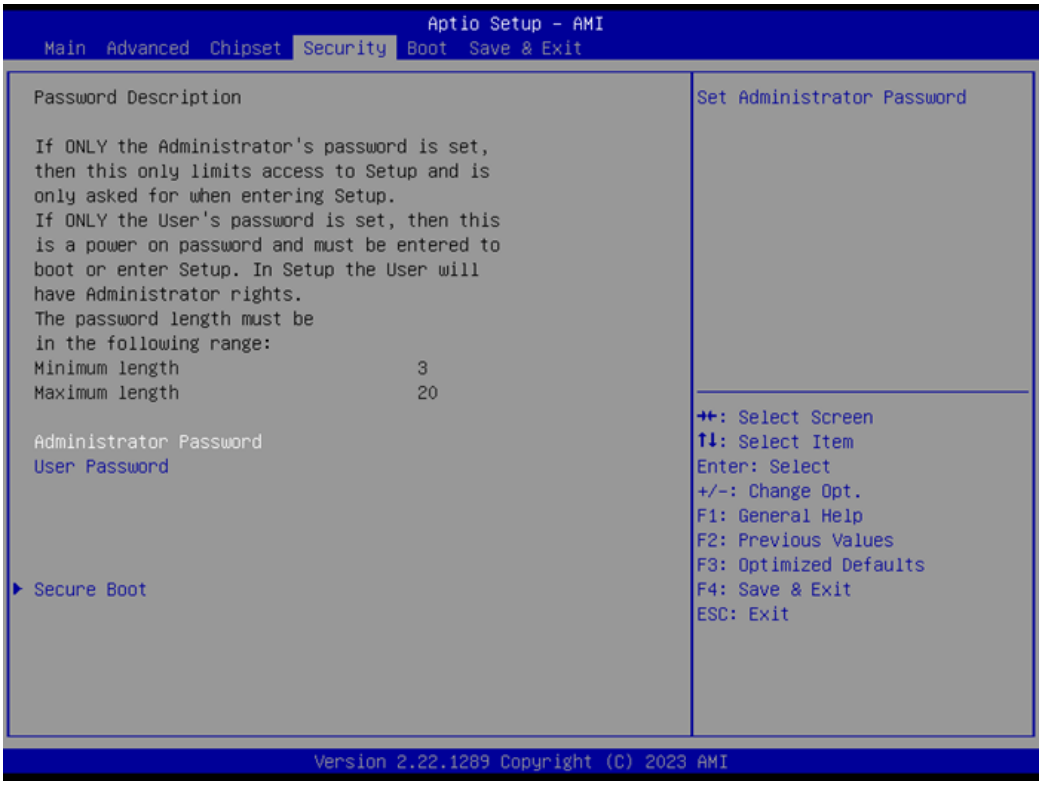

Figure 4.47

Select Security Setup from the MIO-5154 Setup main BIOS setup menu. All Security Setup options, such as password protection and virus protection, are described in this section. To access the sub-menu for the following items, select the item and press <Enter>:

- **Change Administrator / User Password**
  Select this option and press <ENTER> to access the sub-menu, and then type in the password.
- **Secure Boot**
  Secure Boot Configurations.

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4.1.6 Boot

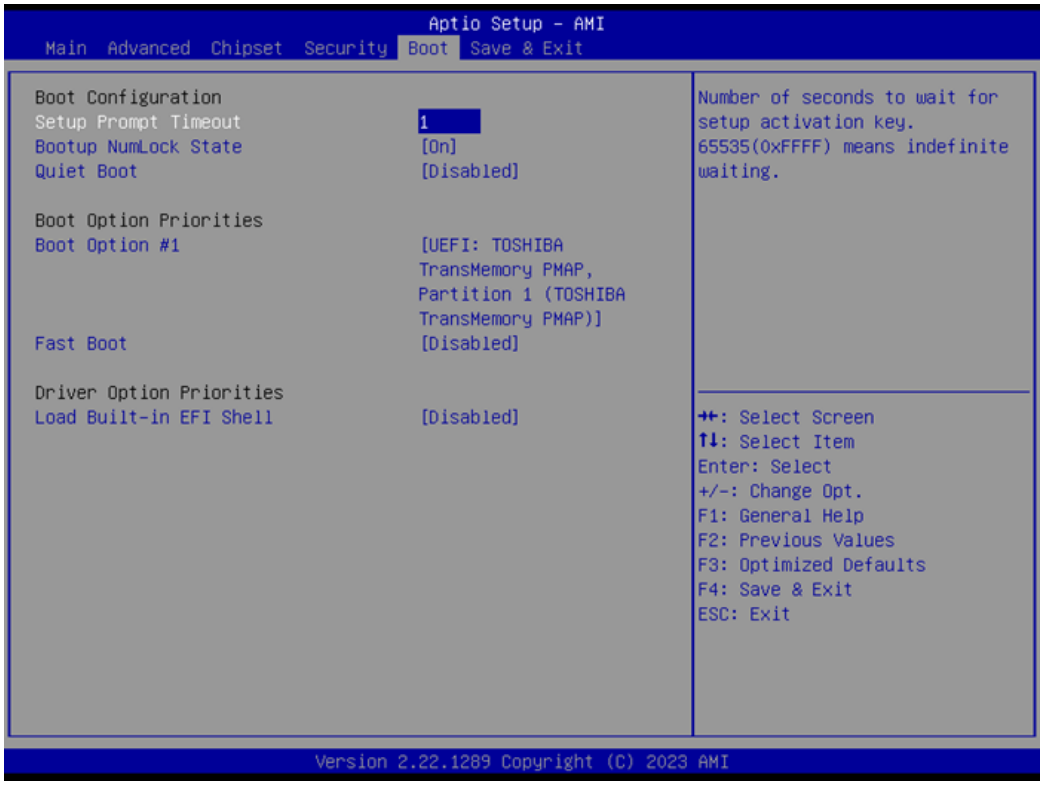

Figure 4.48

- **Setup Prompt Timeout**
  This is the number of seconds that the firmware will wait before initiating the original default boot selection. A value of 0 indicates that the default boot selection is to be initiated immediately on boot. A value of 65535(0xFFFF) indicates that firmware will wait for user input before booting. This means the default boot selection is not automatically started by the firmware.
- **Bootup NumLock State**
  Select the keyboard NumLock state.
- **Quiet Boot**
  Enables or disables the Quiet Boot option.
- **Boot Option #1**
  Sets the system boot order.
- **Fast Boot**
  Enable/Disables boot with initialization of a minimal set of devices required to launch the active boot option. It has no effect on BBS boot options.
- **Load Built-in EFI Shell**
  Load/Unload Internal Built-in EFI Shell image inside the BIOS. (Built-in EFI Shell will still be loaded if no bootable device is found).

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4.1.7 Save & Exit

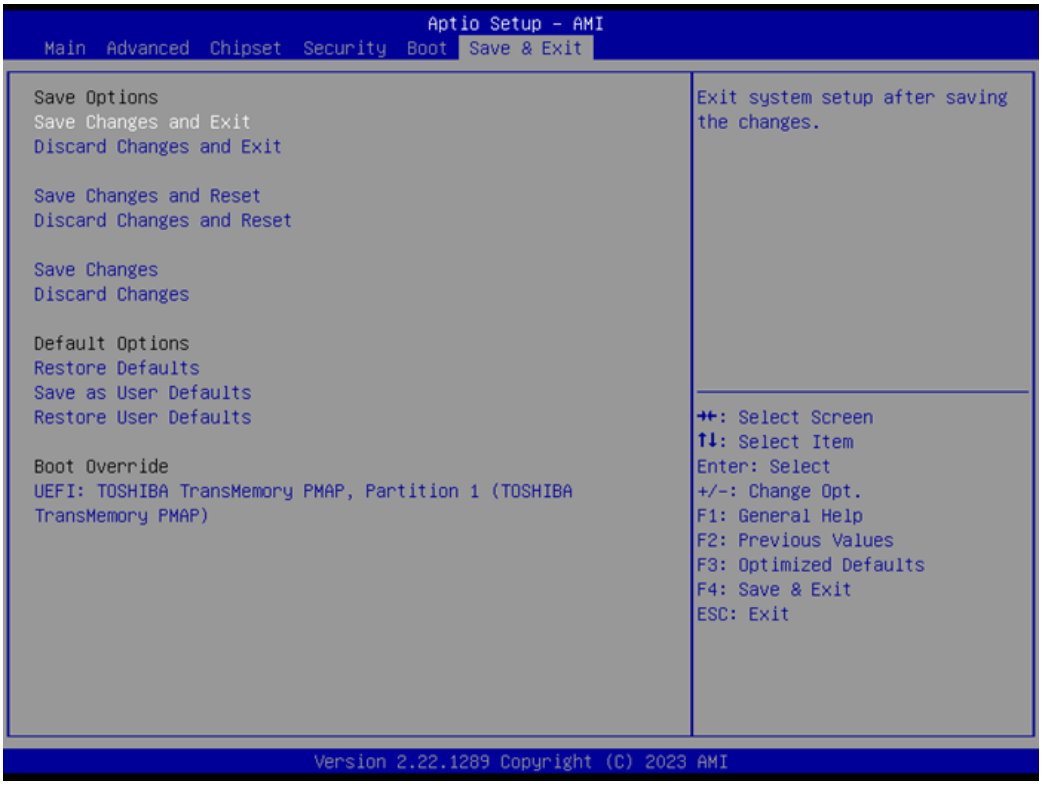

Figure 4.49

- **Save Changes and Exit**
  This item allows you to exit system setup after saving the changes.
- **Discard Changes and Exit**
  This item allows you to exit system setup without saving any changes.
- **Save Changes and Reset**
  This item allows you to reset the system after saving the changes.
- **Discard Changes and Reset**
  This item allows you to reset system setup without saving any changes.
- **Save Changes**
  This item allows you to save changes done so far to any of the options.
- **Discard Changes**
  This item allows you to discard changes done so far to any of the options.
- **Restore Defaults**
  This item allows you to restore/load default values for all the options.
- **Save as User Defaults**
  This item allows you to save the changes done so far as user defaults.
- **Restore User Defaults**
  This item allows you to restore the user defaults to all the options.
- **Boot Override**
  Boot device select can override your boot priority.

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Appendix A

System Assignments

This appendix contains information of a detailed nature.

Sections include:

- System I/O Ports
- 1st MB Memory Map
- Interrupt Assignments

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A.1 System I/O Ports

Table A.1: System I/O Ports	
Addr. Range (Hex)	**Device**
00h-1Fh	DMA Controller
20h-2Dh	Interrupt Controller
2Eh–2Fh	Motherboard resources
30h-3Dh	Interrupt Controller
40h-43h	Timer/Counter
4Eh–4Fh	Motherboard resources
50h-53h	Timer/Counter
60h-6Fh	8042 (keyboard controller) / NMI Controller / Microcontroller
70h-7Fh	Real-Time Controller
80h-8Fh	Debug Port / Reserved
90h-9Fh	Debug Port / Reset Generator
A0h-ADh	Interrupt Controller
B0h-B1h	Interrupt Controller
B4h-BDh	Power Management
220h-227h	Communications Port (COM5)
228h-22Fh	Communications Port (COM6)
290h-29Fh	HW Monitor Index Port and Data Port
2E8h-2EFh	Communications Port (COM4)
2F8h-2FFh	Communications Port (COM2)
3E8h-3EFh	Communications Port (COM3)
3F8h-3FFh	Communications Port (COM1)
480h-4CFh	Motherboard Resources
4D0h-4D1h	Interrupt Controller
680h-69Fh	Motherboard Resources
A00h-AFFh	Motherboard Resources
164Eh-164Fh	Motherboard Resources
1800h-18FFh	Motherboard Resources
CF9h-CF9h	Reset Generator

A.2 DMA Channel Assignments

Table A.2: DMA Channel Assignments	
Channel	**Function**
0	Available
1	Available
2	Available
3	Available
4	Direct memory access controller
5	Available
6	Available
7	Available

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A.3 1st MB Memory Map

Table A.3: 1st MB Memory Map	
Addr. Range (Hex)	**Device**
E0000h - FFFFFh	System board
D0000h - DFFFFh	PCI Bus
C0000h - CFFFFh	System board
A0000h - BFFFFh	PCI Bus
A0000h - BFFFFh	Intel® HD Graphics
00000h - 9FFFFh	System board

A.4 Interrupt Assignments

Table A.4: Interrupt Assignments	
Interrupt#	**Interrupt source**
NMI	Parity error detected
IRQ0	System Timer
IRQ1	Using SERIRQ, Keyboard Emulation
IRQ2	Interrupt from Controller 2 (cascade)
IRQ3	Communications Port (COM2)
IRQ4	Communications Port (COM1)
IRQ5	Communications Port (COM3)
IRQ6	Reserved
IRQ7	Communications Port (COM4)
IRQ8	System CMOS / Real Time Clock
IRQ9	Microsoft ACPI-Compliant System
IRQ10	Communications Port (COM5)
IRQ11	Communications Port (COM6)
IRQ12	Available
IRQ13	Numeric Data Processor
IRQ14	Reserved
IRQ15	Reserved

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