iPac-9x25

User Manual

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(For use with Rev. 2.0 boards or newer)

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1 Introduction

This document describes EMAC's iPac-9x25 Single Board Computer (SBC) module. The iPac-9x25 is a Headless (no video) PC/104 SBC sized module that provides a wide variety of I/O. Controlled by Atmel's powerful SAM9x25 processor, this module provides maximum flexibility with ample processing speed for most control applications. Although being extremely powerful with ample I/O for demanding applications, this board consumes minimal power, low cost, and has a small footprint. The iPac-9x25 uses the Standard PC/104 form factor (3.8" x 3.5") allowing the use of standard PC/104 mounting hardware and enclosures. Note: while the iPac-9x25 uses the PC/104 physical format it does not provide a PC/104 bus and therefore will not work with most PC/104 peripheral modules. The features of the iPac-9x25 are as follows:

1.1 Features

- **Atmel AT91SAM9X25 400MHz Processor**
- **16MB of Serial Flash**
- **128MB DDR2 of RAM**
- **4GB of eMMC Flash**
- **2x 10/100 Base-T Ethernet**
- **4x USB 2.0 Ports (2x High-Speed Host, 1x Full-Speed Host, 1x High-Speed OTG Host/Device)**
- **4x Serial Ports (3x RS232, 1x RS232/422/485)**
- **20x General Purpose SAM9X25 Digital I/O Lines, 16x SPI I/O Expander Based Digital I/O**
- **8x High Drive Digital Outputs**
- **1x microSD Card Slot**
- **1x CAN 2.0b Port**
- **SAM9x25 SPI, I2C and I2S**
- **Battery-Backed Real-Time Clock/Calendar**
- **Up to 4x 16-bit Pulse Width Modulation (PWM)**
- **7x A/D Channels with 10-bit A/D Converter - 0 to 2.5V Range8x Status LEDs**
- **Wide Temperature -40° to +85° C**

2 Hardware

2.1 Specifications

- **CPU:** Atmel AT91SAM9x25 ARM926EJ-S 400 MHz Processor/133 MHz System Bus/JTAG
- **Flash:** 4GB eMMC Flash and 16MB of Serial Data Flash
- **RAM:** 128MB DDR2 RAM
- **Flash Disk:** MMC/uSD Flash Disk socket
- **System Reset:** External Reset Button provision
- **RTC:** Battery-Backed Real-Time Clock/Calendar
- **PWM:** Up to 4, 16-bit PWMs
- **Watchdog Timer:** External Watchdog Timer (MAX6747)
- **Digital I/O:**
  - 20x General Purpose SAM9x25 Digital I/O lines
    - 20 programmable, SAM9x25 based, General Purpose TTL level I/O lines that can be configured as inputs or outputs. When configured as inputs, a 3.3-volt high input voltage is to be used and when configured as outputs, they have a sink/source drive capability of 8 mA.
  - 16x SPI I/O Expander Based Digital I/O lines; sink/source drive capability of 25 mA.
  - 8x High Drive Digital Outputs
    - The 8 open collector High-Drive Digital outputs with 500 mA. sink drive capability have a maximum total I/O drive of 1500 mA for these 8 lines.
- **Analog I/O:** Up to 7 channels of 10-bit A/D, 0 – 2.5 volts
  - 7 analog inputs are multiplexed into a 10-bit A/D converter with Sample & Hold and a conversion time of 2.2 uS. An additional settling time may be required when switching between channels. The analog input voltage range for each channel is 0 – 2.5 Volts.
- **Power:** Barrel jack connector or 4 Pin Supply Header
- **JTAG:** JTAG debugger capability

Serial Interfaces

- **UARTS:** 3x RS232 (1x w/full handshaking, 2x w/TX and RX only), 1x RS232/422/485
- **CAN:** 1x CAN 2.0b Port
- **SPI:** 1x SPI port
- **Audio:** 1x I2S Audio Port
- **USB:** 4x USB 2.0 Ports
  - 2x High-Speed Host
  - 1x Full-Speed Host
  - 1x High-Speed OTG Host/Device
- **I2C:** 1x I2C Port

Ethernet Interface

- **MAC:** AT91SAM9x25 on chip MACs
- **PHY:** Microchip Technology KSZ8041 PHYs
- **Interface:** On-Board 2-Port RJ-45 Connector

On-Board Options

- **Memory:** Up to 16GB of eMMC Flash
- **Software**: Linux

Other Options

- **PCD-39E00 Terminal Board:** Screw Terminal Board allows for easy access to the iPac-9x25 I/O. Up to two Screw Terminal Boards can be stacked onto a single iPac-9x25.

Mechanical and Environmental

- **Dimensions:** 3.77" L x 3.54" W (96mm x 90mm)
- **Power Supply Voltage:** 5 volt regulated +/- 5% DC board input voltage
- **Current Requirements:** (@ 5 Volts with no USB devices connected)
  - 295 mA during boot
  - 200 mA idle without Ethernet enabled
  - 235 mA idle with Ethernet enabled
  - APM Sleep (TBD)
- **Operating Temperature:** -40 ~ 85° C (-40 ~ 185 ° F), fanless operation
- **Operating Humidity:** 0% ~ 90% relative humidity, non-condensing

2.2 Jumper Configuration & Connector Descriptions

The iPac-9x25 comes factory configured. In the event that jumpers need to be verified or modified this section provides the information required, including instructions on setting jumpers and connecting peripherals, switches and indicators. Be sure to read all the safety precautions before you begin any configuration procedure. See Appendix A for connector pinouts and Appendix B for Jumper Setting descriptions.

Table 1: Jumpers

Pin#	Function	Default
JB1	5/12 Volt Open Collector Output Selection	5V
JB2	Open Collector Voltage Selection	3.3V/3.3V
JB3	RTC Battery	Off
JB4	Flash Enable	SFE
JB5	RS4XX Termination	OPN
JB7	ADC REF	2.5V

JB1 & JB2 Jumper Settings

JB2 controls the pull-up voltage of the open collector High Drive Output lines and determines what voltage is present on pin 50 of HDR6. One side of the jumper (VIO) controls pin 50 and the other side (VPU) controls the High Drive pull-up voltage. Leaving the VIO shunt off leaves pin 50 open and leaving the VPU shunt off sets the High Drive Outputs to no pull-up voltage (open collector). The voltage at the SEL2 pins is defined by JB1. The default position for the jumpers on JB2 are 1 & 3 and 2 & 4. The default jumper position sets the open collector output pull ups of Port X and the output voltage on Pin 50 of HDR6 to 3.3V. Note pin1 of JB1 (Vin) is fed from pin 4 (Vin) of the power connector CN2. While the Vin power input is typically fed by 12Vdc it can also be fed higher voltages in order to offer Port X compatibility with higher voltage systems such as 24V.

Pull-up Voltage

I/O Header (HDR6, pin 50) Voltage Selection & High Drive Pull-up Selection Jumper. See schematic below for the jumper block pin numbers.

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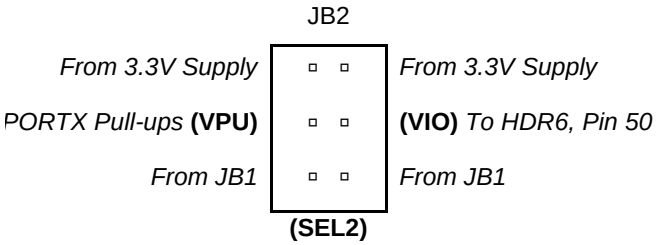


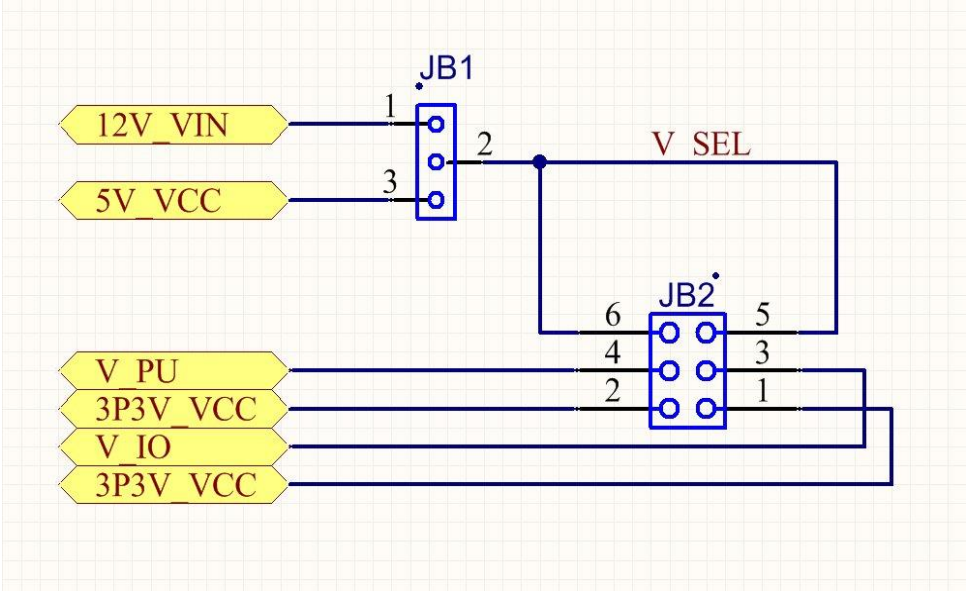


Table 2: Connectors

Label	Function
JK1	Dual USB Host Port
JK2	USB Host/Device Port
JK3	Dual Port Ethernet Connector
JK4	Vin Barrel Power Jack Connector
HDR1	RS232 Debug (UART) 10-pin Header
HDR2	JTAG 10-pin Header
HDR3	CAN 3-pin Header
HDR4	(UART0) 10-pin Header
HDR5	Misc. I/O 40-pin Header
HDR6	GPIO 50-pin Header
HDR7	Processor-Based GPIO 50-Pin Header
HDR8	RS232 Serial (UTXD0/URXD0) 10-pin Header
HDR9	USB Host Bulkhead 10-pin Header
CN1	RS232 Serial (UART3) 9-Pin D-Sub Connector
CN2	Alternate 4-pin Power Connector
SOK1	MMC/uSD Flash Card Socket

2.3 Power Connectors

The iPac-9x25 provides a keyed locking alternate power connector that lends itself more to industrial applications located at CN2 that has an operating temperature of -55 ~ 105° C. Pin #4 of CN2 is referred to as Vin. This pin is routed exclusively to JB1 pin #1 as a jumper option. The Vin power input can handle up to 24V for interfacing the iPac-9x25 with industrial equipment.

There is also a standard barrel type power jack that can be used to provide 5 volt regulated power located at JK4 and has an inner diameter of 2.1mm with a center V+ connection and has an operating temperature of -25 ~ 85° C. This jack allows for easy connection to a wall mount power supply (EMAC part number PER-PWR-00035).

Table 3: Alternate Power Connector (CN2)

Pin#	Signal
1	+5 Volt Regulated
2	GND
3	GND
4	12V_Vin* (Can support 3.3V – 34V)

* This pin is routed exclusively to JB1 pin #1 as a jumper option

2.4 Real-Time Clock

The iPac-9x25 processor is equipped with an internal, ultra-low power Real-Time Clock (RTC). The SAM9x25 processor provides an internal RTC and a 200-year Gregorian calendar with programmable periodic interrupt. This RTC is battery backed by on-board battery located at B1. JB3 provides the ability to disconnect the battery from the RTC.

2.5 Watchdog Timer

The iPac-9x25 is equipped with an external watch dog timer (MAX6747) that provides a time out of approximately 1.4 seconds. The watch dog timer is disabled by default and can be enabled by writing PC7 low. The watch dog timer is then pulsed by using PC6.

2.6 JTAG (HDR2)

This multipurpose header (HDR2) provides JTAG debugging interface directly to the Processor. HDR2's pinout is a derivation of the standard 10 pin JTAG header with the added pins (6 & 8) used for a SAM-ICE in circuit emulator. A special cable is required to connect the SAM-ICE to HDR2. Note: be careful to check for pin-out compatibility with your JTAG device.

Table 4: JTAG and BDM Interface (HDR2)

Pin#	Signal	Description
1	JTAG_TCK	JTAG Clock
2	GND	Ground
3	JTAG_TDO	JTAG Serial Out
4	3.3.V_VCC	3.3 Volts
5	JTAG_TMS	JTAG Operation Mode
6	NRST	Microcontroller Reset
7	RTCK	Return Test Clock
8	JTAG_NTRST	Test Reset Signal
9	JTAG_TDI	JTAG Serial In
10	GND	Ground

2.7 Processor-Based General-Purpose Digital I/O (HDR7)

These GPIO lines are for the most part exactly that, general purpose. Of these lines, 20 are connected directly to the processor (so use caution when interfacing to these lines). The names of each line listed in Table 5 matches the port line on the SAM9x25 processor. Each can be configured as input or output with/without internal pull-ups through software. Many of these lines have alternate multiplexed functionality that can be utilized by configuring the processor in software and connecting to the appropriate lines.

When using these processor lines as outputs, these lines can drive 5 mA. When used as inputs, the input voltage should not exceed 3.3 Vdc or go below ground.

Table 5: Processor Based Digital I/O Connector (HDR7)

Pin#	Signal	Pin#	Signal
1	GND	**2**	PD0
3	GND	**4**	PD1
5	GND	**6**	PD2
7	GND	**8**	PD3
9	GND	**10**	PD4
11	GND	**12**	PD5
13	GND	**14**	PD6
15	GND	**16**	PD7
17	GND	**18**	PD8
19	GND	**20**	PD9
21	GND	**22**	PD10
23	GND	**24**	PD11
25	GND	**26**	PD12
27	GND	**28**	PD13
29	GND	**30**	PD14
31	GND	**32**	PD15
33	GND	**34**	PD16
35	GND	**36**	PD17
37	GND	**38**	PD18
39	GND	**40**	PD19
41	GND	**42**	+3.3V
43	GND	**44**	+3.3V
45	GND	**46**	+3.3V
47	GND	**48**	+3.3V
49	GND	**50**	+5V

2.8 General Purpose Digital I/O (HDR6)

These input and output lines provide connections for heavier industrial relays and switches. They are connected to the SPI I/O Expander chip on the iPac. There are 24 port lines in all and are broken up into three 8-bit ports (X, Y, & Z). Port Y and Z can be programmed as input or output ports and X is an open collector high drive output port. When using Port Y and Z as inputs, the input voltage should not exceed 3.3 Vdc or go below ground and as such define a high as any voltage above 1.65 volts (half of the 3.3V Vdd). When used as an Output Port, Y and Z port lines can drive up to 25 mA loads.

The high-drive output port PY1 – PY8 has an open-collector output driver chip (ULN2803) with 500 mA sink drive capability per line and a maximum total package current of 1500 mA. The open-collector output lines can provide a high-level voltage through the use of the pull-up resistors selectable by Jumper JB1. The fly-back diodes in the ULN2803 will be tied to the same voltage selected by JB1.

Table 6: Extended Digital I/O Connector (HDR6)

Pin#	Signal	Pin#	Signal
1	GND	**2**	PX1
3	GND	**4**	PX2
5	GND	**6**	PX3
7	GND	**8**	PX4
9	GND	**10**	PX5
11	GND	**12**	PX6
13	GND	**14**	PX7
15	GND	**16**	PX8
17	GND	**18**	PY1
19	GND	**20**	PY2
21	GND	**22**	PY3
23	GND	**24**	PY4
25	GND	**26**	PY5
27	GND	**28**	PY6
29	GND	**30**	PY7
31	GND	**32**	PY8
33	GND	**34**	PZ1
35	GND	**36**	PZ2
37	GND	**38**	PZ3
39	GND	**40**	PZ4
41	GND	**42**	PZ5
43	GND	**44**	PZ6
45	GND	**46**	PZ7
47	GND	**48**	PZ8
49	GND	**50**	(see JB1 options)

2.9 SPI GPIO Expansion ICs

All of the general-purpose digital I/O on HDR6 is derived from three SPI GPIO expansion ICs (MCP23S08). Each of the three 8-bit ports are controlled by a GPIO expansion IC. All share a common chip select, SPI0_CS1, and are assigned a unique address for each specific IC. For specific data regarding the GPIO expansion ICs please refer to Microchips datasheet for the device.

Table 7: GPIO Port SPI Addresses

Port	Address
PX	0x00
PY	0x02
PZ	0x01

2.10 Analog Channels & PWMs (HDR5)

The SAM9x25 processor on the iPac-9x25 has a 10-bit, 12 channel A/D module which provides lines AD0 – AD6. These lines can accept signals in the range of 0 to 2.5 Volts. The iPac-9x25 has an internal 2.5v reference for the A/D voltage reference. The internal regulator can be disabled by writing a 1 to PD21 in order to reduce power consumption.

In addition to the A/D, the iPac-9x25 provides 4 PWM channels which drive at 3.3V. PWM channels 2 and 3 are shared with the A/D inputs AD2 and AD3. Each of the 4 PWM channels has its own 16-bit counter with the ability to select from 13 different clock signals.

In addition to the A/D and PWMs on HDR5, there are a number of processor specific I/O lines such as SPI, I2S, I2C, and GPIO. The SPI has two chip select lines available.

Table 8: Miscellaneous I/O (HDR5)

Pin#	Signal	Pin#	Signal
1	AD0 / PWM0 / PB11	**2**	AD1 / PWM1 / PB12
3	AD2 / PWM2 / PB13	**4**	AD3 / PWM3 / PB14
5	AD4 / PB15	**6**	AD5 / PB16
7	AD6 / PB17	**8**	PWM0 / PC10
9	I2C0_CLK / SPI1_CS2# / PA31	**10**	PWM1 / PC11
11	I2C0_DAT / SPI1_CS3# / PA30	**12**	SPI1_SPCK / PA23
13	SPI1_MOSI / PA22	**14**	SPI1_MISO / PA21
15	3.3 Vdc	**16**	3.3 Vdc
17	GND	**18**	GND
19	SSC_TF / PA25	**20**	SSC_RK / PA28
21	GND	**22**	GND
23	3.3 Vdc	**24**	3.3 Vdc
25	SSC_TK / PA21	**26**	SSC_RD / PA27
27	GND	**28**	GND
29	SSC_TD / PA26	**30**	SSC_RF / PA29
31	3.3 Vdc	**32**	3.3 Vdc
33	I2C1_DAT / PC0	**34**	I2C1_CLK / PC1
35	RST_OUT#	**36**	RST_IN#
37	GND	**38**	GND
39	5V_VCC	**40**	5V_VCC

2.11 RS232 SERIAL UART3 (CN1)

The iPac-9x25 provides one dedicated RS232 UART3 serial port which has software configurable baud rates. Both transmission and asynchronous data reception are possible. Handshake Lines are implemented by the use of the processors GPIO lines (with the exception of CTS & RTS which are true handshake lines) and thus software is required to utilize these lines as handshake lines. Serial UART 3 is connected to a DB-9 male pin connector on the iPac-9x25.

Table 9: RS232 UART3 (CN1)

Pin#	Signal
1	DCD
2	RXD
3	TXD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI
10	NC

2.12 RS232/422/485 SERIAL UART0 (HDR4)

The iPac-9x25 provides one software selectable RS232/422/485 UART which has software configurable baud rates. Both transmission and asynchronous data reception are possible. RS232 Handshake Lines (CTS & RTS) are provided by the processor's UART0. Hardware logic is provided to prevent the RS422/485 TX driver from being enabled at the same time as the RS232 driver.

Table 10: RS232/422/485 UART0 (HDR4)

Pin#	RS-232 Signal	RS-485/422 Signal
1	NC	TX-
2	NC	NC
3	RXD	TX+
4	RTS	NC
5	TXD	RX+
6	CTS	NC
7	NC	RX-
8	NC	NC
9	GND	GND
10	NC	NC

Table 10.1 below shows the control logic to select between RS232/RS422/RS485. The function of the serial port is controlled by processor port lines PC17, PA4, and PC26.

Table 10.1: RS232/422/485 Software Configuration

Transmitter/Receiver Configuration	Processor Port PC17	Processor Port PA4	Processor Port PC26
OFF	1	0	0
RS232	1	0	1
RS422	1	1	0
RS485	0	1	0

2.13 RS232 Serial (UTXD0/URXD0) (HDR8)

The iPac-9x25 provides two RS232 serial UARTs that supply TX and RX signals only. UART0 is terminated to a 10-pin header for easy access.

Table 11: RS232 COM2 (HDR8)

Pin#	Signal
1	NC
2	NC
3	RXD
4	NC
5	TXD
6	NC
7	NC
8	NC
9	GND
10	NC

2.14 RS232 Debug Serial UART (HDR1)

The iPac-9x25 provides two RS232 serial UARTs that supply TX and RX signals only. The debug UART is terminated to a 10-pin header for easy access.

Table 12: RS232 Debug (HDR1)

Pin#	Signal
1	NC
2	NC
3	RXD
4	NC

5	TXD
6	NC
7	NC
8	NC
9	GND
10	NC

2.15 CAN Bus (HDR3)

The iPac-9x25 provides a CAN bus interface through a 3-pin header HDR3. The on-processor CAN controller provides all the features required to implement the serial communication protocol. CAN1 of the processor is used for the external CAN interface. The CAN port is able to achieve bit rates up to 1 Mbits/s and complies with CAN 2.0 Part A and 2.0 Part B.

Table 13: CAN Bus (HDR3)

Pin#	Description
1	CANH
2	CANL
3	GND

2.16 Ethernet (JK3)

The iPac-9x25 comes equipped with two 10/100 BaseT Ethernet ports terminated to a standard RJ45 jack. The iPac-9x25 can be connected directly (point to point) to a PC with the use of a crossover Ethernet cable. To connect the iPac-9x25 to a switch or a hub, use a standard Ethernet cable.

The Ethernet MACs are provided internally within the processor. The PHYs are external to the processor and are implemented using a Microchip Technology KSZ8041 PHY chip. The PHY is a relatively power-hungry chip and as such the 50MHz oscillator can be powered down via PC12 in order to conserve power. Shutting off the oscillator will disable both Ethernet PHYs.

2.17 Dual USB Host (JK1)

The iPac-9x25 provides two USB 2.0 Hi-Speed (480 Mbits/Sec) Host ports. The High-Speed ports are also capable of Full-Speed operation and are backwards compatible with USB 1.1 devices. USB devices (printer, mouse, keyboard, camera, etc.) and hubs can be connected to the USB Host in the USB tiered-star topology.

The specification for standard USB states that each USB port be capable of providing 5 volts at 500 mA. This provision is strictly dependent on the power supply used with the iPac. Obviously, the power supply must be able to source 5 volts at 1 amp for the USB requirement in addition to the other power requirements of the board. A 500 mA polyfuse protects each USB port from over-current damage. There is no provision to turn off power to the USB host ports.

2.18 USB Host/Device (JK2)

The iPac-9x25 provides one High-Speed USB 2.0 Host/Device port. When using the iPac as a device, the iPac must be powered independently as it cannot use the USB Device Port for power. When the High-Speed host port is utilized the USB bus power can be switched on by writing a 1 to PC13. The USB bus power and current protection are supplied by a MIC2506YM power management IC. The over current signal is supplied to the processor through PB8. The USB bus power is off by default so in order to use the Host function the USB power will need to be enabled.

2.19 USB Host Bulkhead Connector (HDR9)

The iPac-9x25 provides an additional Full-Speed USB host port and access to one of the High-Speed host ports provided through JK1. The USB bulkhead connector allows a Full-Speed port and shares the High-Speed port that is routed to the top USB port of JK1 to be available via a 10-pin header. Both USB ports provided through the bulkhead connector are capable of sourcing up to 500mA of current at 5V and are protected from over current by a resettable polyfuse.

Table 14: USB Bulkhead Connector (HDR9)

Pin#	Signal
1	FS Host VBUS
2	HS Host VBUS
3	FS Host Data-
4	HS Host Data-
5	FS Host Data+
6	HS Host Data+
7	GND
8	GND
9	NC
10	Key

2.20 MMC/SD Flash Card Socket (SOK1)

The iPac-9x25 provides standard Micro SD type socket, which accepts uSD cards. This Socket is connected to a USB to MMC Bridge controller USB266i.

2.21 Serial Flash

Also equipped on some models is 16MB Bytes of SPI based Serial Flash. The Serial Flash is usually used to store the boot loader and/or operating system. The iPac-9x25 can also be configured to boot from the eMMC or Micro SD card. By default, the iPac-9x25 is configured to boot from the serial flash. This can be controlled with JB4 to force the processor to use its internal boot ROM or enter the serial downloader mode. See the section describing JB4 for further details.

2.22 Module Status LEDs and Reset

The iPac-9x25 is equipped with multiple status LEDs and are listed below in Table 15. The iPac-9x25 is also equipped with a reset button located at PB1. Pressing this button will cause the system to reset.

Table 15: Status LEDs

Location	Description
LD1-8	High drive open collector output indicator LEDs.
LD9	Power indicator LED. Indicates that on-board 3.3v regulator is functioning.
LD10	General Purpose Green Status LED controlled by processor GPIO (PD20) pin. This is a user programmable LED.
LD11	uSD Activity LED

3 Software

The iPac-9x25 offers a wide variety of software support from both open source and proprietary sources. The hardware core utilizes the AT91SAM9x25, which is supported by Linux.

For more information on Linux Software Support, please visit the EMAC Wiki Software Section at:

http://wiki.emacinc.com/wiki/Product_wiki

3.1 Das U-Boot

EMAC utilizes Das U-Boot for its ARM based products. U-Boot is an open source/cross-architecture platform independent bootloader. It supports reading and writing to the flash, auto-booting, environmental variables, and TFTP. Das U-boot can be used to upload and run and/or reflash the OS or to run stand-alone programs without an OS. Products are shipped with valid MAC addresses installed in flash in the protected U-boot environmental variable "ethaddr". At boot time U-Boot automatically stores this address in a register within the MAC, which effectively provides it to any OS loaded after that point.

3.2 Embedded Linux

EMAC Open Embedded Linux (EMAC OE Linux) is an open source Linux distribution for use in embedded systems. The EMAC OE Linux Build is based on the Open Embedded (www.openembedded.org) and Yocto (www.yoctoproject.org) Linux build systems. Open Embedded is a superior Linux distribution for embedded systems. Custom Linux builds are also available on request.

The distribution contains everything a user could expect from a standard Linux kernel: powerful networking features, advanced file system support, security, debugging utilities, and countless other features.

The basic root file system includes:

- Busybox
- Hotplugging support
- APM utilities for power management
- Openssh SSH server
- lighttpd HTTP server
- EXT4 file system with utilities

3.2.1 Linux with PREEMPT RT

PREEMPT RT provides pseudo real time to the kernel and can be used to schedule tasks with hard deadlines and minimal latencies. The PREEMPT RT build is an option to the standard Linux build and is available for a one-time inexpensive support/installation fee.

3.2.2 Linux Packages

EMAC provides support for many Linux Packages such as: PHP, SQLite, Perl, SNMP, DHCP Server, etc. As with the PREEMPT RT Option, other Packages can be added to the standard Linux file system and are available for a one-time inexpensive support/installation fee.

3.2.3 Linux Patches

In addition to standard Embedded Linux support, EMAC has released a number of patches and device drivers from the open source community and from internal EMAC engineering into its standard distribution. Along with kernel patches, EMAC provides the binaries for the kernel and root file system.

3.3 Qt Creator

Qt Creator is a cross-platform IDE (Integrated Development Environment) tailored to the needs of Qt developers but works well for Headless applications as well. EMAC provides sample code as projects that can be imported into Qt Creator. Qt Creator supports remote deployment and source debugging.

http://wiki.qt.io/Main

3.4 ARM EABI Cross Compiler

The popular open source gcc compiler has a stable build for the ARM family. EMAC uses the 4.9.1 version of the ARM EABI compiler. The Embedded Linux kernel and EMAC Qt Creator projects use this compiler for building ARM stand alone, and OS specific binaries. The EMAC Qt Creator provides source level debugging over Ethernet or serial using gdbserver. The Linux binaries for the ARM EABI cross compiler are available online along with the SDK. See the EMAC wiki for further information.

4 Appendix A: Connector Pinouts

4.1 JK1 - Dual USB Host Port

Pin#	Signal
T1	USB_2_VCC
T2	USB_2_N
T3	USB_2_P
T4	GND
9	FRM_GND
10	FRM_GND
11	FRM_GND
12	FRM_GND
B1	USB_3_VCC
B2	USB_3_N
B3	USB_3_P
B4	GND

4.2 JK2 - USB Host/Device Port

Pin#	Signal
1	USB3_VCC
2	USB3_N
3	USB3_P
4	USB_OTG_ID
5	GND
6	FRM_GND
7	FRM_GND

4.3 JK3 - Dual Port Ethernet Connector

Pin#	Signal
T1	GND
T2	E0_TX_P
T3	E0_TX_N
T4	E0_RX_P
T7	E0_RX_N
T11	3P3V_VCC
T12	E0_ACT1#
T13	E0_LINK#
T14	3P3V_VCC
B1	GND
B2	E1_TX_P
B3	E1_TX_N
B4	E1_RX_P
B7	E1_RX_N
B11	3P3V_VCC

B12	E1_ACT1#
B13	E1_LINK#
B14	3P3V_VCC

4.4 JK4 - Vin Barrel Power Jack Connector

Pin#	Signal
1	Vin
2	GND
3	NC

4.5 HDR1 - RS232 Debug (UART) 10-pin Header

Pin#	Signal
1	NC
2	NC
3	RXD
4	NC
5	TXD
6	NC
7	NC
8	NC
9	GND
10	NC

4.6 HDR2 - JTAG 10-pin Header

Pin#	Signal	Description
1	JTAG_TCK	JTAG Clock
2	GND	Ground
3	JTAG_TDO	JTAG Serial Out
4	3.3.V_VCC	3.3 Volts
5	JTAG_TMS	JTAG Operation Mode
6	NRST	Reset
7	RTCK	Return TCK
8	JTAG_NTRST	Test Reset Signal
9	JTAG_TDI	JTAG Serial In
10	GND	Ground

4.7 HDR3 - CAN 3-pin Header

Pin#	Description
1	CANH
2	CANL
3	GND

4.8 HDR4 - UART0 10-pin Header

Pin#	RS-232 Signal	RS-485/422 Signal
1	NC	TX-
2	NC	NC
3	RXD	TX+
4	RTS	NC
5	TXD	RX+
6	CTS	NC
7	NC	RX-
8	NC	NC
9	GND	GND
10	NC	NC

4.9 HDR5 - Misc. I/O 40-pin Header

Pin#	Signal	Pin#	Signal
1	AD0 / PWM0 / PB11	**2**	AD1 / PWM1 / PB12
3	AD2 / PWM2 / PB13	**4**	AD3 / PWM3 / PB14
5	AD4 / PB15	**6**	AD5 / PB16
7	AD6 / PB17	**8**	PWM0 / PC10
9	I2C0_CLK / SPI1_CS2# / PA31	**10**	PWM1 / PC11
11	I2C0_DAT / SPI1_CS3# / PA30	**12**	SPI1_SPCK / PA23
13	SPI1_MOSI / PA22	**14**	SPI1_MISO / PA21
15	3.3 Vdc	**16**	3.3 Vdc
17	GND	**18**	GND
19	SSC_TF / PA25	**20**	SSC_RK / PA28
21	GND	**22**	GND
23	3.3 Vdc	**24**	3.3 Vdc
25	SSC_TK / PA21	**26**	SSC_RD / PA27
27	GND	**28**	GND
29	SSC_TD / PA26	**30**	SSC_RF / PA29
31	3.3 Vdc	**32**	3.3 Vdc
33	I2C1_DAT / PC0	**34**	I2C1_CLK / PC1
35	RST_OUT#	**36**	RST_IN#
37	GND	**38**	GND
39	5V_VCC	**40**	5V_VCC

4.10 HDR6 - GPIO 50-pin Header

Pin#	Signal	Pin#	Signal
1	GND	**2**	PX1
3	GND	**4**	PX2
5	GND	**6**	PX3
7	GND	**8**	PX4
9	GND	**10**	PX5
11	GND	**12**	PX6
13	GND	**14**	PX7

15	GND	**16**	PX8
17	GND	**18**	PY1
19	GND	**20**	PY2
21	GND	**22**	PY3
23	GND	**24**	PY4
25	GND	**26**	PY5
27	GND	**28**	PY6
29	GND	**30**	PY7
31	GND	**32**	PY8
33	GND	**34**	PZ1
35	GND	**36**	PZ2
37	GND	**38**	PZ3
39	GND	**40**	PZ4
41	GND	**42**	PZ5
43	GND	**44**	PZ6
45	GND	**46**	PZ7
47	GND	**48**	PZ8
49	GND	**50**	(see JB1 options)

4.11 HDR7 - Processor-Based GPIO 50-Pin Header

Pin#	Signal	Pin#	Signal
1	GND	**2**	PD0
3	GND	**4**	PD1
5	GND	**6**	PD2
7	GND	**8**	PD3
9	GND	**10**	PD4
11	GND	**12**	PD5
13	GND	**14**	PD6
15	GND	**16**	PD7
17	GND	**18**	PD8
19	GND	**20**	PD9
21	GND	**22**	PD10
23	GND	**24**	PD11
25	GND	**26**	PD12
27	GND	**28**	PD13
29	GND	**30**	PD14
31	GND	**32**	PD15
33	GND	**34**	PD16
35	GND	**36**	PD17
37	GND	**38**	PD18
39	GND	**40**	PD19
41	GND	**42**	+3.3V
43	GND	**44**	+3.3V
45	GND	**46**	+3.3V
47	GND	**48**	+3.3V
49	GND	**50**	+5V

4.12 HDR8 - RS232 Serial (UTXD0/URXD0) 10-pin Header

Pin#	Signal
1	NC
2	NC
3	RXD
4	NC
5	TXD
6	NC
7	NC
8	NC
9	GND
10	NC

4.13 HDR9 - USB Host Bulkhead 10-pin Header

Pin#	Signal
1	FS Host VBUS
2	HS Host VBUS
3	FS Host Data-
4	HS Host Data-
5	FS Host Data+
6	HS Host Data+
7	GND
8	GND
9	NC
10	Key

4.14 CN1 - RS232 Serial (UART3) 10-pin Header

Pin#	Signal
1	DCD
2	RXD
3	TXD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI
10	NC

4.15 CN2 - Alternate 4-pin Power Connector

Pin	Signal
1	+5 Volt Regulated
2	GND
3	GND
4	12V_Vin* (Can support 3.3V – 34V)

4.16 SOK1 - MMC/SD Flash Card Socket

Pin#	Signal
1	SD2_D2
2	SD2_D3
3	SD2_CMD
4	3P3V_VCC
5	SD2_CLK
6	GND
7	SD2_D0
8	SD2_D1
9	CARD_DET
10	GND

5 Appendix B: Jumper Settings

5.1 JB1 (5/12 Volt Open Collector Output Selection)

Jumper	Position	Setting
Pins 1 & 2	12V	12V Selection
Pins 2 & 3*	5V	5V Selection

*Default Setting

5.2 JB2 (Open Collector Voltage Selection)

Jumper	Position	Setting
Pins 1 & 3*	3.3V	3.3V VIO to HDR6 (Pin-50)
Pins 3 & 5	5V or 12V	5V or 12V VIO to HDR6 (Pin-50)
Pins 2 & 4*	3.3V	3.3V VPU to PORTX Pull-Ups
Pins 4 & 6	5V or 12V	5V or 12V VPU to PORTX Pull-Ups

*Default Setting

5.3 JB3 (RTC Battery)

RTC Backup: RTC and Calendar battery Backup

Jumper	Position	Setting
Pins 1 & 2*	OFF	Disable Battery Backup
Pins 2 & 3	ON	Enable Battery Backup

*Default Setting

5.4 JB4 (Flash Enable)

Boot Select: Disables Serial Flash and Enables Boot from Internal ROM

Jumper	Position	Setting
Pins 1 & 2	SFD	Serial Flash Disable
Pins 2 & 3*	SFE	Serial Flash Enable

*Default Setting

5.5 JB5 (RS4XX Termination)

RS4XX Termination: Selects a Parallel 120 Ohm Termination Resistor on RX Pair.

Jumper	Position	Setting
Pins 1 & 2	TRM	Termination Resistor Present
Pins 2 & 3*	OPN	Termination Resistor Not Present

*Default Setting

5.6 JB7 (ADC REF)

ADC Reference Voltage: Selects Either 2.5V or 3.3V as the ADC Reference Voltage.

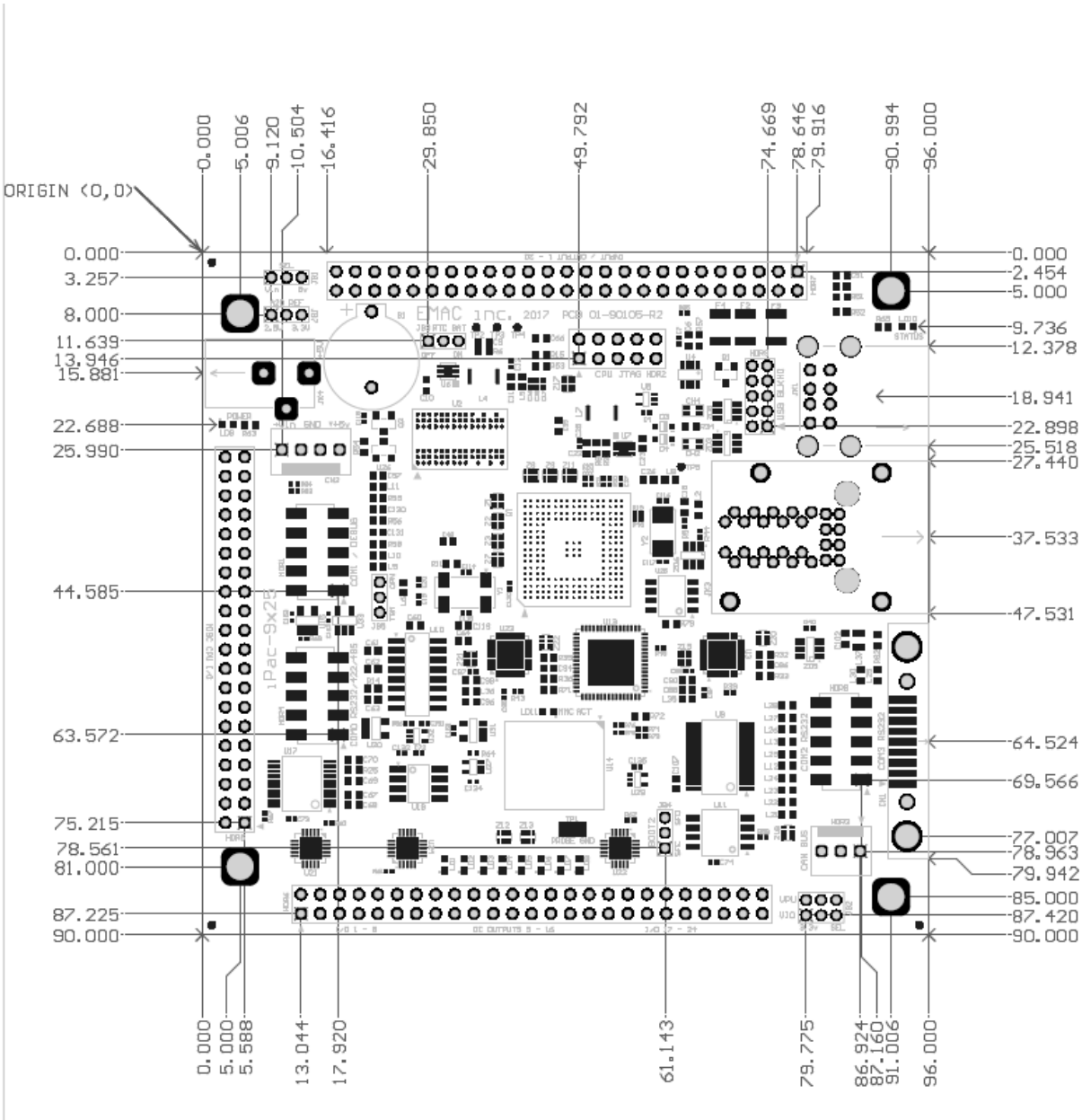
Jumper	Position	Setting
Pins 1 & 2	3.3V	3.3V Reference
Pins 2 & 3*	2.5V	2.5V Reference

*Default Setting

6 Dimensional Drawings

6.1 iPac-9x25 Header Locations

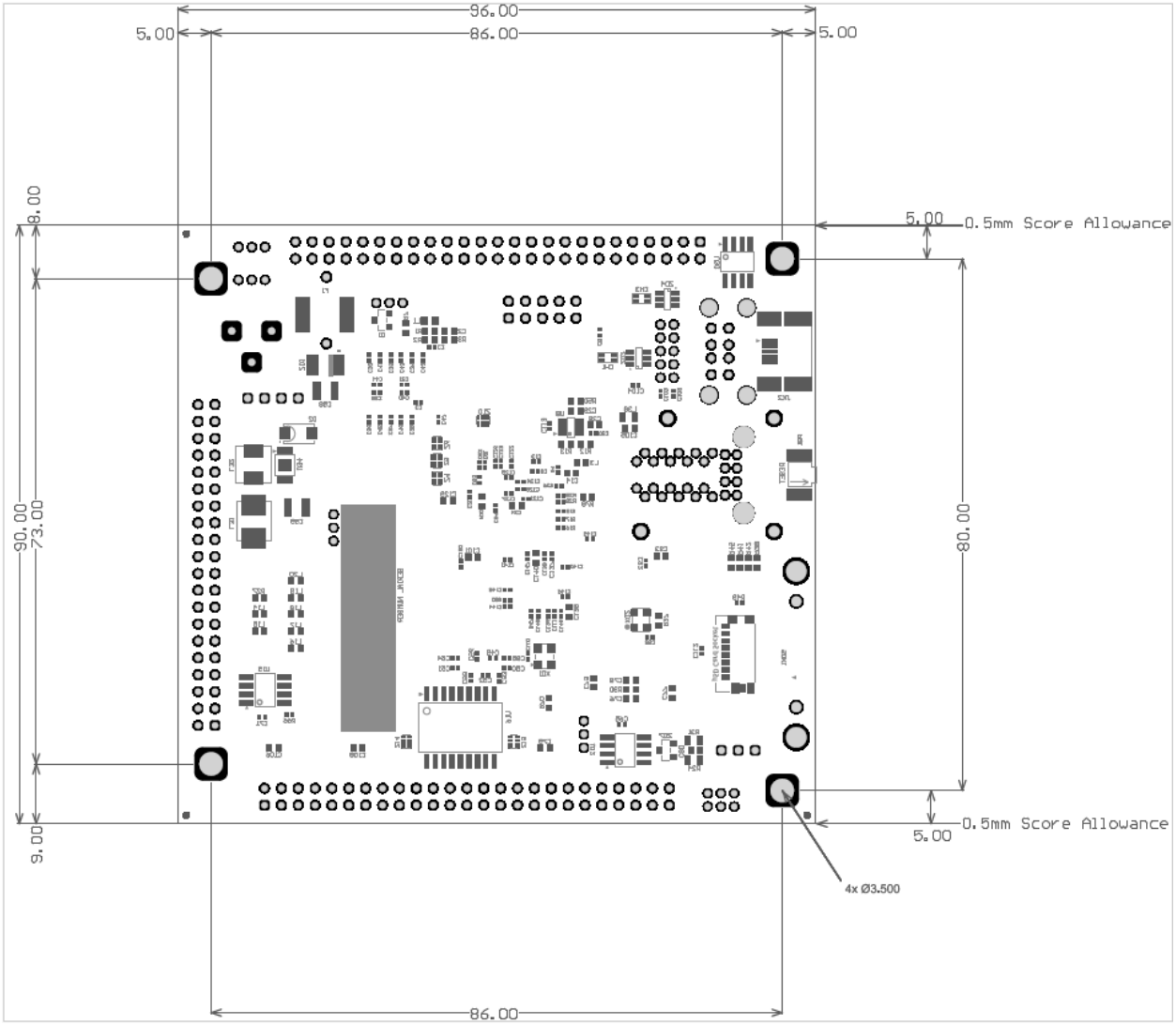
Drawing 1: Top Side Component Placement



*All units are shown in millimeters

6.2 iPac-9x25 Board Dimensions

Drawing 2: Bottom Side and Board Dimensions



*All units are shown in millimeters