iPac-35D1

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1 Introduction

This document provides an overview of EMAC's iPac-35D1 Single Board Computer (SBC). The iPac-35D1 is a high-performance, industrial-temperature SBC designed for Edge IIoT gateway applications. It is a web-enabled platform built on the Nuvoton NuMicro® MA35D1, featuring dual 64-bit Arm® Cortex®-A35 cores alongside a 180 MHz Arm® Cortex®-M4 core for real-time control.

Designed and manufactured in the USA by EMAC, Inc., the iPac-35D1 SBC is an ideal solution for IIoT Edge Gateway applications. This ARM64-based SBC can host an embedded web server or MQTT broker, enabling monitored or logged data to be delivered directly to end-user dashboards or cloud services.

The iPac-35D1 provides flexible connectivity, featuring both 1000Base-T Gigabit Ethernet and 10/100Base-T Ethernet ports, with optional support for 802.11 Wi-Fi modules. Powered by the Nuvoton NuMicro® MA35D1 System-on-Chip, it brings most all I/O connections out to header connectors while maintaining the compact PC/104 footprint (3.77" x 3.54").

The iPAC-35D1 is perfectly suited for IIoT Edge Gateway or Embedded Data Acquisition and Control applications where an Industrial Temperature operating range system is needed. Designed for high-end edge IIoT gateway systems, the IPAC-35D1 SBC provides multiple advanced and high-speed connection interfaces, such as Gigabit Ethernet, SDIO, USB 2.0, and CAN-FD, for edge gateway, HMI and new energy applications.

1.1 Features

- **High-end Edge IIoT Gateway ARM64 Single Board Computer**
- **NuvoTon MA35D1 Dual ARM Cortex A35 800MHz & 180Mhz Cortex M4 Processor**
- **16MB Serial Data Flash**
- **512MB DDR3L RAM**
- **4GB eMMC**
- **4x Serial ports**
- **1x CAN port**
- **2x USB 2.0**
- **36x General Purpose Digital I/O lines**
- **8x High Drive Digital Outputs.**
- **1x 10/100 BaseT Ethernet and 1x 10/100/1000 BaseT Gig Ethernet**
- **4x channels of 12-bit A/D**
- **32x 8-bit PWM Channels**
- **1x 12S External Port**
- **1x External I2C & 1x SPI External Port**
- **1x uSD Flash Disk socket**
- **External Reset Button provision**

2 Hardware

2.1 Specifications

- **CPU:** NuvoTon MA35D1 Dual ARM Cortex A35 800MHz Cores & 180Mhz Cortex M4 MCU
- **Flash:** 4GB of eMMC Flash and 16MB of Serial Data Flash
- **RAM:** 512MB of DDR3L RAM
- **System Reset:** External Reset Button provision
- **RTC:** Battery backed Real Time Clock
- **Digital I/O:**
  - 32x General Purpose Digital I/O (3.3V/5V Tolerant) Lines
  - 4x General Purpose Digital (3.3V) I/O lines
  - 8x High Drive Digital Outputs (Open Collect; 500mA Sink)
- **Analog I/O:**
  - 4x channels of 12-bit A/D (0 to 2.5V)
  - 32x PWM Channels (shared with GPIOs)
- **Power:** +5V board input voltage required

Serial Interfaces

- **UARTS:**
  - 1x RS232 serial DB9 port with full handshake
  - 2x RS232 serial ports with RTS/CTS handshake (10 pin header)
  - 1x RS232/485/422 serial port with RTS/CTS handshake (10 pin header)
- **SPI:** 1x SPI External Port
- **I2C:** 1x External I2C
- **Audio:** 1x I2S External Port
- **USB:**
  - 1x USB 2.0 High speed Host port (Type C; no USB Port Control)
  - 1x USB 2.0 High speed OTG (Type A)

Mechanical and Environmental

- **Form Factor:** PC/104
- **Dimensions:** 90mm x 96mm
- **Operating Temperature:** -40C – 85C

2.2 Jumper Configuration

The iPac-35D1 comes factory configured. In the event that jumpers need to be verified or modified, this section provides the information required including instructions on setting jumpers and connecting peripherals, switches and indicators. Be sure to read all the safety precautions before you begin any configuration procedure. See Appendix A, for connector pinouts and Appendix B for Jumper Setting descriptions.

Table 1: Jumpers

Label	Function	Default
JB0	Boot 0 Source Selection	Position A
JB1	Boot 1 Source Selection	Position B
JB2	Battery Backup On/Off Selection	Off
JB3	CAN Interface 120Ω Termination Selection	O
JB4	High Drive (HD) GPIO Power/Pullup Source Selection 1	+5V
JB5	High Drive (HD) GPIO Power/Pullup Source Selection 2	Pin 3 to 5 | Pin 4 to 6

2.3 Power Connectors

The iPac-35D1 provides two power connectors. JK1 is a standard 5.5mm barrel jack with an inner diameter of 2.1mm with a center V+ connection. This jack allows for easy connection to a wall mount power supply (see iPac-35D1 product page for available power supply options). HDR1 is a four-pin TE Connectivity locking alternate power connector (part number 640456-4) that mates with a TE Connectivity part number 3-640441-4 mating connector. Using this power input provides for a more rugged/industrial locking connection.

Table 2: Alternate Power Connector (HDR1)

Pin#	Signal
1	+5 Volt Regulated Vin
2	GND
3	GND
4	External Vin* (12V Typical)

***** This pin is routed exclusively to JB5 pins #9 & #10 as a jumper option and is not required to power the board.

2.4 Other Connectors

Table 3 lists the functions of the other various connectors. See Appendix A for connector pinouts.

Table 3: Connectors

Label	Function
CN1	RS232 Serial 9-Pin D-Sub Connector
HDR1	External Vin Alternate Power Connector
HDR2	Com-B RS-232/RS-4xx 10-pin Header Port
HDR3	CAN 3-pin Header Port
HDR4	Com-C RS-232 10-pin Header
HDR5	Linux Console 10-pin Header
HDR6	Misc. ADC/SPI/I2S/I2C 40-pin Header
HDR7	High Drive GPIO/Misc. GPIO 50-Pin Header
HDR8	Processor Based GPIO/ Misc. GPIO
JK1	Vin Barrel Power Connector (regulated 5V only)
JK2	Dual Port Ethernet Connector
JK3	USB Host Port (Type-A)
JK4	USB Host/Device Port (Type-C)
SOK1	uSD Flash Card Socket

2.5 Ethernet

The iPac-35D1 is equipped with two Ethernet PHYs, supporting both Gigabit Ethernet (10/100/1000 Mbps) and Fast Ethernet (10/100 Mbps) connections accessible at a dual port located at JK2. The Gigabit Ethernet PHY allows for high-speed data transfer, making it ideal for applications requiring low latency and high bandwidth, such as network-intensive tasks or large file transfers. Meanwhile, the 10/100 Ethernet PHY provides a more power-efficient option for applications where Gigabit speeds are unnecessary. JK2 is a stacked Ethernet connector with the upper RJ45 being the Gigabit Ethernet BaseT port and the lower being the 10/100 BaseT port.

2.6 Serial Ports

The iPac-35D1 is equipped with four serial ports, one of which terminates to a male DB9 and the other three which terminate to 10-pin header connectors. Most product variations include three 10-pin header to male DB9 connector cables, giving easy access to these ports. Baud Rate, Stop Bits, etc. are all programmable for each port via software.

COMA (CN1) is a dedicated RS232 serial port which has software configurable baud rates. Both asynchronous transmission and data reception are possible. Serial COMA (UART1) is connected to a DB-9 male pin connector on the iPac-35D1. RTS & CTS are native hand shake lines with DTR, DSR, DCD, and RI being GPIO lines PM2, PM3, PM4 and PM5.

Table 4: COMA (CN1)

Pin#	Signal
1	DCD
2	RXD
3	TXD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI
10	NC

COMB (HDR2) provides one software selectable RS232/422/485 serial port which has software configurable baud rates. Both asynchronous transmission and data reception are possible. RS232 Handshake Lines (CTS & RTS) are provided by the processor's UART3. Hardware logic is provided to prevent the RS422/485 TX driver from being enabled at the same time as the RS232 driver.

Table 5: COMB (HDR2)

Pin#	RS-232 Signal	RS-422/485 Signal
1	NC	TX-
2	NC	NC
3	RXD	TX+
4	RTS	NC
5	TXD	RX+
6	CTS	NC
7	NC	RX-
8	NC	NC
9	GND	GND
10	NC	NC

Table 5.1 below shows the control logic to select between RS232/RS422/RS485.

Table 5.1: RS232/422/485 Software Configuration

Transmitter/Receiver Configuration	#4xx_Rx_EN (PI10)	RS485_TRM_EN (PI12)	#COMB_PWRDN (PH6)
OFF	0	0	0
RS232	0	0	1
RS422	1	1	0
RS485	RTS	1	0

These lines are programmable using GPIO PI10, PI12 and PH6.

Com C (HDR4) is an RS-232 communication port that includes Clear to Send (CTS) and Request to Send (RTS) hardware flow control lines, utilizing UART4 for data transmission. This allows for reliable serial communication by preventing data loss due to buffer overflows, as the CTS/RTS signals help regulate the flow of data between devices. COMC is a dedicated hardware UART module within the processor, ensures efficient asynchronous communication with configurable baud rates, parity, and stop bits. This makes COMC suitable for interfacing with a variety of serial devices, including industrial controllers, legacy peripherals, and diagnostic equipment.

Table 6: COMC (HDR4)

Pin#	Signal
1	NC
2	NC
3	RXD
4	RTS
5	TXD
6	CTS
7	NC
8	NC
9	GND
10	NC

Linux Console (HDR5) is an RS-232 communication port utilizing only transmit (Tx) and receive (Rx) lines without hardware flow control signals such as CTS and RTS. This allows for direct serial communication with the system for debugging, configuration, and terminal access. Since it operates without flow control, software-based methods like XON/XOFF may be used to manage data flow if needed. The simplicity of this interface makes it ideal for connecting to terminal emulators, embedded system debugging, or accessing the bootloader for system management.

Table 7: Linux Console (HDR5)

Pin#	Signal
1	NC
2	NC
3	RXD
4	NC
5	TXD
6	NC
7	NC
8	NC
9	GND
10	NC

2.7 CAN

The iPac-35D1 provides a CAN bus interface through a 3-pin header HDR3. The on-processor CAN controller provides all the features required to implement the serial communication protocol. HDR3 utilizes a TE connector part number 640456-3 which mates with 1375820-3.

Table 8: CAN Bus (HDR3)

Pin#	Description
1	CAN_P
2	CAN_N
3	GND

2.8 USB

The iPac-35D1 provides two USB 2.0 Hi-Speed (480 Mbits/Sec) Host ports at JK3 & JK4. The High-Speed ports are also capable of Full-Speed operation and are backwards compatible with USB 1.1 devices. USB devices (printer, mouse, keyboard, camera, etc.) and hubs can be connected to the USB Host in the USB tiered-star topology. JK3 is USB Type A and JK4 is USB Type C.

The specification for standard USB states that each USB port be capable of providing 5 volts at 500 mA. This provision is strictly dependent on the power supply used with the iPac. The power supply must be able to source 5 volts at 1 amp for the USB requirement in addition to the other power requirements of the board. A 500 mA polyfuse protects each USB port from over-current damage. There is no provision to turn off power to the USB host ports.

The iPac-35D1 is equipped with a USB Type-C port located at JK4 that supports High-Speed USB 2.0 OTG (On-The-Go) functionality. This port allows the device to operate as either a USB host or a USB device, enabling flexible connectivity with peripherals such as external storage, input devices, or other USB-enabled hardware. The OTG capability makes it suitable for applications that require dynamic role-switching between host and device modes.

2.9 GPIO

The iPac-35D1 features 32 digital I/O and 4 native processor I/O accessible at headers HDR7 and HDR8 with PWM capability enabled by two Semtech SX1509QB GPIO expanders controlled via an I2C interface. The SX1509QB supports advanced functions such as keypad scanning, LED intensity control through PWM, and programmable logic features, enhancing flexibility in digital interfacing. Additionally, 8 High-Drive (HD) GPIO lines are provided by a Texas Instruments ULN2803C, a Darlington transistor array capable of handling high-current loads with open collector capability which allows interfacing with other voltages such as 24V industrial systems. The ULN2803C integrates clamp diodes for inductive load protection, ensuring robust operation in demanding environments.

Table 9: Digital GPIO/ High Drive GPIO (HDR7)

Pin#	Signal	Pin#	Signal
1	GND	**2**	Ext0_GPIO/PWM0
3	GND	**4**	Ext0_GPIO/PWM1
5	GND	**6**	Ext0_GPIO/PWM2
7	GND	**8**	Ext0_GPIO/PWM3
9	GND	**10**	Ext0_GPIO/PWM4
11	GND	**12**	Ext0_GPIO/PWM5
13	GND	**14**	Ext0_GPIO/PWM6
15	GND	**16**	Ext0_GPIO/PWM7
17	GND	**18**	HDGPIO7
19	GND	**20**	HDGPIO6
21	GND	**22**	HDGPIO5
23	GND	**24**	HDGPIO4
25	GND	**26**	HDGPIO3
27	GND	**28**	HDGPIO2
29	GND	**30**	HDGPIO1
31	GND	**32**	HDGPIO0
33	GND	**34**	Ext0_GPIO/PWM8
35	GND	**36**	Ext0_GPIO/PWM9
37	GND	**38**	Ext0_GPIO/PWM10
39	GND	**40**	Ext0_GPIO/PWM11
41	GND	**42**	Ext0_GPIO/PWM12
43	GND	**44**	Ext0_GPIO/PWM13
45	GND	**46**	Ext0_GPIO/PWM14
47	GND	**48**	Ext0_GPIO/PWM15
49	GND	**50**	I/O_Vout

Table 10: Digital GPIO/Processor Based GPIO (HDR8)

Pin#	Signal	Pin#	Signal
1	GND	**2**	Ext1_GPIO/PWM15
3	GND	**4**	Ext0_GPIO/PWM14
5	GND	**6**	Ext0_GPIO/PWM13
7	GND	**8**	Ext0_GPIO/PWM12
9	GND	**10**	Ext0_GPIO/PWM11
11	GND	**12**	Ext0_GPIO/PWM10
13	GND	**14**	Ext0_GPIO/PWM9
15	GND	**16**	Ext0_GPIO/PWM8
17	GND	**18**	Ext0_GPIO/PWM7
19	GND	**20**	Ext0_GPIO/PWM6
21	GND	**22**	Ext0_GPIO/PWM5
23	GND	**24**	Ext0_GPIO/PWM4
25	GND	**26**	Ext0_GPIO/PWM3
27	GND	**28**	Ext0_GPIO/PWM2
29	GND	**30**	Ext0_GPIO/PWM1
31	GND	**32**	Ext0_GPIO/PWM0
33	GND	**34**	Native I/O 0
35	GND	**36**	Native I/O 1
37	GND	**38**	Native I/O 2
39	GND	**40**	Native I/O 3
41	GND	**42**	+3.3V VCC
43	GND	**44**	+3.3V VCC
45	GND	**46**	+3.3V VCC
47	GND	**48**	+3.3V VCC
49	GND	**50**	+5.0V_VCC

2.10 Miscellaneous I/O

The iPac-35D1 provides a variety of functions, supporting multiple interfaces and power connections. The 40-pin header HDR6 includes eight ADC channels for analog signal input, SPI interface with chip select, clock, MOSI/MISO pins for serial communication, and timer signals for timing applications. The I2S interface offers support for digital audio transmission while I2C5_SDA and I2C5_SCL enable communication with I2C-compatible devices. Power and ground connections, including 3.3V and 5V VCC lines, are available for powering external components. Additionally, reset functionality and an I/O pull-up pin are provided for signal integrity and system control.

Table 11: Miscellaneous I/O (HDR6)

Pin#	Signal	Pin#	Signal
1	ADC0_CH0	**2**	ADC0_CH1
3	ADC0_CH2	**4**	ADC0_CH3
5	ADC0_CH4	**6**	ADC0_CH5
7	ADC0_CH6	**8**	ADC0_CH7
9	SPI2_CS0	**10**	TM0
11	SPI2_CS1	**12**	SPI2_CLK
13	SPI2_MOSI	**14**	SPI2_MISO
15	3.3v_ADC	**16**	3.3V_VCC
17	GND	**18**	GND
19	I2S1_LRCLK	**20**	TM0_EXT
21	GND	**22**	GND
23	3.3V_VCC	**24**	Reset
25	I2S1_MCLK	**26**	I2S1_DI
27	GND	**28**	GND
29	I2S1_DO	**30**	I2S1_BCLK
31	3.3V_VCC	**32**	3.3V_VCC
33	I2C5_SDA	**34**	I2C5_SCL
35	I/O_Pullup	**36**	VStby
37	GND	**38**	GND
39	+5V_VCC	**40**	+5V_VCC

2.11 MMC/SDIO (SD Card)

The iPac-35D1 features integrated eMMC (embedded MultiMediaCard) storage providing a reliable and efficient solution for removable data storage in embedded applications. The 4GB of eMMC on-board flash memory provides the iPac-35D1 with fast read and write speeds, enhancing the overall performance of applications that require quick access to data. For those needing additional quick access storage capacity, an optional upgrade to 16GB of eMMC flash is available allowing for greater flexibility in managing larger datasets and applications. The iPac-35D1 also provides a standard Micro SD type socket located at SOK1 that accepts uSD cards for further memory expansion.

2.12 Real Time Clock

The iPac-35D1 processor is equipped with an internal, ultra-low power Real-Time Clock (RTC). The integrated RTC is powered by an on-board 3V Lithium battery (BR-1225A/HBN) which is managed via JB2.

3 Software

The iPac-35D1 offers a wide variety of software support from both open source and proprietary sources. The hardware core utilizes the Nuvoton MA35D1, which is supported by Linux. For more information on Linux Software Support, please visit the EMAC Wiki Software Section at http://wiki.emacinc.com/wiki/Product_wiki

3.1 Das U-Boot

EMAC utilizes Das U-Boot for its ARM based products. U-Boot is an open source/cross-architecture platform independent bootloader. It supports reading and writing to the flash, auto-booting, environmental variables, and TFTP. Das U-boot can be used to upload and run and/or reflash the OS or to run stand-alone programs without an OS. Products are shipped with valid MAC addresses installed in flash in the protected U-boot environmental variable "ethaddr". At boot time U-Boot automatically stores this address in a register within the MAC, which effectively provides it to any OS loaded after that point.

3.2 Embedded Linux

EMAC Open Embedded Linux (EMAC OE Linux) is an open source Linux distribution for use in embedded systems. The EMAC OE Linux Build is based on the Open Embedded (www.openembedded.org) and Yocto (www.yoctoproject.org) Linux build systems. Open Embedded is a superior Linux distribution for embedded systems. Custom Linux builds are also available on request.

The distribution contains everything a user could expect from a standard Linux kernel: powerful networking features, advanced file system support, security, debugging utilities, and countless other features.

The basic root file system includes:

- Busybox
- Hotplugging support
- APM utilities for power management
- Openssh SSH server
- lighttpd HTTP server
- EXT4 file system with utilities

3.2.1 Linux with PREEMPT RT

PREEMPT RT provides pseudo real time to the kernel and can be used to schedule tasks with hard deadlines and minimal latencies. The PREEMPT RT build is an option to the standard Linux build and is available for a one-time inexpensive support/installation fee.

3.2.2 Linux Packages

EMAC provides support for many Linux Packages such as: PHP, SQLite, Perl, SNMP, DHCP Server, etc. As with the PREEMPT RT Option, other Packages can be added to the standard Linux file system and are available for a one-time inexpensive support/installation fee.

3.2.3 Linux Patches

In addition to standard Embedded Linux support, EMAC has released a number of patches and device drivers from the open source community and from internal EMAC engineering into its standard distribution. Along with kernel patches, EMAC provides the binaries for the kernel and root file system.

3.3 Qt Creator

Qt Creator is a cross-platform IDE (Integrated Development Environment) tailored to the needs of Qt developers but works well for Headless applications as well. EMAC provides sample code as projects that can be imported into Qt Creator. Qt Creator supports remote deployment and source debugging.

http://wiki.qt.io/Main

3.4 ARM EABI Cross Compiler

The popular open source gcc compiler has a stable build for the ARM family. EMAC uses the 4.9.1 version of the ARM EABI compiler. The Embedded Linux kernel and EMAC Qt Creator projects use this compiler for building ARM stand alone, and OS specific binaries. The EMAC Qt Creator provides source level debugging over Ethernet or serial using gdbserver. The Linux binaries for the ARM EABI cross compiler are available online along with the SDK. See the EMAC wiki for further information.

4 Appendix A: Connector Pinouts

4.1 JK1 - Vin Barrel Power Jack Connector

Pin#	Signal
1	Vin
2	GND
3	NC

4.2 JK2 - Dual Port Ethernet Connector

Pin#	Signal
T1	GND
T2	GETH_TX1_P
T3	GETH_TX1_N
T4	GETH_RX1_P
T5	GETH_TX2_P
T6	GETH_TX2_N
T7	GETH_RX1_N
T8	GETH_RX2_P
T9	GETH_RX2_N
T11	ACT_T_3P3V
T12	Gb_ACT_BUF
T13	LINK_T_3P3V
T14	Gb_Link_BUF
B1	GND
B2	10/100_TX_P
B3	10/100_TX_N
B4	10/100_RX_P
B7	10/100_RX_N
B11	ACT_B_3P3V
B12	10/100_ACT
B13	10/100_Link
B14	Link_B_3P3V

4.3 HDR1 - Alternative Power Input

Pin#	Signal
1	+5 Volt Regulated Vin
2	GND
3	GND
4	External_Vin*

4.4 CN1 – Serial Port COMA

Pin#	Signal
1	DCD
2	RXD
3	TXD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI
10	NC

4.5 HDR2 – Serial Port COMB

Pin#	RS-232 Signal	RS-485/422 Signal
1	NC	TX-
2	NC	NC
3	RXD	TX+
4	RTS	NC
5	TXD	RX+
6	CTS	NC
7	NC	RX-
8	NC	NC
9	GND	GND
10	NC	NC

4.6 HDR4 – Serial Port COMC

Pin#	Signal
1	NC
2	NC
3	RXD
4	RTS
5	TXD
6	CTS
7	NC
8	NC
9	GND
10	NC

4.7 HDR5 - Linux Console RS-232

Pin#	Signal
1	NC
2	NC
3	RXD
4	NC
5	TXD
6	NC
7	NC
8	NC
9	GND
10	NC

4.8 HDR3 - CAN Port

Pin#	Description
1	CAN_P
2	CAN_N
3	GND

4.9 JK3 - USB Host Port

Pin#	Signal
1	USB_VCC
2	USB_N
3	USB_P
4	GND

4.10 JK4 - USB Host/Device Port

Pin#	Signal	Pin#	Signal
A1	GND	**B1**	GND
A2	NC	**B2**	NC
A3	NC	**B3**	NC
A4	VBUS	**B4**	VBUS
A5	CC1	**B5**	CC2
A6	DA+	**B6**	DB+
A7	DA-	**B7**	DB-
A8	NC	**B8**	NC
A9	VBUS	**B9**	VBUS
A10	NC	**B10**	NC
A11	NC	**B11**	NC
A12	GND	**B12**	GND

4.11 HDR7 – High-Drive / Digital GPIO

Pin#	Signal	Pin#	Signal
1	GND	**2**	Ext0_GPIO/PWM0
3	GND	**4**	Ext0_GPIO/PWM1
5	GND	**6**	Ext0_GPIO/PWM2
7	GND	**8**	Ext0_GPIO/PWM3
9	GND	**10**	Ext0_GPIO/PWM4
11	GND	**12**	Ext0_GPIO/PWM5
13	GND	**14**	Ext0_GPIO/PWM6
15	GND	**16**	Ext0_GPIO/PWM7
17	GND	**18**	HDGPIO7
19	GND	**20**	HDGPIO6
21	GND	**22**	HDGPIO5
23	GND	**24**	HDGPIO4
25	GND	**26**	HDGPIO3
27	GND	**28**	HDGPIO2
29	GND	**30**	HDGPIO1
31	GND	**32**	HDGPIO0
33	GND	**34**	Ext0_GPIO/PWM8
35	GND	**36**	Ext0_GPIO/PWM9
37	GND	**38**	Ext0_GPIO/PWM10
39	GND	**40**	Ext0_GPIO/PWM11
41	GND	**42**	Ext0_GPIO/PWM12
43	GND	**44**	Ext0_GPIO/PWM13
45	GND	**46**	Ext0_GPIO/PWM14
47	GND	**48**	Ext0_GPIO/PWM15
49	GND	**50**	I/O_Vout

4.12 HDR8 – Digital GPIO / Native Processor I/O

Pin#	Signal	Pin#	Signal
1	GND	**2**	Ext1_GPIO/PWM15
3	GND	**4**	Ext0_GPIO/PWM14
5	GND	**6**	Ext0_GPIO/PWM13
7	GND	**8**	Ext0_GPIO/PWM12
9	GND	**10**	Ext0_GPIO/PWM11
11	GND	**12**	Ext0_GPIO/PWM10
13	GND	**14**	Ext0_GPIO/PWM9
15	GND	**16**	Ext0_GPIO/PWM8
17	GND	**18**	Ext0_GPIO/PWM7
19	GND	**20**	Ext0_GPIO/PWM6
21	GND	**22**	Ext0_GPIO/PWM5
23	GND	**24**	Ext0_GPIO/PWM4
25	GND	**26**	Ext0_GPIO/PWM3
27	GND	**28**	Ext0_GPIO/PWM2
29	GND	**30**	Ext0_GPIO/PWM1
31	GND	**32**	Ext0_GPIO/PWM0
33	GND	**34**	Native I/O 0
35	GND	**36**	Native I/O 1
37	GND	**38**	Native I/O 2
39	GND	**40**	Native I/O 3
41	GND	**42**	+3.3V VCC
43	GND	**44**	+3.3V VCC
45	GND	**46**	+3.3V VCC
47	GND	**48**	+3.3V VCC
49	GND	**50**	+5.0V_VCC

4.13 HRD6 – Miscellaneous I/O

Pin#	Signal	Pin#	Signal
1	ADC0_CH0	**2**	ADC0_CH1
3	ADC0_CH2	**4**	ADC0_CH3
5	ADC0_CH4	**6**	ADC0_CH5
7	ADC0_CH6	**8**	ADC0_CH7
9	SPI2_CS0	**10**	TM0
11	SPI2_CS1	**12**	SPI2_CLK
13	SPI2_MOSI	**14**	SPI2_MISO
15	3.3v_ADC	**16**	3.3V_VCC
17	GND	**18**	GND
19	I2S1_LRCLK	**20**	TM0_EXT
21	GND	**22**	GND
23	3.3V_VCC	**24**	Reset
25	I2S1_MCLK	**26**	I2S1_DI
27	GND	**28**	GND
29	I2S1_DO	**30**	I2S1_BCLK
31	3.3V_VCC	**32**	3.3V_VCC
33	I2C5_SDA	**34**	I2C5_SCL
35	I/O_Pullup	**36**	VStby
37	GND	**38**	GND
39	+5V_VCC	**40**	+5V_VCC

5 Appendix B: Jumper Settings

5.1 JB0 (Boot 0 Source Selection)

Jumper	Position	Setting
Pins 1 & 2*	A	Line Pulled High
Pins 2 & 3	B	Line Pulled Low

*Default Setting

5.2 JB1 (Boot 1 Source Selection)

Jumper	Position	Setting
Pins 1 & 2	A	Line Pulled High
Pins 2 & 3*	B	Line Pulled Low

*Default Setting

5.3 JB2 (Battery Backup On/Off Selection)

Jumper	Position	Setting
Pins 1 & 2	On	Enable Battery Backup
Pins 2 & 3*	Off	Disable Battery Backup

*Default Setting

5.4 JB3 (Can Interface 120Ω Termination Selection)

Jumper	Position	Setting
Pins 1 & 2	Closed	Termination Present
Pins 2 & 3*	Open	Not Terminated

*Default Setting

5.5 JB4 (High Drive GPIO Power/Pullup Source Selection 1)

Jumper	Position	Setting
Pins 1 & 2	Vin Protect	Vin from iPac Power Input
Pins 2 & 3*	5VCC	5VCC

*Default Setting

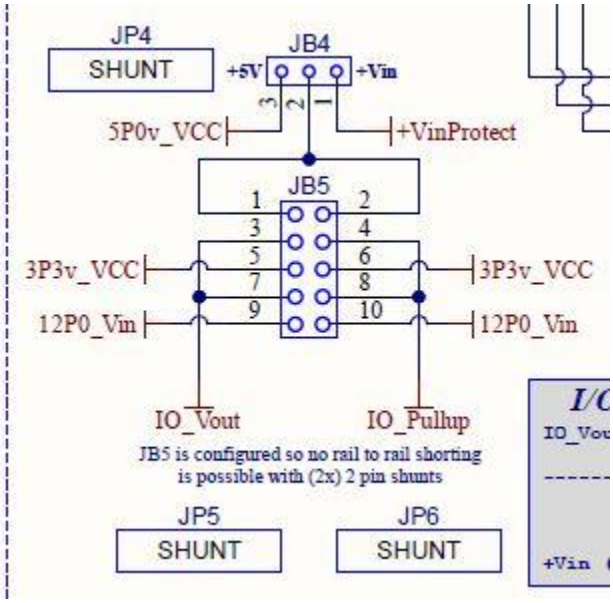
5.6 JB5 (High Drive GPIO Power/Pullup Source Selection 2)

Jumper	Position	Setting
Pins 3 & 5*	3.3VCC	I/O Vout
Pins 4 & 6*	3.3VCC	I/O Pullup

*Default Setting

JB4 controls the pull-up voltage of the High Drive Output lines and determines what voltage is present at Pin 50 of HDR7. One side of the jumper (IO_Vout) controls pin 50 of HDR7 and the other side (IO_Pullup) controls the pull-up voltage of Pin 35 of HDR6 . Leaving the IO_Vout shunt off leaves pin 50 of HDR7 open and leaving the IO_Pullup shunt off sets the High Drive Outputs to no pull-up voltage. The voltage at Pins 1 & 2 on JB5 is defined by JB4. The default position for the jumpers on JB5 are Pins 3 & 5 and 4 & 6. The default jumper position sets the output pull-ups and the output voltage on Pin50 of HDR7 to 3.3V. See image below for the JB4 and JB5 jumper block pin numbers.

JB4 and JB5



6 Dimensional Drawings