SoM-35D1F

User Manual

November 2024

Rev. 1.0

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1. Introduction

This document describes EMAC's SoM-35D1F System on Module (SoMs). The SoM-35D1F is based on the 64-bit NuvoTon MA35D1 Dual ARM Cortex-A35 processor, providing dual 800MHz Cortex-A35 Cores and an additional 180MHz Cortex-M4 Processor core. The SoM-35D1F is a System on Module, designed to be compatible with EMAC's 200-pin SODIMM form factor. The SoM-35D1F has an onboard Gigabit Ethernet PHY, 4 serial ports, an RTC, onboard eMMC flash, Serial Flash, and SDRAM. In addition to the standard SoM features, the SoM-35D1F also features open-source software support and a wide range of controller I/O pins.

1.1. Features

- **Small, 200 pin SODIMM form factor (2.66" x 2.384")**
- **NuvoTon MA35D1 Dual ARM Cortex A35 800MHz & 180MHz Cortex M4 Processor**
- **4GB of eMMC flash (16GB Optional)**
- **16MB of NOR serial flash**
- **512MB of DDR3L RAM**
- **4x Serial ports (1x with full handshake and 2x with RTS/CTS handshake)**
- **10/100/1000 BaseT Ethernet with on-board PHY**
- **10/100 BaseT MAC**
    - **RMII Interface for additional 10/100 BaseT Carrier based PHY**
- **2x USB 2.0 (HIGH Speed) host ports**
- **1x USB 2.0 (HIGH Speed) OTG host/ device port**
- **4-Channel 12-bit ADC**
- **4 wire touchscreen interface**
- **24-bit LCD controller**
- **Internal Real Time Clock/Calendar (with external battery backup)**
- **16x GPIO**
- **4x GP PWM channels**
- **1x PWM channel for LCD backlight**
- **3x Timer/Counters (Replaces 3 ADC channels if used)**
- **1x Programmable clock output (Replaces one GPIO if used)**
- **1x Synchronous serial I/O audio port (I2S)**
- **2x I2C ports**
- **2x SPI ports (4 SPI CS)**

- **2x CAN ports**
- **External reset button**
- **Software controlled green status LED**
- **2x SDIO SD port (1 available, 1 used by eMMC)**
- **+3.3V board input voltage**
- **4x Lanes of MIPI CSI Camera Interface**

2. Hardware

2.1. Specifications

- **CPU:** NuvoTon MA35D1 Dual ARM Cortex A35 800MHz & 180MHz Cortex M4 Processor
- **Flash:** 4GB eMMC Flash (16GB eMMC Flash Optional) and 16 MB of Serial Data Flash
- **RAM:** 512 MB of DDR3L
- **Security:** NuvoTon Trusted Secure Island (TSI), an isolated secure hardware unit with TrustZone, secure boot, tamper-detection, built-in cryptographic accelerators with AES, SHA, ECC, RSA, SM2/3/4, and a TRNG, as well as Key Store and OTP memory.
- **SDIO:** 4-bit SDHC/MMC interface
- **System Reset:** External reset button
- **RTC:** Internal real time clock with external battery backup
- **Timer/Counters:** 12 sets of 32-bit timers integrated into the MA35D1
- **PWM:** 4x PWM modulation channels
- **Watchdog Timer:** 3x WDT's and 3x WWDT's integrated into the MA35D1.
- **Digital I/O:** 16x GPIO
- **Analog I/O:** 4x Channels, 12-bit ADC
- **Power:** Power management controller allows for selectively shutting down on-processor I/O functionality and running from a slow clock**.**
- **Clocks:** Programmable clock output

Serial Interfaces

- **UARTS:** 4x channels which support RS485
- **SPI:** 2x SPI port (4 SPI CS)
- **Audio:** I2S Synchronous Serial Controller with analog interface support
- **USB:** 2x USB high speed host port, 1 USB high speed host/device port (OTG)
- **I2C:** 2x I2C ports

Ethernet Interface

- **MAC:** 2x MACs (RGMII, RMII)
  - The RGMII connects to an on board PHY (KSZ9031) and requires external magnetics for a 10/100/1000 port.
  - The RMII requires an external PHY and external magnetics for a 10/100 port

Mechanical and Environmental

- **Dimensions:** SODIMM form factor with the length dimension extended (2.66" x 2.384")
- **SODIMM TYPE:** 200 Pin DDR1 (not compatible with DDR2 connector. See the section titled Designing Your Own Carrier.)
- **Power Supply Voltage:** +3.3 Volts DC +/- 5%
- **Power Requirements (Typical):**
  - 3.3 Volts @ 100 mA
  - Max current draw during boot process: 340 mA
- **Operating Temperature:** -40 to 85° C (-40 to 185 ° F), fanless operation
- **Operating Humidity:** 0% to 90% relative humidity, non-condensing

2.2. Real-Time Clock

The SoM-35D1F has an embedded Real-time Clock. Battery backup is provided from the carrier board using the VSTBY pin. The RTC has the provision to set alarms that can interrupt the processor. For example, the processor can be placed in sleep mode and then later awakened using the alarm function.

2.3. Watchdog Timer

The SoM-35D1F provides three watchdog timers (WDT) and three window watchdog timers (WWDT) integrated into the MA35D1. One for Trust Zone Secure (TZS), one for Trust Zone Secure/Non-Secure (TZS/TZNS) and the other is SubM.

2.4. External Connections

The SoM-35D1F connects to the SoM-255G2 carrier board containing connectors, power supply interface logic, and expansion IO, through a standard ENIG-plated (Electroless Nickel Immersion Gold) SODIMM 200-pin connection shown below.

The SoM model will fit in any standard EMAC 200-pin SODIMM socket. These connections are designed to be compatible with all EMAC 200-pin SoM products. See EMAC SoM 200-pin SODIMM Pinout Specification to see how other 200-pin SoM pinouts line up with the SoM-35D1F's pinout. The use of the DDR SODIMM form-factor for EMAC's SoMs is a sound choice that has been proven rugged and reliable in the laptop and embedded SBC markets. The remainder of this section describes the pinout as it applies specifically to the SoM-35D1F processor.

Notes about the signal descriptions that follow:

- Signals are 3.3V unless otherwise specified.
- Signals names that include "#" are active low, and are normally pulled high on the SOM.
- * in the Port Line column means that the signal goes to other logic on the SOM and may not terminate at a single processor port pin
- "NC" in the tables stands for Not Connected, which means that although a signal is defined in the 200-pin SOM specification, it is not used by this SOM.

2.4.1. System

RST_IN# pin is an active low input that drives the processor reset pin. The RST_OUT pin is an active low output that is driven low by either the watchdog timer or a software reset. The FLASH_WP# pin is an active low input that prevents the serial NOR flash from being written to. The BOOT_OPTION pins are read on the falling edge of RST_IN# and determine the boot device:

Table 1: Boot Options

Boot1	Boot2	Description
0	0	On-board QSPI Serial Flash
0	1	On-board eMMC0
1	0	SDIO1 interface
1	1	USB OTG port

Table 2: System Control

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
151	RST_IN#	*	*	Processor Reset
152	RST_OUT#	nRESET	nRESET	Processor Reset
154	FLASH WP#	*	PB8	Serial Flash Write Protect
54	WKUP	*	*	Processor Wakeup Input
157	BOOT_OPTION0	*	PG0-7	Boot0 Option Select
158	BOOT_OPTION1	*	PG0-7	Boot1 Option Select

2.4.2. JTAG

JTAG (Joint Test Action Group) is a standard for testing and debugging integrated circuits. It provides a means for accessing the internal features of a microcontroller or processor via a standardized interface. The JTAG interface is not necessary for this SOM, and not connected. The following pins are normally allocated for JTAG in the 200 pin SOM spec.

Table 3: Processor JTAG

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
139	JTAG_TCK	NC	JTAG Clock
140	JTAG_TDI	NC	JTAG Serial In
141	JTAG_TDO	NC	JTAG Serial Out
142	JTAG_TMS	NC	JTAG Operation Mode
143	JTAG_TRST	NC	Test Reset Signal
144	JTAG_RTCK	NC	Dynamic Clock Sync

2.4.3. I2C

Two I2C ports are brought to the card edge. The I2C addresses already used by SOM devices are as follows:

I2C1 Addresses: Touch Controller 0x4A, EEPROM 0x50
I2C2 Addresses: Camera bridge 0x0E, GPIO expander 0x20

Table 4: I2C Port

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
29	I2C_A_CLK	I2C1_SCL	PN5	Clock Pin
30	I2C_A_DATA	I2C1_SDA	PN4	Data Pin
146	I2C_B_CLK	I2C2_SCL	PN1	Clock Pin
148	I2C_B_DATA	I2C2_SDA	PN0	Data Pin

2.4.4. Ethernet

The SoM-35D1F provides a KSZ9031 10/100/1000 Ethernet PHY IC on board. Carrier designers need only run these lines through the appropriate magnetics layer to have a functional Ethernet connection.

Table 5: Ethernet

SODIMM Pin#	SoM Pin Name	KSZ9031 Pin Name(s)	Description
12	MDI_D-	TXRXD_N	GIG Ethernet D- pin
14	MDI_D+	TXRXAD_P	GIG Ethernet D+ pin
13	MDI_C-	TXRXC_N	GIG Ethernet C- pin
15	MDI_C+	TXRXC_P	GIG Ethernet C+ pin
16	MDI_B-	TXRXB_N	GIG Ethernet B- pin
18	MDI_B+	TXRXB_P	GIG Ethernet B+ pin
17	MDI_A-	TXRX_A-	GIG Ethernet A- pin
19	MDI_A+	TXRX_A+	GIG Ethernet A+ pin
38	LINK#	LED2/ PHYAD1	Ethernet Link LED2/ Configuration
39	ACT#	LED1/ PHYAD1	Ethernet Link LED1/ Configuration

Table 6: RMII Ethernet Interface

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
159	TXD0	RMII TXD0	RMII Transmit Data 0
161	TXD1	RMII TXD1	RMII Transmit Data 1
160	RXD0	RMII RXD0	RMII Receive Data 0
162	RXD1	RMII RXD1	RMII Receive Data 1
167	TX_CTL	RMII TXEN	RMII Transmit Control
168	RX_CTL	RMII CRSDV	RMII Receive Control
172	RX_ERR	RMII RX ERR	RMII Receive Error
170	RX_CLK	RMII REFCK	RMII Reference Clock
171	MDC	RMII MDC	RMII Management Data Clock
173	MDIO	RMII MDIO	RMII Management Data IO

2.4.5. USB

The SoM 200-pin specification provides for 2 USB hosts and 1 USB device or OTG (On-The-GO) port.

Table 7: USB

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
5	USB_A+ (To USB Hub)	HSUSB1_D+ (From Hub)	*	Host USB 2.0 Port A+
7	USB_A- (To USB Hub)	HSUSB1_D- (From Hub)	*	Host USB 2.0 Port A-
6	USB _B+ (To USB Hub)	HSUSB1_D+ (From Hub)	*	Host USB 2.0 Port B+
8	USB _B- (To USB Hub)	HSUSB1_D- (From Hub)	*	Host USB 2.0 Port B-
9	USB_OTG_D-	HSUSB0_D-	HSUSB1_D-	USB OTG 2.0 Port D-
11	USB_OTG_D+	HSUSB0_D+	HSUSB1_D+	USB OTG 2.0 Port D+
10	USB_OTG_VBUS	HSUSB0_VBUSVLD	PF15	OTG VBUS
40	USB_OTG_ID	HUSB0_ID	HSUSB1_ID	OTG ID
174	HSUSB0_PWREN	HSUSB0_PWREN	PL12	Power Enable

2.4.6. SPI

The MA35D1 processor provides two SPI (Serial Peripheral Interface) channels, SPI0 and SPI1, for communicating with peripheral devices. The SPI1 bus is connected internally to the serial flash. The serial flash chip select line is not brought out to the card fingers. Table 7 below lists the lines for SPI channel 0. Table 8 below lists the lines for the SPI channel 1. Note SPI Chip Selects (CS) for Linux does not require a specific SPI_CS and as such can use any GPIO allowing additional chip selects if a custom carrier is used.

Table 8: SPI Channel 0

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
22	SPI0_MISO	SPI0_MISO	PB11	SPI0 Serial Data In
23	SPI0_MOSI	SPI0_MOSI	PB10	SPI0 Serial Data Out
24	SPI0_SCK	SPI0_CLK	PB9	SPIO Serial Clock Out
25	SPI0_CS0#	CS0	PD6	SPI0 Chip Select line 0
26	SPI0_CS1#	CS1	PE15	SPI0 Chip Select line 1
27	SPI0_CS2#	CS2	PE14	SPI0 Chip Select line2
28	SPI0_CS3#	CS3	PL14	SPI0 Chip Select line 3

Table 9: SPI Channel 1

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
126	SPI1_SCK	QSPI0_CLK	PD0	SPI1 serial clock out
127	SPI1_MOSI	QSPI0_MOSI	PD1	SPI1 serial data out
128	SPI1_MISO	QSPI0_MISO	PD2	SPI1 serial data in
134	SPI1_CS0#	GPB6 (16x GPIO Expander)	*	SPI1 Chip Select

2.4.7. Media Card Interfaces

The SoM-35D1F features integrated eMMC (embedded MultiMediaCard) storage, providing a reliable and efficient solution for removable data storage in embedded applications. The 4GB of eMMC flash memory provides the SoM-35D1F with fast read and write speeds, enhancing the overall performance of applications that require quick access to data. For those needing additional quick access storage capacity, an optional upgrade to 16GB of eMMC flash is available, allowing for greater flexibility in managing larger datasets and applications.

The SOM also features an SDIO interface to the card edge as shown in the table below.

Table 10: MMC/SD Card Interface

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
31	SCLK	SD1_CLK	PJ7	SDIO Clock
32	CMD	SD1_CMD	PJ6	SDIO Command
33	DAT0	SDI_DAT0	PJ8	SDIO D0
34	DAT1	SDI_DAT1	PJ9	SDIO D1
35	DAT2	SDI_DAT2	PJ10	SDIO D2
36	DAT3	SDI_DAT3	PJ11	SDIO D3
37	Card Detect	SD1_nCD	PJ5	Card Detect
196	SD_WP	SD1_WP	PJ4	SD Write Protect

2.4.8. UART

UART (Universal Asynchronous Receiver-Transmitter) enables asynchronous serial communication between devices. The SoM-35D1F utilizes four communications ports, COMA, COMB (No Handshaking), COMC, and COMD. These communication ports facilitate connections with peripherals, sensors, and other devices providing flexibility for developers to implement serial communication in their applications. These signals are all logic level at the card edge. Any physical layer signal levels need to be generated by the carrier board.

Table 11: UARTs

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	SoM Description
95	COMA_TXD	UART1_TXD	PA3	COMA transmit/GPIO
96	COMA_RXD	UART1_RXD	PA2	COMA receive/GPIO
97	COMA_CTS	UART1_nCTS	PA0	COMA CTS/GPIO
98	COMA_RTS	UART1_nRTS	PA1	COMA RTS/GPIO
99	COMA_DTR	DTR	PC7	COMA DTR/GPIO
100	COMA_DSR	DSR	PN2	COMA DSR /GPIO
101	COMA_RI	RI	PN3	COMA RING/GPIO
102	COMB_TXD	UART0_TXD	PE14	COMB transmit/GPIO
103	COMB_RXD	UART0_RXD	PE15	COMB receive/GPIO
104	COMB_CTS	NC	NC	NC
105	COMB_RTS	NC	NC	NC
106	COMC_TXD	UART5_TXD	PA11	COMC transmit/GPIO
107	COMC_RXD	UART5_RXD	PA10	COMC receive/GPIO
108	COMC_CTS	UART5_nCTS	PA8	COMC CTS/GPIO
109	COMC_RTS	UART5_nRTS	PA9	COMC RTS/GPIO
110	COMD_TXD	UART3_TXD	PA7	COMD transmit/GPIO
111	COMD_RXD	UART3_RXD	PA6	COMD receive/GPIO
112	COMD_CTS	UART3_nCTS	PA5	COMD CTS/GPIO
113	COMD_RTS	UART3_nRTS	PA4	COMD RTS/GPIO

2.4.9. Oscillators

The SoM-35D1F has one programmable oscillator output which is a versatile timing component that generates clock signals at configurable frequencies.

Table 12: Oscillators

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	SoM Description
133	GPIO15	PN.15/CLKO	PN.15	Programmable clock output

2.4.10. Analog to Digital Converters

The SoM-200 pin specification allocates eight pins for ADC's. Four of these pins are used for touchscreen control and the other four provide 12-bit Successive Approximation Register analog -to-digital conversion (SAR ADC).

The analog voltage reference must be 3.3V. The Analog voltage reference pin and analog ground pin are listed in the Power Connections section. The voltage reference pin and analog ground pin must be connected in order for the analog inputs and touch interface pins to function properly.

Table 13: ADC

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
49	SX+/ADC4	ADC0_CH4	PB12	12- bit ADC
50	SX-/ADC5	ADC0_CH5	PB13	12- bit ADC
51	SY+/ADC6	ADC0_CH6	PB14	12- bit ADC
52	SY-/ADC7	ADC0_CH7	PB15	12- bit ADC

Table 14: Touch Screen Controller

SODIMM Pin#	SoM Pin Name	Controller Pin Name(s)	Description
45	X+/ADC0	X+	X+ Channel Input
46	X-/ADC1	X-	X- Channel Input
47	Y+/ADC2	Y+	Y+ Channel Input
48	Y-/ADC3	Y-	Y- Channel Input

2.4.11. GPIO

The SoM-35D1F features a robust set of 16 GPIO (General Purpose Input/Output) pins, enhancing its versatility for various applications. GPIO 0 through GPIO 13 are connected to a GPIO expander, allowing for expanded control and management through an I2C interface. GPIO 14 and 15 are directly connected to the CPU, enabling high-speed communication for critical tasks. GPIO 15 can also be programmed as a programmable oscillator output, and is listed in the Oscillators section.

Table 15: GPIO

SODIMM Pin#	SoM Pin Name	GPIO Expander Pin Name	Description
114	GPIO0	GPA0	General Purpose Input/Output
115	GPIO1	GPA1	General Purpose Input/Output
116	GPIO2	GPA2	General Purpose Input/Output
117	GPIO3	GPA3	General Purpose Input/Output
118	GPIO4	GPA4	General Purpose Input/Output
119	GPIO5	GPA5	General Purpose Input/Output
120	GPIO6	GPA6	General Purpose Input/Output
121	GPIO7	GPA7	General Purpose Input/Output
122	GPIO8	GPB0	General Purpose Input/Output
123	GPIO9	GPB1	General Purpose Input/Output
124	GPIO10	GPB2	General Purpose Input/Output
125	GPIO11	GPB3	General Purpose Input/Output
130	GPIO12	GPB4	General Purpose Input/Output
131	GPIO13	GPB5	General Purpose Input/Output
132	GPIO 14	CPU Pin 165 (PN14)	General Purpose Input/Output
133	GPIO 15	CPU Pin 166 (PN15)	General Purpose Input/Output

2.4.12. LCD & Touch Screen

The resistive touch screen LCD utilizes a four-wire touchscreen interface allowing for accurate touch detection. This interface works by measuring voltage changes across the layers of the touchscreen providing reliable input in various environmental conditions. The touch lines are listed below and also in the Analog to Digital Converter section.

Table 16: Touch Screen Controller

SODIMM Pin#	SoM Pin Name	Controller Pin Name(s)	Description
45	X+/ADC0	X+	X+ Channel Input
46	X-/ADC1	X-	X- Channel Input
47	Y+/ADC2	Y+	Y+ Channel Input
48	Y-/ADC3	Y-	Y- Channel Input

The display is driven by a 24-bit LCD controller that facilitates high-resolution color depth and precise pixel control and provides a PWM for Display brightness control.

Table 17: LCD

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
57	LCD_BLUE0	LMC_DATA16	PC12	LCD Blue 0
58	LCD_BLUE1	LMC_DATA17	PC13	LCD Blue1
59	LCD_BLUE2	LMC_DATA18	PC14	LCD Blue2
60	LCD_BLUE3	LMC_DATA19	PC15	LCD Blue3
61	LCD_BLUE4	LMC_DATA20	PH12	LCD Blue4
62	LCD_BLUE5	LMC_DATA21	PH13	LCD Blue5
63	LCD_BLUE6	LMC_DATA22	PH14	LCD Blue6
64	LCD_BLUE7	LMC_DATA23	PH15	LCD Blue7
65	LCD_GREEN0	LMC_DATA8	PH0	LCD Green0
66	LCD_GREEN1	LMC_DATA9	PH1	LCD Green1
67	LCD_GREEN2	LMC_DATA10	PH2	LCD Green2
68	LCD_GREEN3	LMC_DATA11	PH3	LCD Green3
69	LCD_GREEN4	LMC_DATA12	PH4	LCD Green4
70	LCD_GREEN5	LMC_DATA13	PH5	LCD Green5
71	LCD_GREEN6	LMC_DATA14	PH6	LCD Green6
72	LCD_GREEN7	LMC_DATA15	PH7	LCD Green7
73	LCD_RED0	LMC_DATA0	PI8	LCD Red0
74	LCD_RED1	LMC_DATA1	PI9	LCD Red1
75	LCD_RED2	LMC_DATA2	PI10	LCD Red2
76	LCD_RED3	LMC_DATA3	PI11	LCD Red3
77	LCD_RED4	LMC_DATA4	PI12	LCD Red4
78	LCD_RED5	LMC_DATA5	PI13	LCD Red5
79	LCD_RED6	LMC_DATA6	PI14	LCD Red6
80	LCD_RED7	LMC_DATA7	PI15	LCD Red7
81	LCD_HSYNC	LMC_HSYNC	PG9	LCD Vertical Sync
82	LCD_VSYNC	LMC_VSYNC	PG8	LCD Horizontal Sync
83	LCD_ENA	LMC_DEN	PK4	LCD Enable
84	LCD_CLK	LMC_CLK	PG10	LCD Clock
85	BCKLIGHT_PWM	EPWM2_CH0	PK12	Backlight Brightness Control

2.4.13. Camera Serial Interface

CSI (Camera Serial Interface) is a high-speed interface standard used for connecting cameras to processors in embedded systems. It facilitates the transmission of image data from the camera to the host processor with minimal latency supporting multiple data lanes for increased bandwidth. MIPI CSI typically employs a differential signaling method enhancing noise immunity and enabling reliable communication. The table below illustrates the connections between the 200-pin SODIMM pinout and the Toshiba TC358748XBG Camera Bridge.

Table 18: CSI

SODIMM Pin#	SoM Pin Name	Camera Bridge Pin Name	Description
184	CSI_CLK+	MIPI-CP	MIPI Clock Positive
186	CSI_CLK-	MIPI-CN	MIPI Clock Negative
187	CSI_D0+	MIPI-D0P	MIPI Data0 Positive
189	CSI_D0-	MIPI-D0N	MIPI Data0 Negative
188	CSI_D1+	MIPI-D1P	MIPI Data1 Positive
190	CSI_D1-	MIPI-D1N	MIPI Data1 Negative
191	CSI_D2+	MIPI-D2P	MIPI Data2 Positive
193	CSI_D2-	MIPI-D2N	MIPI Data2 Negative
192	CSI_D3+	MIPI-D3P	MIPI Data3 Positive
194	CSI_D3-	MIPI-D3N	MIPI Data3 Negative

2.4.14. Power Connections

The SoM-35D1F only requires a 3.3V supply. Other voltage levels required by the SOM are derived on the SOM from the 3.3V supply.

Table 19: Power Connections

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
3,4,43,44,135, 136,197,198	3.3VCC	3.3VCC	3.3 Volt SoM Supply Voltage
1,2,20,21,41,42, 91,92,137,138, 155,156,199,200	GND	GND	Digital Ground
53	Analog_GND	ADC_GND	Analog Ground
56	VSTBY	Vstandby_3.3	Voltage standby, this is the backup voltage provided to the SoM's RTC. If RTC readings are not important for the application, this can be attached to the 3.3V rail.
55	AV_REF	NC	Analog power/reference. It can be typically connected to 3.3V. LC filtering for this power signal is provided on-module.

2.4.15. I2S

The M35D1 provides an I2S audio port which is accommodated within the SoM specification. Note that there is no CODEC on the SoM and therefore must be provided on the Carrier. In addition, the CODEC will require either SPI or I2C for control.

Table 20: I2S

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
86	AudioA_SCLK	I2S1_BCLK	PG13	I2S Clock
87	AudioA_LRCLK/Frame	I2S1_LRCLK	PG12	I2S Left/Right Clock
88	AudioA_MCLK	I2S1_MCLK	PG11	I2S Master Clock
89	AudioA_DIN	I2S1_DI	PG14	I2S Data Input
90	AudioA_DOUT	I2S1_DO	PG15	I2S Data Output

2.4.16. Control Area Network

The Controller Area Network (CAN) is a robust communication protocol designed for microcontrollers and devices to exchange data without a central host commonly used in automotive and industrial systems. Known for its reliability, noise immunity, and real-time data handling, CAN efficiently manages data between multiple devices making it ideal for safety-critical and complex network environments.

Table 21: CAN

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
93	CAN_A_TX	CAN1_TXD	PN7	CAN Transmit
94	CAN_A_RX	CAN1_RXD	PN6	CAN Receive
145	CAN_B_TX	CAN2_TXD	PN11	CAN Transmit
147	CAN_B_RX	CAN2_RXD	PN10	CAN Receive

3. Design Considerations

One of the goals of the SoM-35D1F is to provide a modular, flexible and inexpensive solution capable of delivering high-end performance with low power requirements.

3.1. Off-the-Shelf Carriers

Many SoM-35D1F applications can make use of EMAC's off-the-shelf carriers. These carriers provide power to the SoM as well as a wealth of connectors and interfaces to access peripheral I/O including audio.

3.1.1. SoM-255G2

- 1x 1000 BaseT Ethernet Port
- 1x 10/100 BaseT Ethernet Port
- 1 Wifi/BT module
- 4x serial ports (3x RS232 and 1x RS232/422/485 port)
- Resistive Touchscreen interface
- 7” graphic TFT color LCD, 800 x 480 (WVGA)
- Or 10” TFT LVDS color LCD, 1024 x 600 (WSVGA) Graphic LCD with Touchscreen
- MicroSD Flash Slot
- 2x USB Host & 1 USB OTG ports
- 1x I2S Audio port with Line-In/Line-Out
- Headers with access to GPIO, SPI, I2C, PWM, A/D
- 1x CAN-FD
- 4-lane CSI Connector
- 4-lane DSI Connector (for use with other SOMs)
- Operating Temp 0°C to 60°C (-40°C to 85°C available without LCD or CSI)
- Operating Voltage of 12 to 28 Vdc.

https://shop.emacinc.com/product/som-255g2/

3.2. Semi-Custom Carriers

EMAC also offers a semi-custom engineering service. By modifying one of our existing designs, EMAC can offer quick-turn, low-cost engineering for your specific application.

3.3. Designing Your Own Carrier

It is best to start with the SoM-255G2 as a reference. When designing a carrier, be sure to use a 200 pin DDR1 SODIMM socket instead of the more common DDR2 socket. The DDR2 socket is keyed in such a way as to prevent the SoM from being inserted into it. The part number for a compatible DDR1 socket made by Tyco is 1473005-1. This socket will provide 3.0 mm of height from the top of carrier PCB to the bottom of the module PCB. The module specification allows for a 1.5 mm maximum height for bottom components. Therefore, this allows the user < 1.5 mm for placing components safely under the module. If more height is needed, Tyco as well as other manufacturers, make SODIMM sockets with additional height, although these are more expensive.

3.3.1. Power

The SoM-35D1F requires a voltage of 3.3V at 300mA for a normal operation. Users can get away with using only 3.3V and simply provide this to all the voltage inputs listed in 3.6. This however will not provide battery backup for the RTC. Additionally, 5V is required if USB Host capability is required.

3.3.2. Battery Backup

The real-time clock requires a backup voltage to maintain its data. This backup voltage comes from the VSTBY SoM pin, and should be connected to 3 volts or 3.3 volts.

The RTC will draw approximately 8 µA when the processor is not powered by the main 3.3V supply. Be aware that the Static current can rise if the temperature increases to 85° C. When the module is powered, no current is drawn from the backup battery supply. If RTC backup is not needed, this can be tied to 3.3V.

The SoM-255G2, as well as other carriers, provide battery backup voltage through a replaceable CR2032X. This is a standard, widely available, 3V 200mA/H 20MM coin battery.

4. Software

The SoM-35D1F offers a wide variety of software support from both open source and proprietary sources. The hardware core utilizes the Nuvoton ARM dual core Cortex A35 and Cortex M4 Microprocessor, which is supported by Linux.

For more information on Linux Software Support, please visit the EMAC Wiki Software Section at:

http://wiki.emacinc.com/wiki/Product_wiki

4.1. Das U-Boot

EMAC utilizes Das U-Boot for its ARM based products. U-Boot is an open source/cross-architecture platform independent bootloader. It supports reading and writing to the flash, auto-booting, environmental variables, and TFTP. Das U-boot can be used to upload and run and/or reflash the OS or to run stand-alone programs without an OS. Products are shipped with a valid MAC address installed in flash in the protected U-boot environmental variable “ethaddr”. At boot time U-Boot automatically stores this address in a register within the MAC, which effectively provides it to any OS loaded after that point.

4.2. Embedded Linux

EMAC Open Embedded Linux (EMAC OE Linux) is an open source Linux distribution for use in embedded systems. The EMAC OE Linux Build is based on the Open Embedded (www.openembedded.org) and Yocto (www.yoctoproject.org) Linux build systems. Open Embedded is a superior Linux distribution for embedded systems. Custom Linux builds are also available on request.

The distribution contains everything a user could expect from a standard Linux kernel: powerful networking features, advanced file system support, security, debugging utilities, and countless other features.

The basic root file system includes:

- Busybox
- Hotplugging support
- APM utilities for power management
- Openssh SSH server
- lighttpd HTTP server
- JJFS2 or EXT4 file system with utilities

4.2.1. Linux with Real Time Extensions

Real Time processing can be had by utilizing Linux PREEMPT RT or Xenomai real time extensions. PREEEMPT RT is pseudo real time by is often good enough for various use cases. Xenomai is hard real time adds real time extensions to the kernel and can be used to schedule tasks with hard deadlines and µs latencies. The Xenomai build is an additional module that can be added to the standard Linux kernel and is available for a one-time inexpensive support/installation fee.

http://www.xenomai.org/

4.2.2. Linux Packages

EMAC provides support for many Linux Packages such as: PHP, SQLite, Perl, SNMP, DHCP Server, etc. As with the Xenomai Package, other Packages can be added to the standard Linux file system and are available for a one-time inexpensive support/installation fee.

4.2.3. Linux Patches

In addition to standard Embedded Linux support, EMAC has released a number of patches and device drivers from the open-source community and from internal EMAC engineering into its standard distribution. Along with kernel patches, EMAC provides the binaries for the kernel and root file system.

4.3. Qt Creator

Qt Creator is a cross-platform IDE (Integrated Development Environment) tailored to the needs of Qt developers but works well for Headless applications as well. EMAC provides sample code as projects that can be imported into Qt Creator. Qt Creator supports remote deployment and source debugging.

http://wiki.qt.io/Main

4.4. ARM EABI Cross Compiler

The popular open source gcc compiler has a stable build for the ARM family. EMAC uses the 4.9.1 version of the ARM EABI compiler. The Embedded Linux kernel and EMAC Qt Creator projects use this compiler for building ARM stand alone, and OS specific binaries. The EMAC Qt Creator provides source level debugging over Ethernet or serial using gdbserver. The Linux binaries for the ARM EABI cross compiler are available online along with the SDK. See the EMAC wiki for further information.