SoM-iMX6U

User Manual

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1 Introduction

This document describes EMAC's SoM-iMX6U System-on-Module (SoM). TheSoM-iMX6U is designed to be compatible with EMAC's 144-pin SODIMM form factor. This module is built around the Freescale/NXP i.MX 6UltraLite (MCIMX6G1) Cortex A7 528MHz processor, which provides several of its key features.

The SoM-iMX6U has onboard Ethernet PHY, 5 serial ports, 2 USB 2.0 ports, 1 I2S audio port, 1 SDIO SD port, 1 I2C port, 2 CAN port, an internal real time clock (RTC), a programmable clock synthesizer, onboard eMMC flash, a Serial NOR Flash and LPDDR2 RAM.

In addition to the standard SoM features, the SoM- iMX6U also features a fast 32-bit core, open source software support, and a wide range of controller I/O pins.

1.1 Features

- Small, 144 pin SODIMM form factor (2.66" x 1.5")
- NXP ARM Cortex-A7 MCIMX6G1CVM05AA 528MHz Processor
- 10/100 BaseT Ethernet with on-board PHY
- 16 bit External Bus Interface
- 4 Serial RS232 ports and 1 Serial RS232/422/485 port
- 2 USB 2.0 (High Speed) OTG ports
- 512/128 MB LPDDR2
- 4 GB of Resident eMMC Flash
- 16 MB of Serial Data Flash
- Battery-backed Real-Time Clock
- SD/MMC Flash Card Interface
- 1 SPI port
- 1 I2C port
- 1 I2S Audio port
- 2 CAN Bus Interface
- Timer/Counters and Pulse Width Modulation (PWM) ports
- 4-Channel 12-bit Analog-to-Digital Converter
- Typical power requirement: 3.3V @ 170 mA
- JTAG for debug, including real-time trace
- FREE QT Creator IDE with GCC and GDB development tools

2 Hardware

2.1 Specifications

- **CPU:** Embedded NXP MCIMX6G1CVM05AA processor running at 528 MHz
- **Flash:** 4 GB eMMC Flash and 16 MB of Serial NOR Flash
- **RAM:** 512/128 MB LPDDR2
- **Flash Disk:** 4-bit Parallel or SPI serial SDHC/MMC interface
- **System Reset:** Supervisor with external Reset Button provision
- **RTC:** Real-Time Clock with battery-backed provision using 32-bit free running counter
- **Timer/Counters:** 2, 3-channel , 32-bit timers/counters with capture, compare, and PWM
- **Watchdog Timer:** External Watchdog Timer (MAX6747)
- **Digital I/O:** 18 General Purpose I/Os with 16mA drive when used as an output
- **Analog I/O:** 4-channel, 12-bit Analog-to-Digital Converter (ADC)
- **Power:** Power Management Controller allows selectively shutting down on-processor I/O functionality and running from a slow clock
- **JTAG:** JTAG for debug, including real-time trace
- **Clocks:** PLL synthesized 8 MHz, 200 KHz, and 14.3 MHz clock outputs

Serial Interfaces

- **UARTS:** 4 Serial RS232 ports with no handshaking and 1 Serial RS232/422/485 port with handshaking
- **SPI:** 1 High-Speed SPI port with chip select
- **Audio:** I2S Synchronous Serial Controller with Analog interface support
- **USB:** 2 USB 2.0 High-Speed OTG ports

Ethernet Interface

- **MAC:** MCIMX6G1CVM05AA on chip MAC
- **PHY:** Micrel KSZ8081 low power PHY with software shutdown and slow clock modes
- **Interface:** IEEE 802.3u 10/100 BaseT Fast Ethernet (requires external magnetics and Jack)

Bus Interface:

- Local ARM MCIMX6G1CVM05AA Bus accessible through SODIMM provides 8 address lines, 16 data bus lines, and control lines.

Mechanical and Environmental

- **Dimensions:** SODIMM form factor with the length dimension extended (2.66" x 1.5")
- **Power Supply Voltage:** +3.3 Volts DC +/- 5%
- **Power Requirements (typical):**
  - Typical 3.3 Volts @ 170mA (0.56 watts)
  - Max current draw during boot process: 300 mA
  - Constant busy loop: 240 mA
  - Idle system: 170 mA
  - APM sleep mode with Ethernet PHY disabled: 3.60 mA
- **Operating Temperature:** -40 ~ 85° C (-40 ~ 185 ° F), fan-less operation
- **Operating Humidity:** 0% ~ 90% relative humidity, non-condensing

2.2 Real-Time Clock

The SoM-iMX6U has an embedded Real-time Clock. Battery backup is provided from the carrier board using the VSTBY pin. The SoM-iMX6U will retain the RTT value register during reset and hence use it as a RTC. The RTC has the provision to set alarms that can interrupt the processor. For example, the processor can be placed in sleep mode and then later awakened using the alarm function.

2.3 Watchdog Timer

The SoM-iMX6U provides an external Watchdog Timer/ Supervisor (MAX6747) with an extended watchdog timeout period of 1.42 seconds (±10%). Upon power-up the Watchdog is disabled and does not require pulsing. To start the Watchdog, it must first be enabled. This is done by configuring port line CSI_HSYNC as an output and setting it low in software. Once enabled, the Watchdog should be pulsed, using port line LCD_DATA02, continually every 1.28 seconds or faster to prevent the Watchdog from timing out and resetting the module. If the user is using the watchdog to force a system reset, the watchdog may need up to 1.56 seconds of inactivity before the watchdog reset will occur. The watchdog is automatically disabled upon reset but it can also be disabled by setting CSI_HSYNC high.

2.4 External Connections

The SoM-iMX6U connects to a carrier board containing its connectors, power supply and any expansion I/O, through a standard ENIG-plated (Electroless Nickel Immersion Gold) SODIMM 144 pin connection (top half shown below).

The SoM model will fit in any standard 144-pin SODIMM socket. These connections are designed to be compatible with all EMAC 144-pin SoM products. See EMAC SoM 144-pin SODIMM pin-out Specification to see how other 144-pin SoMs pin-outs line up with the SoM-A5D35's pin-out.

The use of the SODIMM form-factor for EMAC's SoMs is a sound choice that has been proven rugged and reliable in the laptop market.

2.4.1 External Bus

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
100	GP_CS1	CSI_MCLK /EIM_CS0#	General Purpose Processor Chip Select CS0
98	GP_CS2	~NAND READY /EIM_CS1#	General Purpose Processor Chip Select CS1
108	GP_CS3	LCD_CLK /EIM_CS2#	General Purpose Processor Chip Select CS2
16	~OE	CSI_PIXCLK	Read Signal
83	~WR	CSI_VSYNC	Write Signal
6	~RST_IN	~SOM_RST_OUT	Processor Reset
43	~RST_OUT	~ POR	Processor Reset
85	Flash WP	Serial Flash WP	Serial Flash Write Protect
26,35,33,31, 28,109,111, 113	A0-A7	A0-A7	Address Bus
29,27,25,22, 23,21,19,20, 8,24,34,70, 77,81,84,86	D0-D15	D0-D15	Data Bus

2.4.2 JTAG

The SoM specification allows for access to the JTAG lines for the MCIMX6G1CVM05AA processor. These connections are used for the I2S interface; custom software will need to be deployed to enable the JTAG lines' capability to debug software.

Processor JTAG

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
139	JTAG_TCK	JTAG_TCK	JTAG clock
137	JTAG_TDI	JTAG_TDI	JTAG serial in
138	JTAG_TDO	JTAG_TDO	JTAG serial out
140	JTAG_TMS	JTAG_TMS	JTAG operation mode
112	JTAG_TRST	~JTAG_TRST	Test Reset Signal

2.4.3 One-Wire / I2C

The SoM specification calls for a one-wire port. Since the SoM-iMX6U does not have a one-wire port, this line is not connected for One-Wire Operation. The MCIMX6G1CVM05AA processor does provide an I2C bus and so these pins are dedicated to that function although they can also be used as GPIOs.

One-Wire / I2C Port

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
116	LOCAL1W /SCL	GPIO1_IO02	I2C Clock
88	SDA	GPIO1_IO03	I2C Data

2.4.4 Ethernet

The SoM-iMX6U provides a Micrel KSZ8081 Low Power Ethernet RMII PHY IC on board. Carrier designers need only run these lines through the appropriate magnetics layer to have a functional Ethernet connection. Remember the RX and TX lines are differential pairs and need to be routed as such.

The LED/configuration pins' state at reset determines the Ethernet's configuration (10-baseT, 100-baseT, autoconfig) and the function of the LED's. The SoM-100ES and the SoM-150ES pull them all high, which configures the chip for network autoconfig, with LED0 functioning as active low link, and LED1 is functioning as active low Rx Activity (Refer to Carrier schematics).

The Ethernet PHY can be put into a low power mode by writing directly to the MAC via software.

Additional power can be saved by turning off the PHY Oscillator. This is done by setting GPIO1_IO00 low. Make sure to send software commands to the PHY to put it into slow clock and power-down mode before shutting off the Oscillator. When restoring the PHY first turn the Oscillator on and disable slow clock mode before accessing the PHY.

Ethernet

SODIMM Pin#	SoM Pin Name	{PHY} Pin Name	Description
89	LED1_LINK	LED0/NWAYEN	Ethernet Link LED Configuration Pin
90	LED2_ACT	LED1/SPEED	Ethernet Activity LED Configuration pin
94	Ethernet_Rx-	RXM	Low differential Ethernet receive line
92	Ethernet_Rx+	RXP	High differential Ethernet receive line
93	Ethernet_Tx-	TXM	Low differential Ethernet transmit line
91	Ethernet_Tx+	TXP	High differential Ethernet transmit line

2.4.5 USB

The SoM-iMX6U provides 1 High speed USB 2.0 Host ports and 1 High Speed USB 2.0 Device/Host port. The USB Device/Host port can be used as an "On-The-Go"-like port on custom carriers. The Device/Host port is connected to a USB Type B connector on the SoM-100ES and SoM-150ES carrier boards.

USB

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
64	USB_D+	USB_OTG1_DP	Host, High Speed USB 1
66	USB_D-	USB_OTG1_DN	Host, High Speed USB 1
60	USB/OTG_D-	USB_OTG2_DN	Device/Host, HS USB 2
61	USB/OTG_D+	USB_OTG2_DP	Device/Host, HS USB 2
45	USB_OTG_VBUS	USB_OTG1_VBUS /USB_OTG2_VBUS	USB OTG VBUS Detect

2.4.6 SPI

The MCIMX6G1CVM05AA processor provides a dual (SPI3 and SPI4) SPI module for communicating with peripheral devices. On the SoM the SPI4 bus is already connected to the serial flash, which uses SPI4_CS0# (SPI4_CS0# is not brought out to the card fingers). The first Table below lists the lines for the #4 SPI module. The SoM pin specification allows for three SPI chip selects. The SPI chip selects available to the card edge are SPI_CS0#, SPI_CS1#, and SPI_CS2#. The second Table below lists the lines for the #3 SPI module.

Serial Peripheral Interface

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
122	SPI4_MI	ENET2_TX_CLK	SPIO4 serial data in
121	SPI4_MO	ENET2_TX_EN	SPIO4 serial data out
120	SPI4_SCK	ENET_TX_DATA1	SPIO4 serial clock out
123	SPI4_CS0#	ENET2_RX_EN	SPIO4 slave select line 0
124	SPI4_CS1#	ENET2_TX_DATA0	SPIO4 slave select line 1
110	SPI4_CS2#	LCD_DATA04	SPIO4 slave select line 2

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
133	SPI3_MISO/GPIO	NAND CLE	SPIO3 serial data in/GPIO
134	SPI3_MOSI/GPIO	~NAND_CE1	SPIO3 serial data out/GPIO
135	SPI3_SCK/GPIO	~NAND_CE0	SPIO3 serial clock out/GPIO
136	SPI3_CS0#/GPIO	NAND_ALE	SPIO3 slave select line 0/GPIO
105	SPI3_CS1#/GPIO	GPIO1_IO1	SPIO3 slave select line 1/GPIO

2.4.7 MCI Multimedia Card / SDIO

The MCIMX6G1CVM05AA processor provides a 4-bit MMC/SD card interface using the MC lines.

The SoM-100ES Carrier board uses a serial SPI based MMC/SD interface. The SoM-iMX6U could be programmed to use this serial interface, however the drivers provided are written to utilize the 4-bit interface and as such require the SoM-150ES Carrier board to use these drivers.

MMC/SD Card Interface

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
54	SD_CLK	~NAND_RE	SD Clock
51	SD_CMD	~NAND_WE	SD Command
50	SD_DA0	NAND_DATA00	SD Data 0
55	SD_DA1	NAND_DATA01	SD Data 1
56	SD_DA2	NAND_DATA02	SD Data 2
57	SD_DA3	NAND_DATA03	SD Data 3
42	SD_CD	~NAND_WP	SD Card Detect

2.4.8 Serial Ports

The SoM-144 pin specification has the provision for 4 serial ports. However, the MCIMX6G1CVM05AA provides 5 serial ports so the 2 additional serial ports are accommodated through the use of alternate SoM pins.

Serial Ports

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
71	COMA_RXD	UART3_RX_DATA	UART3 Receive/GPIO
73	COMA_TXD	UART3_TX_DATA	UART3 Transmit/GPIO
38	COMB_RXD	UART2_RX_DATA	UART2 Receive/GPIO
36	COMB_TXD	UART2_TX_DATA	UART2 Transmit/GPIO
82	COMB_RTS/GPIO	~UART2_RTS	UART2 RTS/GPIO
78	COMB_CTS/GPIO	~UART2_CTS	UART2 CTS/GPIO
103	COMC_RXD	UART1_RX_DATA	UART1 Receive/GPIO
102	COMC_TXD	UART1_TX_DATA	UART1 Transmit/GPIO
107	COMC_DSR/GPIO	NAND_DATA05	UART1 DSR /GPIO
106	COMC_DTR/GPIO	NAND_DATA06	UART1 DTR/GPIO
76	COMC_RI/GPIO	NAND_DATA07	UART1 RING/GPIO
30	COMC_DCD/GPIO	NAND_DATA04	UART1 DCD/GPIO
39	COMC_RTS/GPIO	~UART1_RTS	UART1 RTS/GPIO
79	COMC_CTS/GPIO	~UART1_CTS	UART1 CTS/GPIO
46	Debug RXD	UART5_RX_DATA	Debug Receive / GPIO
47	Debug TXD	UART5_TX_DATA	Debug Transmit / GPIO
49	COMD RXD	UART4_RX_DATA	UART4 Receive / GPIO
48	COMD TXD	UART4_TX_DATA	UART4 Transmit / GPIO

2.4.9 I2S

The SoM-iMX6U provides an I2S serial interface for connecting to an audio codec.

I2S

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
87	I2S_TXCK	JTAG_TMS	Transmit Clock/GPIO
80	I2S_LRCK	JTAG_TDO	Transmit Frame / GPIO
125	I2S_RXD	JTAG_TCK	Serial Receive Data / GPIO
126	I2S_TXD	~JTAG_TRST	Serial Transmit Data / GPIO
128	I2S_RF	JTAG_TDI	Receive Frame / GPIO
127	I2S_RXCK		Receive Clock / GPIO

2.4.10 CAN

The MCIMX6G1CVM05AA has two CAN controllers that are brought out to the SoM card edge. One is defined by the SoM specification and the second can be utilized instead of the serial port COM B control lines. The SoM specified CAN port can be used as GPIO if desired.

CAN

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
96	CANTX	~UART3_CTS	CAN Transmit / GPIO
95	CANRX	~UART3_RTS	CAN Receive / GPIO

Additional CAN Port

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
78	COMB_CTS	~UART2_CTS	CAN Receive / UART2 CTS
82	COMB_RTS	~UART2_RTS	CAN Transmit / UART2 RTS

2.4.11 GPIO

This section provides for the SoM general purpose IO section (GPIO). All of these pins can be configured to be general-purpose digital ports. These pins often have other capabilities besides GPIO as well but be aware that these additional capabilities cannot always be guaranteed to be shared between different pin-compatible EMAC SoMs.

Interrupts:

The MCIMX6G1CVM05AA is capable of using any GPIO pin as an interrupt as well as the pins that are labeled IRQ. The 144-Pin SoM Specification defines 3 IRQs.

Interrupt Lines

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
75	IRQA/GPIO_1	LCD_VSYNC	Interrupt A / GPIO 1
32	IRQB/GPIO_2	LCD_RESET	Interrupt B / GPIO 2
40	IRQC/GPIO_0	LCD_HSYNC	Interrupt C / GPIO 0

A/D:

The MCIMX6G1CVM05AA Analog to Digital pins provides 4 channels of 12-bit resolution with a 1 us conversion time. With the enhanced DSP extensions, this can make quite a capable signal processor. The Analog to Digital Reference Voltage is enabled by default, but can be controlled by LCD_DATA03. LCD_DATA03 configured as an input disables the reference, or it can be enabled by configuring it as an output and driving it low.

Analog to Digital Converters

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
129	AD1/GPIO_5	GPIO1_IO06	ADC CH1 / GPIO 5
130	AD2/GPIO_6	GPIO1_IO07	ADC CH2 / GPIO 6
131	AD3/GPIO_7	GPIO1_IO08	ADC CH3 / GPIO 7
132	AD4/GPIO_8	GPIO1_IO09	ADC CH4 / GPIO 8

Timer/Counters:

The general-purpose Timer/Counter (TC) module on the MCIMX6G1CVM05AA is comprised of six 32-bit timer/counter channels with independently programmable input capture or output compare lines. These can be used for a wide variety of timed applications, including counters and PWM.

Timers/Counters

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
117	CLK1/GPIO_3	GPIO1_IO04	Programmable Clock / GPIO 3
127	CLK2/GPIO_4	GPIO1_IO05	Programmable Clock / GPIO 4
114	PWM1/GPIO_14	LCD_DATA00	PWM / Clock / GPIO 14
115	PWM2/GPIO_15	LCD_DATA01	PWM / Clock / GPIO 15

GPIOs:

General Purpose IO

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
40	IRQC/GPIO_0	LCD_HSYNC	Interrupt C / GPIO 0
75	IRQA/GPIO_1	LCD_VSYNC	Interrupt A / GPIO 1
32	IRQB/GPIO_2	LCD_RESET	Interrupt B / GPIO 2
117	CLK1/GPIO_3	GPIO1_IO04	Programmable Clock / GPIO 3
127	CLK2/GPIO_4	GPIO1_IO05	Programmable Clock / GPIO 4
129	AD1/GPIO_5	GPIO1_IO06	ADC CH1 / GPIO 5
130	AD2/GPIO_6	GPIO1_IO07	ADC CH2 / GPIO 6
131	AD3/GPIO_7	GPIO1_IO08	ADC CH3 / GPIO 7
132	AD4/GPIO_8	GPIO1_IO09	ADC CH4 / GPIO 8
133	SPI3_MI/GPIO_9	NAND_CLE	SPI3 Master In / GPIO 9
134	SPI3_MO/GPIO_10	~NAND_CE1	SPI3 Master Out / GPIO 10
135	SPI3_SCK/GPIO_11	~NAND_CE0	SPI3 Serial Clock / GPIO 11
136	SPI3_CS0/GPIO_12	NAND_ALE	SPI3 Chip Select 0 / GPIO 12
105	SPI3_CS1/GPIO_13	GPIO1_IO01	SPI3 Chip Select 1 / GPIO 13
114	PWM1/GPIO_14	LCD_DATA00	PWM / Clock / GPIO 14
115	PWM2/GPIO_15	LCD_DATA01	PWM / Clock / GPIO 15
48	COMD TXD/GPIO_16	UART4_TX_DATA	COM D Transmit / GPIO
49	COMD RXD/GPIO_17	UART4_RX_DATA	COM D Receive / GPIO

2.5 Power Connections

The SoM-iMX6U requires a 3.3V supply for the Bus and I/O voltages. The 1.35V core voltage is regulated on module from the 3.3V. The on-processor RTC also requires 3.3V supplied by either a battery or the 3.3V power rail. The 5.0V USB VBUS voltage is regulated on module from 3.3V.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
3,4,141,142	3.3VCC	3.3VCC	3.3 Volt I/O voltage to the processor
1,2,52,53, 58,59,62,63,68,69,143, 144	GND	GND	Ground
119	VSTBY	VDD_SNVS_IN	The SNVS regulator takes the SNVS_IN supply and generates the SNVS_CAP supply, which powers the real time clock and SNVS blocks
118	ALT_VCC	USB_OTG1_VBUS USB_OTG2_VBUS	To control PMIC to supply VBUS voltage
101	AV_VCC	Not Used	Analog power. This is not required for the SoM-iMX6U
99	V_REF	ADC_VREFH	ADC Voltage reference high

2.6 Boot Options

The SoM specification provides two pins for boot time configuration, BOOT_OPTION1 and BOOT_OPTION2. On the SoM-iMX6U, these are BMS1 and BMS2. The Boot Mode Select (BMS) pins allow the SoM-iMX6U to be low-level booted from either its internal ROM or USB.

The Module can high-level boot from either the Serial Flash or the eMMC (selected through the low-level boot loader). It is recommended to high-level boot from the Serial Flash.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
41	BOOT_OPTION1	LCD_DATA05	Boot Mode Select 1
74	BOOT_OPTION2	LCD_DATA06	Boot Mode Select 2

2.7 Serial Data Flash

The Serial Data Flash is connected to SPI4 and uses ENET2_RX_ER to enable it. The Serial Data Flash also has a Write Protect Provision. To Write Protect the Serial Data Flash pull SoM pin# 85 low. This pin is pulled up by a 10K ohm resistor on the module.

If this feature is required, it would be implemented on the carrier as a jumper or an I/O line.

2.8 Module Status LED

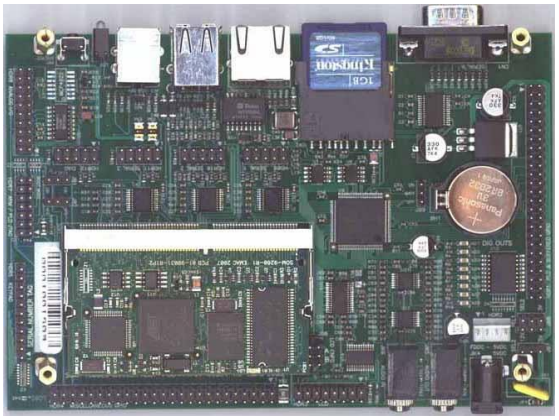
A green status LED (labeled LD1) is active-low and is controlled by port line NAND_DQS.

3 Design Considerations

One of the goals of the SoM-iMX6U is to provide a modular, flexible and inexpensive solution capable of delivering high-end microcontroller performance with low power requirements.

3.1 The EMAC SoM Carrier SoM-150ES

EMAC provides an off-the-shelf carrier for the SoM-iMX6U module, the SoM-150ES, which provides power to SoM modules and provides them with an extended range of I/O. This board comes with full schematics and BOM, and can be used as is, or as a reference for a customer's own design.



http://www.emacinc.com/products/system_on_module/SoM-150ES

EMAC also offers a semi-custom engineering service. By modifying an existing design, EMAC can offer quick-turn, low-cost engineering, for your specific application.

3.2 Power

The SoM-iMX6U requires a voltage of 3.3V at 170mA. For a bare-bones population, users can get away with using only 3.3V, and simply provide this to all the voltage inputs listed in Power Connections section.

3.2.1 Legacy

ALT_VCC is a legacy connection, required to support the SoM-400EM and may be used in future SoM modules. The SoM-iMX6U does not use this connection, so if general SoM compatibility is not an issue then this can be tied to 3.3V in a carrier designed for this SoM.

3.2.2 Battery Backup

The SoM-iMX6U real-time clock (RTC) requires a backup voltage to maintain its data. This backup voltage comes from the VSTBY pin, and should be connected to 3.3 volts.

The RTC will draw approximately 40uA when the processor is not powered by the 3.3V supply. When the module is powered no current is drawn from the backup battery supply. If the RTC is not needed, this can be tied to 3.3V.

The SoM-100ES and SoM-150ES provide battery backup voltage through a BR2032, which is a standard 3V 190mA/H 20MM coin battery that can be picked up from most electronics stores.

3.2.3 Analog Reference

No external Analog Reference voltage (VREF) is required for the SoM-iMX6U so this pin is normally a No Connect on the Module. An on-module 2.5V reference is provided. Analog input range is therefore 0 to 2.5V.

This Reference uses power and therefore can be turned off by setting LCD_DATA03 to a high, thus conserving about 2.2mA.

3.2.4 Analog Voltage

When designing power for the Analog subsystem there are two main considerations: range and accuracy.

- **Range**
  The AVCC normally will have an effect on the range, however, on the SoM-iMX6U this pin is a no-connect since the processor's Analog VCC (ADC_VREFH) is directly connected to a filtered 3.3V. This voltage reference defines the voltage range of the A/D convertor.

- **Accuracy**
  The accuracy of the A/D converters is determined by the voltage reference that is provided to the analog subsystem. Since the stability of the voltage between this reference and ground will affect the accuracy of the subsystem's measurements, this has been built into the SoM in this design. No external Analog Reference voltage is required for the SoM-iMX6U.

4 Software

The SoM-iMX6U offers a wide variety of software support from both open source and proprietary sources. The hardware core was designed to be software compatible with the NXP MCIMX6G1CVM05AA reference design, which is supported by Linux.

For more information on software support, please visit the EMAC Wiki Software Section at:

http://wiki.emacinc.com/wiki/product_wiki

4.1 Das U-Boot

EMAC utilizes Das U-Boot for its ARM based products. U-Boot is an open source/cross-architecture platform independent bootloader. It supports reading and writing to the flash, auto-booting, environmental variables, and TFTP. Das U-boot can be used to upload and run and/or reflash the OS or to run stand-alone programs without an OS. Products are shipped with a valid MAC address installed in flash in the protected U-boot environmental variable “ethaddr”. At boot time U-Boot automatically stores this address in a register within the MAC, which effectively provides it to any OS loaded after that point.

4.2 Embedded Linux

EMAC Open Embedded Linux is an open source Linux distribution for use in embedded systems. The EMAC OE Linux Build is based on the Open Embedded (www.openembedded.org) Linux build system. Open Embedded is a superior Linux distribution for embedded systems. Custom Linux builds are also available on request.

The distribution contains everything a user could expect from a standard Linux kernel: powerful networking features, advanced file system support, security, debugging utilities, and countless other features.

The basic root file system includes:

- Busybox
- Hotplugging support
- APM utilities for power management
- Openssh SSH server
- lighttpd HTTP server
- JJFS2 or EXT4 file system with utilities

4.2.1 Linux with Xenomai Real Time Extensions

Xenomai provides real time extensions to the kernel and can be used to schedule tasks with hard deadlines and µs latencies. The Xenomai build is an additional module that can be added to the standard Linux kernel and is available for a one-time inexpensive support/installation fee.

http://www.xenomai.org/

4.2.2 Linux Packages

EMAC provides support for many Linux Packages such as: PHP, SQLite, Perl, SNMP, DHCP Server, etc. As with the Xenomai Package, other Packages can be added to the standard Linux file system and are available for a one-time inexpensive support/installation fee.

4.2.3 Linux Patches

In addition to standard Embedded Linux support, EMAC has released a number of patches and device drivers from the open source community and from internal EMAC engineering into its standard distribution. Along with kernel patches, EMAC provides the binaries for the kernel and root file system.

4.3 Qt Creator

Qt Creator is a cross-platform IDE (Integrated Development Environment) tailored to the needs of Qt developers but works well for Headless applications as well. EMAC provides sample code as projects that can be imported into Qt Creator. Qt Creator supports remote deployment and source debugging.

https://qt-project.org/wiki/Category:Tools::QtCreator

4.4 ARM EABI Cross Compiler

The popular open source gcc compiler has a stable build for the ARM family. EMAC uses the 4.9.1 version of the ARM EABI compiler. The Embedded Linux kernel and EMAC Qt Creator projects use this compiler for building ARM stand alone, and OS specific binaries. The EMAC Qt Creator provides source level debugging over Ethernet or serial using gdbserver. The Linux binaries for the ARM EABI cross compiler are available online along with the SDK. See the EMAC wiki for further information.