SoM-iMX6M

User Manual

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Revision 1.20

(for use with Rev 5 boards or newer)

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1 Introduction

This document describes EMAC's SoM-iMX6M System on Module (SoM). The SoM-iMX6M is a System on Module, designed to be compatible with EMAC's 314-pin SODIMM form factor. This module is built around the Freescale/NXP/Qualcomm i.MX6 microcontroller, which provides several of its key features.

The SoM-iMX6M comes with either a single, dual, or quad core processor to suit a wide variety of needs. The SoM has Gigabit Ethernet, PCIe, and SATA interfaces. There are two SDIO/MMC ports, two SPI ports and two I2S ports. There are four RS232 serial ports available, three with RTS/CTS handshaking and one with full handshaking. Any of these four ports can be configured for RS485 hardware flow control. There are two high speed USB 2.0 host ports and one high speed USB 2.0 OTG port. The SoM has support for three different video interfaces that include HDMI, 24-bit LVDS and DSI. The SoM-iMX6M also has a CSI interface for video capture. There are two CAN interfaces and two I2C interfaces along with a battery charge control interface. The SoM has 22 GPIO pins, four of which support PWM and two are for a general-purpose timer.

In addition to the standard SoM features, the SoM-iMX6M also features open source software support and a wide range of controller I/O pins.

1.1 Features

- **Freescale i.MX6 Microcontroller**
- **Multiple Video Output Including HDMI, LVDS and DSI**
- **Video Input Support Through CSI**
- **Gigabit Ethernet**
- **High Speed USB 2.0**
- **SATA II**
- **PCIe**
- **SDIO/MMC**
- **I2S/AC97 Audio**
- **I2C**
- **SPI**
- **CAN**
- **RS232 Serial Ports**
- **Various GPIO**

2 Hardware

2.1 Specifications

Microcontroller

- **CPU: Single/Dual/Quad ARM™ Cortex™ -A9 MPcore with Cortex-A9 NEON MPE**

Memory

- **Flash: 16MB Serial NOR Flash**
- **RAM: Up to 2GB DDR3 @ 800MHz**
- **eMMC: Up to 8GB of Onboard eMMC**

Video

- **LVDS: 1 24bit, 165 Mpixels/sec, LVDS Interface**
- **HDMI: 1 HDMI 1.4 Port**
- **MIPI/DSI: 2 Lanes @ 1Gbps**
- **MIPI/CSI: 4 Lanes @ 1Gbps Each**

Serial Interfaces

- **UARTS: 4 Serial Ports, 3 with RTS/CTS Handshaking and 1 with Full Handshaking**
- **SPI: 2 Serial Peripheral Interfaces with 3 Chip Selects Each**
- **USB: 2 USB 2.0 High Speed Host Ports and 1 USB 2.0 High Speed OTG Port**
- **PCI: 1 Lane PCIe (Gen 2.0)**
- **I2C: 2 General Use 400Kbps I2C Ports and Dedicated I2C Ports for LVDS and HDMI Interfaces**
- **I2S: 2 I2S/AC97 Audio Interfaces up to 1.4Mbps Each**

Ethernet Interface

- **MAC: i.MX6 MAC Utilizing RGMII Interface**
- **PHY: Micrel KSZ9031 Gigabit Ethernet PHY**
- **Interface: Media Dependent Interface (MDI)**

Miscellaneous

- **SDIO/MMC: 2 4bit SDIO/MMC Interfaces Supporting SDHC Cards up to 32GB**
- **Reset: MAX6747 Watchdog Timer and Reset Supervisor**
- **RTC: DS1337U Real Time Clock**
- **Timer/Counters: 1 General Purpose Timer Counter with Dedicated Clock Input**
- **PWM: 4 Channels of PWM Output**
- **Watchdog Timer: MAX6747 Watchdog Timer and Reset Supervisor**
- **Digital I/O: 22 General Purpose Input/Output lines**
- **Analog I/O: 4 Channel 12-bit Analog to Digital Converter**
- **Power: Single 5.0V Supply**
- **JTAG: Processor JTAG Supporting Programming, Trace and Boundary Scan**
- **Clocks: 24MHz Main Oscillator and a 32.768KHz RTC Oscillator**

Mechanical and Environmental

- **Dimensions: 82.0 x 60.0 mm**
- **Power Supply Voltage: 5.0 VDC**
- **Power Requirements (typical, dual-core):**
  - 5.0 Volts @ 3.0A
  - Max current draw during boot process: 900mA
  - Constant busy loop: 1200mA
  - Idle system: 550mA
  - Idle system with Ethernet PHY disabled: TBD
  - APM sleep mode with Ethernet PHY disabled: TBD
  - APM sleep mode with Ethernet PHY enabled: TBD
- **Operating Temperature:** 0 ~ 95°C, -25 ~ 85°C**,** -40 ~ 85° C Options, fanless operation
- **Operating Humidity:** 0% ~ 90% relative humidity, non-condensing

2.2 Real-Time Clock

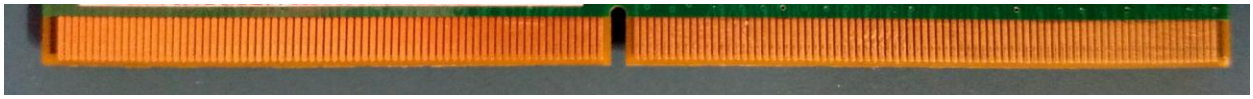
The SoM-iMX6M provides a real time clock through the use of a DS1337 Real Time Clock chip. The RTC is powered from a Lithium Ion battery supplied on the carrier. There is a dedicated 32.768KHz oscillator on the SoM-iMX6M to drive the RTC.

2.3 Watchdog Timer

A Watchdog timer is provided on the SoM-iMX6M by use of a MAX6747 Watchdog Timer and Reset Supervisor. The WDT is set for a timeout of approximately 1.4 seconds. The WDT can be enabled by writing GPIO1_IO25 low. The WDT is pulsed by using processor pin GPIO1_IO22.

2.4 External Connections

All external connections to the SoM-iMX6M are provided through a 314-pin card edge connector. The SoM utilizes an MM70-314 or equivalent connector on a carrier board to provide access to the various processor interfaces.



2.4.1 JTAG

The SoM-iMX6M provides access to the i.MX6's JTAG interface for programming and debugging. Supports IEEE P149.1 and 1149.6.

Table 1: Processor JTAG

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
46	JTAG_MOD	JTAG_MOD	N/A	JTAG Operation Mode
50	JTAG_TCK	JTAG_TCK	N/A	JTAG Clock
52	JTAG_TDI	JTAG_TDI	N/A	JTAG Serial In
56	JTAG_TDO	JTAG_TDO	N/A	JTAG Serial Out
58	JTAG_TMS	JTAG_TMS	N/A	JTAG Test Mode Select
62	JTAG_TRSTB	JTAG_TRST	N/A	Test Reset Signal

2.4.2 System Control

There are ten pins provided for system control. These include power and reset as well as boot mode selection (see i.MX6 datasheet for details on boot modes). The RST_IN# and RST_OUT# are buffered through the MAX6747 reset supervisor IC. There is a write protect line that connects directly to the serial NOR flash. This line is active low and is pulled up on the SoM through a 10K Ohm resistor.

Table 2: System Control

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
252	ON/OFF	ON/OFF	N/A	On/Off Power button
253	S5	N/A	N/A	Power State S5
251	S3	N/A	N/A	Power State S3
74	BOOT_0	BOOT_MODE0	GPIO3_IO06	Processor Boot Options Select 0
76	BOOT_1	BOOT_MODE1	N/A	Processor Boot Options Select 1
276	MS1	BOOT_MODE2	GPIO3_IO05	Additional Boot Options Select 2
278	MS2	BOOT_MODE3	N/A	Additional Boot Options Select 3
254	RESET_IN#	POR_B	N/A	Reset In (active low)
182	RESET_OUT#	POR_B	N/A	Reset Out (active low)
279	WP#	N/A	N/A	Serial Flash Write Protect (active

2.4.3 One-Wire / I2C

The SoM-iMX6M provides two I2C serial ports. Both are capable of 400kbps communication speeds. The I2C data and clock lines are pulled up to 3.3V through 4.7K resistors on the SoM so that none are required on the carrier.

Table 3: I2C A

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
231	I2C_A_SCL	CSI0_DATA09/I2C1_SCL	GPIO5_IO27	Two Wire Serial Interface Clock
233	I2C_A_SDA	CSI0_DATA08/I2C1_SDA	GPIO5_IO26	Two Wire Serial Interface Data

Table 4: I2C B

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
235	I2C_B_SCL	EIB_EB2/I2C2_SCL	GPIO2_IO30	Two Wire Serial Interface Clock
237	I2C_B_SDA	EIM_DATA16/I2C2_SDA	GPIO3_IO16	Two Wire Serial Interface Data

2.4.4 Ethernet

The SoM-iMX6M provides for 10/100/1000 BaseT Ethernet. The SoM is equipped with a Micrel KSZ9031 physical layer that is routed out to the card edge. A 1:1 Gigabit Ethernet transformer is required on the carrier board between the SoM and an RJ45 jack. The KSZ9031 provides on chip termination for the four Ethernet differential pairs so none are required on the carrier. An active low Ethernet Link and Activity LED signal is provided by the KSZ9031 and routed to the card edge. While EMAC's EM4C SoM Specification provides for dual Gigabit Ethernet the SoM-iMX6M only provides one.

Table 5: Ethernet A

SODIMM Pin#	SoM Pin Name	KSZ9031 Pin Name	Description
E4_3	GBE_A_MDI0-	TXRXA_N	Gigabit Ethernet Media Dependent Interface Pair A0-
E4_2	GBE_A_MDI0+	TXRXA_P	Gigabit Ethernet Media Dependent Interface Pair A0+
E4_6	GBE_A_MDI1-	TXRXB_N	Gigabit Ethernet Media Dependent Interface Pair A1-
E4_5	GBE_A_MDI1+	TXRXB_P	Gigabit Ethernet Media Dependent Interface Pair A1+
E3_3	GBE_A_MDI2-	TXRXC_N	Gigabit Ethernet Media Dependent Interface Pair A2-
E3_2	GBE_A_MDI2+	TXRXC_P	Gigabit Ethernet Media Dependent Interface Pair A2+
E3_6	GBE_A_MDI3-	TXRXD_N	Gigabit Ethernet Media Dependent Interface Pair A3-
E3_5	GBE_A_MDI3+	TXRXD_P	Gigabit Ethernet Media Dependent Interface Pair A3+
E3_7	LED0_A_ACT#	LED1/PHYAD	Ethernet Activity LED A, Active Low
E4_9	LED1_A_LINK1000#	N/C	Ethernet Link1000 Status A, Active Low
E4_8	LED2_A_LINK100#	LED2	Ethernet Link100 Status A, Active Low

Table 6: Ethernet B

SODIMM Pin#	SoM Pin Name	KSZ9031 Pin Name	Description
108	GBE_B_MDI0-	N/C	Gigabit Ethernet Media Dependent Interface Pair B0-
106	GBE_B_MDI0+	N/C	Gigabit Ethernet Media Dependent Interface Pair B0+
112	GBE_B_MDI1-	N/C	Gigabit Ethernet Media Dependent Interface Pair B1-
110	GBE_B_MDI1+	N/C	Gigabit Ethernet Media Dependent Interface Pair B1+
118	GBE_B_MDI2-	N/C	Gigabit Ethernet Media Dependent Interface Pair B2-
116	GBE_B_MDI2+	N/C	Gigabit Ethernet Media Dependent Interface Pair B2+
122	GBE_B_MDI3-	N/C	Gigabit Ethernet Media Dependent Interface Pair B3-
120	GBE_B_MDI3+	N/C	Gigabit Ethernet Media Dependent Interface Pair B3+
134	LED0_B_ACT#	N/C	Ethernet Activity LED B, Active Low
136	LED2_B_LINK100#	N/C	Ethernet Link1000 Status B, Active Low
138	LED1_B_LINK1000#	N/C	Ethernet Link100 Status B, Active Low

2.4.5 USB

The SoM-iMX6M has three USB 2.0 ports. The EM4C specification provides for two USB 3.0 ports however the i.MX6 processor only supports USB 2.0 through the 3.0 interface. All USB Super Speed lines are no connect. There is a high-speed USB 2.0 host/device port that supports OTG functionality. The USB OTG port is connected directly to the processor while the two host ports are achieved through the use of Microchip's USB2512 two port USB 2.0 hub controller. There are signals provided for USB OTG functionality as well as port power and over-current control for each USB port.

Table 7: USB 2.0 Host

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
70	USB_C_D+	N/C	N/C	USB 2.0 Host C Data+
72	USB_C_D-	N/C	N/C	USB 2.0 Host C Data-

Table 8: USB 2.0 Host/Device

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
64	USB_D_OTG_D+	USB_OTG_DP	N/A	USB 2.0 Host/Device D Data+
68	USB_D_OTG_D-	USB_OTG_DN	N/A	USB 2.0 Host/Device D Data-
84	OTG_PWR_EN	GPIO1	GPIO1_IO01	USB D On The Go Power Enable
161	USB_OTG_VBUS	USB_OTG_VBUS	N/A	USB D On The Go Voltage Bus
155	USB_OTG_ID	ENET_RX_ER	GPIO1_IO24	USB D On The Go Device ID

Table 9: USB 3.0 A

SODIMM Pin#	SoM Pin Name	USB Pin Name(s)	Port Line	Description
167	USB_A_SS_RX+	N/C	N/C	USB A Super Speed RX Data+
169	USB_A_SS_RX-	N/C	N/C	USB A Super Speed RX Data-
173	USB_A_SS_TX+	N/C	N/C	USB A Super Speed TX Data+
175	USB_A_SS_TX-	N/C	N/C	USB A Super Speed TX Data-
181	USB_A_D+	USBDP_DN1 (USB2512 Pin)	N/A	USB A Host 2.0/3.0 Data+
179	USB_A_D-	USBDM_DN1 (USB2512 Pin)	N/A	USB A Host 2.0/3.0 Data-

Table 10: USB 3.0 B

SODIMM Pin#	SoM Pin Name	USB Pin Name(s)	Port Line	Description
143	USB_B_SS_RX+	N/C	N/C	USB B Super Speed RX Data+
145	USB_B_SS_RX-	N/C	N/C	USB B Super Speed RX Data-
149	USB_B_SS_TX+	N/C	N/C	USB B Super Speed TX Data+
151	USB_B_SS_TX-	N/C	N/C	USB B Super Speed TX Data-
157	USB_B_D+	USBDP_DN2 (USB2512 Pin)	N/A	USB B Host 2.0/3.0 Data+
159	USB_B_D-	USBDM_DN2 (USB2512 Pin)	N/A	USB B Host 2.0/3.0 Data-

Table 11: USB 3.0 Control

SODIMM Pin#	SoM Pin Name	USB Pin Name(s)	Port Line	Description
163	USB_PWR_EN	PRTPWR1/PRTPWR2 (USB2512 Pin)	N/A	USB 3.0 Voltage Bus Enable
183	USB_VBUS	SD4_DATA7	GPIO2_IO15	USB 3.0 Voltage Bus Detect
139	USB_HUB_RST	RESET_N (USB2512 Pin)	N/A	Reset For external USB Hub
165	USB_OC_A	OCS_N1 (USB2512 Pin)	N/A	USB A Over Current Detect
141	USB_OC_B	OCS_N2 (USB2512 Pin)	N/A	USB B Over Current Detect

2.4.6 HSIC

The EM4C SoM Specification provides for two USB High Speed Inter-Chip interfaces. The SoM-iMX6M does not support HSIC and hence all the pins for both interfaces are no connects.

Table 12: HSIC

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
272	HSIC_A_STRB	N/C	N/C	USB High Speed Inter-Chip A Strobe
274	HSIC_A_DATA	N/C	N/C	USB High Speed Inter-Chip A Data
275	HSIC_B_STRB	N/C	N/C	USB High Speed Inter-Chip B Strobe
277	HSIC_B_DATA	N/C	N/C	USB High Speed Inter-Chip B Data

2.4.7 SPI

The SoM-iMX6M provides two Serial Peripheral Interface busses each with three slave select lines. While three slave selects are provided for each SPI interface, any processor GPIO pin may be used as a slave select line. The serial NOR flash is connected to the ECSPI3 bus and uses pin DISP0_DATA03/ECSPI3_SS0.

Table 13: Serial Peripheral Interface A

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
222	SPI_A_MOSI	CSI0_DATA05 / ECSPI1_MOSI	GPIO5_IO23	Serial Peripheral Interface A, Master Out Slave In
224	SPI_A_MISO	CSI0_DATA06 / ECSPI1_MISO	GPIO5_IO24	Serial Peripheral Interface A, Master In Slave Out
226	SPI_A_CLK	CSI0_DATA04 / ECSPI1_SCLK	GPIO5_IO22	Serial Peripheral Interface A, Serial Clock
228	SPI_A_CS0#	DISP0_DATA15 / ECSPI1_SS1	GPIO5_IO09	Serial Peripheral Interface A, Chip Select 0
230	SPI_A_CS1#	KEY_ROW2 / ECSPI1_SS2	GPIO4_IO11	Serial Peripheral Interface A, Chip Select 1
114	SPI_A_CS2#	GPIO16	GPIO7_IO11	Serial Peripheral Interface A, Chip Select 2

Table 14: Serial Peripheral Interface B

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
219	SPI_B_MOSI	DISP0_DATA01 / ECSPI3_MOSI	GPIO4_IO22	Serial Peripheral Interface B, Master Out Slave In
221	SPI_B_MISO	DISP0_DATA02 / ECSPI3_MISO	GPIO4_IO23	Serial Peripheral Interface B, Master In Slave Out
223	SPI_B_CLK	DISP0_DATA00 / ECSPI3_SCLK	GPIO4_IO21	Serial Peripheral Interface B, Serial Clock
225	SPI_B_CS0#	DISP0_DATA04 / ECSPI3_SS1	GPIO4_IO25	Serial Peripheral Interface B, Chip Select 0
227	SPI_B_CS1#	DISP0_DATA05 / ECSPI3_SS2	GPIO4_IO26	Serial Peripheral Interface B, Chip Select 1
280	SPI_B_CS2#	DISP0_DATA06 / ECSPI3_SS3	GPIO4_IO27	Serial Peripheral Interface B, Chip Select 2

2.4.8 MCI Multimedia Card

The SoM-iMX6M provides two SDIO/MMC interfaces for media cards or external peripheral interfacing. Both interfaces provide support for 4-bit mode. The EM4C Specification has the provision for a single 8-bit SDIO/MMC port however the SoM-iMX6M implements the dual 4-bit version.

Table 15: MMC/SD Card Interface A

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
203	SDIO_A_CD	GPIO04 / SD2_CD_B	GPIO1_IO4	SDIO/MMC A Card Detect
205	SDIO_A_CMD	SD2_CMD	GPIO1_IO11	SDIO/MMC A Command
206	SDIO_A_CLK	SD2_CLK	GPIO1_IO10	SDIO/MMC A Clock
212	SDIO_A_DAT0	SD2_DATA0	GPIO1_IO15	SDIO/MMC A Data 0
209	SDIO_A_DAT1	SD2_DATA1	GPIO1_IO14	SDIO/MMC A Data 1
214	SDIO_A_DAT2	SD2_DATA2	GPIO1_IO13	SDIO/MMC A Data 2
211	SDIO_A_DAT3	SD2_DATA3	GPIO1_IO12	SDIO/MMC A Data 3

Table 16: MMC/SD Card Interface B

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
207	SDIO_B_CD	NAND_CS1_B / SD4_VSELECT	GPIO6_IO14	SDIO/MMC B Card Detect
210	SDIO_B_CMD	SD4_CMD	GPIO7_IO09	SDIO/MMC B Command
208	SDIO_B_CLK	SD4_CLK	GPIO7_IO10	SDIO/MMC B Clock
216	SDIO_B_DAT0	SD4_DATA0	GPIO2_IO08	SDIO/MMC B Data 0
213	SDIO_B_DAT1	SD4_DATA1	GPIO2_IO09	SDIO/MMC B Data 1
218	SDIO_B_DAT2	SD4_DATA2	GPIO2_IO10	SDIO/MMC B Data 2
215	SDIO_B_DAT3	SD4_DATA3	GPIO2_IO11	SDIO/MMC B Data 3

2.4.9 Serial Ports

The SoM-iMX6M provides four serial ports, three with RTS and CTS handshaking and one with full handshaking. All serial ports are TTL level and will require either an RS232 or RS485 driver/receiver for interfacing to external devices. Serial port A is generally used as the SoM debug port however this can be changed with custom software.

Table 17: Serial Port A

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
243	UART_A_TXD	EIM_DATA26 / UART2_TX_DATA	GPIO3_IO26	TTL Level Serial Port A Transmit Data
245	UART_A_RXD	EIM_DATA27 / UART2_RX_DATA	GPIO3_IO27	TTL Level Serial Port A Receive Data
247	UART_A_RTS	EIM_DATA28 / UART2_CTS_B	GPIO3_IO28	TTL Level Serial Port A Request To Send
241	UART_A_CTS	EIM_DATA29 / UART2_RTS_B	GPIO3_IO29	TTL Level Serial Port A Clear To Send

Table 18: Serial Port B

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
236	UART_B_TXD	CSI0_DATA10 / UART1_TX_DATA	GPIO5_IO28	TTL Level Serial Port B Transmit Data
238	UART_B_RXD	CSI0_DATA11 / UART1_RX_DATA	GPIO5_IO29	TTL Level Serial Port B Receive Data
234	UART_B_CTS	EIM_DATA2- / UART1_RTS_B	GPIO3_IO20	TTL Level Serial Port B Clear To Send
240	UART_B_RTS	EIM_DATA19 / UART1_CTS_B	GPIO3_IO19	TTL Level Serial Port B Request To Send
242	UART_B_DCD	EIM_DATA23 / UART1_DCD_B	GPIO3_IO23	TTL Level Serial Port B Data Carrier Detect
244	UART_B_DSR	EIM_DATA25 / UART1_DSR_B	GPIO3_IO25	TTL Level Serial Port B Data Set Ready
246	UART_B_DTR	EIM_DATA24 / UART1_DTR_B	GPIO2_IO24	TTL Level Serial Port B Data Terminal Ready
248	UART_B_RI	EIM_EB3 / UART1_RI_B	GPIO2_IO31	TTL Level Serial Port B Ring Indicator

Table 19: Serial Port C

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
140	UART_C_TXD	CSI0_DATA12 / UART4_TX_DATA	GPIO5_IO30	TTL Level Serial Port C Transmit Data
142	UART_C_RXD	CSI0_DATA13 / UART4_RX_DATA	GPIO5_IO31	TTL Level Serial Port C Receive Data
144	UART_C_RTS	CSI0_DATA17 / UART4_CTS_B	GPIO6_IO03	TTL Level Serial Port C Request To Send
146	UART_C_CTS	CSI0_DATA16 / UART4_RTS_B	GPIO6_IO02	TTL Level Serial Port C Clear To Send

Table 20: Serial Port D

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
150	UART_D_TXD	CSI0_DATA14 / UART5_TX_DATA	GPIO6_IO00	TTL Level Serial Port D Transmit Data
152	UART_D_RXD	CSI0_DATA15 / UART5_RX_DATA	GPIO6_IO01	TTL Level Serial Port D Receive Data
156	UART_D_RTS	CSI0_DATA19 / UART5_CTS_B	GPIO6_IO05	TTL Level Serial Port D Request To Send
158	UART_D_CTS	CSI0_DATA18 / UART5_RTS_B	GPIO6_IO04	TTL Level Serial Port D Clear To Send

2.4.10 I2S

The SoM-iMX6M provides dual I2S audio interfaces for connecting to an audio codec or other peripheral hardware. The I2S audio master clock is derived from a 12.000MHz oscillator on the SoM. The oscillator can be disabled by writing port GPIO6_IO07 low.

Table 21: I2S A

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
187	I2S_A_RXD	DISP0_DATA23 / AUD4_RXD	GPIO5_IO17	Integrated Inter-chip Sound A Serial Receive
189	I2S_A_TXFS	DISP0_DATA22 / AUD4_TXFS	GPIO5_IO16	Integrated Inter-chip Sound A Frame Sync
191	I2S_A_TXD	DISP0_DATA21 / AUD4_TXD	GPIO5_IO15	Integrated Inter-chip Sound A Serial Transmit
193	I2S_A_TXC	DISP0_DATA20 / AUD4_TXC	GPIO5_IO14	Integrated Inter-chip Sound A Serial Clock
195	I2S_A_CLK	N/A	Not Driven by i.MX6	Integrated Inter-chip Sound A Master Clock

Table 22: I2S B

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
186	I2S_B_RXD	DIO_PIN04 / AUD6_RXD	GPIO4_IO20	Integrated Inter-chip Sound B Serial Receive
188	I2S_B_TXFS	DIO_PIN03 / AUD6_TXFS	GPIO4_IO19	Integrated Inter-chip Sound B Frame Sync
190	I2S_B_TXD	DIO_PIN02 / AUD6_TXD	GPIO4_IO18	Integrated Inter-chip Sound B Serial Transmit
192	I2S_B_TXC	DIO_PIN15 / AUD6_TXC	GPIO4_IO17	Integrated Inter-chip Sound B Serial Clock
194	I2S_B_CLK	N/A	Not Driven by i.MX6	Integrated Inter-chip Sound B Master Clock

An SPDIF Output is provided on SOM Pin #196. There is a matching SPDIF Input located in the GPIO section at SOM Pin #258. The SPDIF will require a transceiver be designed onto the carrier.

Table 23: SPDIF

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
196	SPDIF_OUT	EIM_DATA22 /	GPIO3_IO22	SPDIF Output

2.4.11 CAN

The SoM-iMX6M has two CAN interfaces. Both interfaces provide RX and TX lines. A CAN transceiver (ex. SN65HVD232) will need to be provided on the carrier board as well as signal termination.

Table 24: CAN A

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
200	CAN_A_TX	GPIO7 / FLEXCAN1_TX	GPIO1_IO07	Controller Area Network Transmit Data
202	CAN_A_RX	GPIO8 / FLEXCAN1_RX	GPIO1_IO08	Controller Area Network Receive Data

Table 25: CAN B

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
197	CAN_B_TX	KEY_COL4 / FLEXCAN2_TX	GPIO4_IO14	Controller Area Network B Transmit Data
199	CAN_B_RX	KEY_ROW4 / FLEXCAN2_RX	GPIO4_IO15	Controller Area Network B Receive Data

2.4.12 GPIO

This section provides for the SoM-iMX6M's general purpose IO section. All of these pins can be configured to be general-purpose digital ports and are 3.3V compatible. They can also be configured to take advantage of several of the functions of the SoM-iMX6M's internal silicon. There are 22 total GPIO pins four of which are connected to the i.MX6's PWM controller and two connect to the general purpose timer. GPIO15 also serves as an SPDIF input channel.

Table 26: PWM

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
2	GPIO0/PWM0	DISP0_DATA08 / PWM1_OUT	GPIO4_IO29	General Purpose Input/Output PWM Output0
4	GPIO1/PWM1	DISP0_DATA09 / PWM2_OUT	GPIO4_IO30	General Purpose Input/Output PWM Output1
8	GPIO2/PWM2	SD1_DATA1 / PWM3_OUT	GPIO1_IO17	General Purpose Input/Output PWM Output2
10	GPIO3/PWM3	SD1_CMD / PWM4_OUT	GPIO1_IO18	General Purpose Input/Output PWM Output3

Table 27: Timers/Counters

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
14	GPIO4/TC1	SD1_DATA0 / GPT_CAPTURE1	GPIO1_IO16	General Purpose Input/Output Timer Counter 1
16	GPIO5/TC2	SD1_CLK / GPT_CLKIN	GPIO1_IO20	General Purpose Input/Output Timer Counter 2

Table 28: General Purpose IO

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
20	GPIO6	DISP0_DATA11	GPIO5_IO05	General Purpose Input/Output
22	GPIO7	DISP0_DATA12	GPIO5_IO06	General Purpose Input/Output
26	GPIO8	DISP0_DATA13	GPIO5_IO07	General Purpose Input/Output
28	GPIO9	DISP0_DATA14	GPIO5_IO08	General Purpose Input/Output
32	GPIO10	DISP0_DATA16	GPIO5_IO10	General Purpose Input/Output
34	GPIO11	CSI0_PIXCLK	GPIO5_IO18	General Purpose Input/Output
255	GPIO12	CSI0_HSYNC	GPIO5_IO19	General Purpose Input/Output
256	GPIO13	CSI0_DATA_EN	GPIO5_IO20	General Purpose Input/Output
257	GPIO14	CSI0_VSYNC	GPIO5_IO21	General Purpose Input/Output
258	GPIO15	EIM_DATA21 / SPDIF_IN	GPIO3_IO21	General Purpose Input/Output
259	GPIO16	KEY_ROW1	GPIO4_IO09	General Purpose Input/Output
260	GPIO17	DISP0_DATA07 / ECSPI3_RDY	GPIO4_IO28	General Purpose Input/Output
261	GPIO18	SD3_DATA4	GPIO7_IO01	General Purpose Input/Output
262	GPIO19	SD3_DATA5	GPIO7_IO00	General Purpose Input/Output
263	GPIO20	SD3_DATA6	GPIO6_IO18	General Purpose Input/Output
264	GPIO21	NAND_CS3_B	GPIO6_IO16	General Purpose Input/Output

2.4.13 LVDS

The SoM-iMX6M provides a 24-bit LVDS interface for video display. The LVDS interface supports 165 Mpixels/sec and provides I2C communication to the display.

Table 29: LVDS

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
E3_9	LVDS_A0-	LVDS0_DATA0_N	N/A	LVDS Data Pair 0-
E3_10	LVDS_A0+	LVDS0_DATA0_P	N/A	LVDS Data Pair 0+
3	LVDS_A1-	LVDS0_DATA1_N	N/A	LVDS Data Pair 1-
5	LVDS_A1+	LVDS0_DATA1_P	N/A	LVDS Data Pair 1+
9	LVDS_A2-	LVDS0_DATA2_N	N/A	LVDS Data Pair 2-
11	LVDS_A2+	LVDS0_DATA2_P	N/A	LVDS Data Pair 2+
15	LVDS_A3-	LVDS0_DATA3_N	N/A	LVDS Data Pair 3-
17	LVDS_A3+	LVDS0_DATA3_P	N/A	LVDS Data Pair 3+
21	LVDS_CLK-	LVDS0_CLK_N	N/A	LVDS Clock Pair -
23	LVDS_CLK+	LVDS0_CLK_P	N/A	LVDS Clock Pair +
27	LVDS_BL_CTRL	ENET_TX_DATA0	GPIO4_IO29	LVDS Backlight Control
29	LVDS_EN	ENET_MDC	GPIO1_IO31	LVDS Display Enable
31	LVDS_VDD_EN	ENET_TX_DATA1	GPIO1_IO29	LVDS Power Enable
37	LVDS_I2C_SDA	EIM_DATA16	GPIO3_IO16	LVDS I2C Serial Data
39	LVDS_I2C_SCL	EIB_EB2	GPIO2_IO30	LVDS I2C Serial Clock

2.4.14 HDMI

The SoM-iMX6M provides one HDMI Version 1.4 port that is capable of up to 264MHz pixel clock. The HDMI port supports HDMI 1.4a, HDMI CTS 1.4a, DVI 1.0 and HDCP 1.4 and Supports video resolution up to 1080p @ 120Hz.

Table 30: HDMI

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
43	HDMI_CLK+	HDMI_TX_CLK_P	N/A	HDMI Clock Pair +
45	HDMI_CLK-	HDMI_TX_CLK_N	N/A	HDMI Clock Pair -
49	HDMI_D0+	HDMI_TX_DATA0_P	N/A	HDMI Data Pair 0+
51	HDMI_D0-	HDMI_TX_DATA0_N	N/A	HDMI Data Pair 0-
55	HDMI_D1+	HDMI_TX_DATA1_P	N/A	HDMI Data Pair 1+
57	HDMI_D1-	HDMI_TX_DATA1_N	N/A	HDMI Data Pair 1-
61	HDMI_D2+	HDMI_TX_DATA2_P	N/A	HDMI Data Pair 2+
63	HDMI_D2-	HDMI_TX_DATA2_N	N/A	HDMI Data Pair 2-
67	HDMI_HPD	HDMI_TX_HPD	N/A	HDMI Hot Plug Detect
69	HDMI_CAD	NAND_WP_B	GPIO6_IO09	HDMI Cable Detect
71	HDMI_CEC	EIM_ADDR25 / HDMI_TX_CEC_LINE	GPIO5_IO02	HDMI CEC
73	HDMI_I2C_SCL	KEY_COL3 / HDMI_TX_DDC_SCL	GPIO4_IO12	HDMI DDC/I2C Serial
75	HDMI_I2C_SDA	KEY_ROW3 / HDMI_TX_DDC_SDA	GPIO4_IO13	HDMI DDC/I2C Serial

2.4.15 CSI

The SoM-iMX6M has CSI (camera serial interface) that supports up to 1Gbps per data lane. There are four total lanes included on the SoM.

Table 31: CSI

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
160	CSI_CLK-	CSI_CLK0_N	N/A	Camera Serial Interface Clock Pair -
162	CSI_CLK+	CSI_CLK0_P	N/A	Camera Serial Interface Clock Pair +
164	CSI_DATA0-	CSI_DATA0_N	N/A	Camera Serial Interface Data Pair 0-
168	CSI_DATA0+	CSI_DATA0_P	N/A	Camera Serial Interface Data Pair 0+
170	CSI_DATA1-	CSI_DATA1_N	N/A	Camera Serial Interface Data Pair 1-
172	CSI_DATA1+	CSI_DATA1_P	N/A	Camera Serial Interface Data Pair 1+
174	CSI_DATA2-	CSI_DATA2_N	N/A	Camera Serial Interface Data Pair 2-
176	CSI_DATA2+	CSI_DATA2_P	N/A	Camera Serial Interface Data Pair 2+
178	CSI_DATA3-	CSI_DATA3_N	N/A	Camera Serial Interface Data Pair 3-
180	CSI_DATA3+	CSI_DATA3_P	N/A	Camera Serial Interface Data Pair 3+

2.4.16 DSI

The SoM-iMX6M includes a DSI (display serial interface) with two lanes that support up to 1GHz each. The DSI interface supports the MIPI DSI standard as well as DSI Version 1.01, DPI Version 2.0, DBI Version 2.0 and DCS Version 1.02.

Table 32: DSI

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
267	DSI_CLK+	DSI_CLK0_P	N/A	Display Serial Interface Clock Pair +
269	DSI_CLK-	DSI_CLK0_N	N/A	Display Serial Interface Clock Pair -
268	DSI_D0+	DSI_DATA0_P	N/A	Display Serial Interface Data Pair 0+
270	DSI_D0-	DSI_DATA0_N	N/A	Display Serial Interface Data Pair 0-
271	DSI_D1+	DSI_DATA1_P	N/A	Display Serial Interface Data Pair 1+
273	DSI_D1-	DSI_DATA1_N	N/A	Display Serial Interface Data Pair 1-

2.4.17 PCIe

The SoM-iMX6M includes one PCIe interface. The EM4C SoM Specification includes two lanes however the i.MX6 processor only provides one lane. The interface supports PCIe v2.0. PCIe B is not implemented on the SoM-iMX6M and all pins are no connect.

Table 33: PCIe A

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
85	PCIE_A_CLK+	CLK1_P	N/A	PCIe A Clock Pair +
87	PCIE_A_CLK-	CLK1_N	N/A	PCIe A Clock Pair -
91	PCIE_A_TX+	PCIE_TX_P	N/A	PCIe A Transmit Data +
93	PCIE_A_TX-	PCIE_TX_N	N/A	PCIe A Transmit Data -
97	PCIE_A_RX+	PCIE_RX_P	N/A	PCIe A Receive Data +
99	PCIE_A_RX-	PCIE_RX_N	N/A	PCIe A Receive Data -
113	PCIE_A_CLK_OE	NAND_DATA00	GPIO2_IO00	PCIe A Clock Output Enable

Table 34: PCIe B

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
79	PCIE_B_CLK+	N/C	N/C	PCIe B Clock Pair CLK+
81	PCIE_B_CLK-	N/C	N/C	PCIe B Clock Pair CLK-
103	PCIE_B_TX+	N/C	N/C	PCIe B Transmit Data +
105	PCIE_B_TX-	N/C	N/C	PCIe B Transmit Data -
109	PCIE_B_RX+	N/C	N/C	PCIe B Receive Data +
111	PCIE_B_RX-	N/C	N/C	PCIe B Receive Data -
115	PCIE_B_CLK_OE	N/C	N/C	PCIe B Clock Output Enable

Table 35: PCIe Control

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
119	PCIE_RST#	NAND_DATA07	GPIO2_IO07	PCIe Reset (active low)
107	PCIE_PRES#	NAND_DATA01	GPIO2_IO01	PCIe Presence (active low)
117	PCIE_WAKE#	NAND_DATA02	GPIO2_IO02	PCIe Wake

2.4.18 SATA

The SoM-iMX6M provides a SATA II interface that supports 3.0Gbps.

Table 36: SATA

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
123	SATA_RX+	SATA_PHY_RX_P	N/A	Serial ATA Receive Data Pair +
125	SATA_RX-	SATA_PHY_RX_N	N/A	Serial ATA Receive Data Pair -
135	SATA_TX+	SATA_PHY_TX_P	N/A	Serial ATA Transmit Data Pair +
137	SATA_TX-	SATA_PHY_TX_N	N/A	Serial ATA Transmit Data Pair -
133	SATA_ACT#	NAND_READY	GPIO6_IO10	Serial ATA Activity (active low)

2.4.19 Battery Control

The battery control section for the SoM-iMX6M is for controlling external battery charging circuitry for a SoM based tablet or similar hardware.

Table 37: Battery Control

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
86	PMIC_BATLOW#	NAND_DATA03	GPIO2_IO03	Battery Low Indicator (active low)
90	PMIC_I2C_PM_DAT	EIM_DATA18 / I2C3_SDA	GPIO3_IO18	PMIC I2C Serial Data
92	PMIC_I2C_PM_CLK	EIM_DATA17 / I2C3_SCL	GPIO3_IO17	PMIC I2C Serial Clock
96	PMIC_CHARGE#	NAND_DATA04	GPIO2_IO04	Battery Full Indicator (active low)
98	PMIC_CHARGE_DET#	NAND_DATA05	GPIO2_IO05	Battery Charge Indicator (active low)
102	PMIC_TEST#	NAND_DATA06	GPIO2_IO06	
104	PMIC_SLEEP#	EIM_CS0	GPIO2_IO23	

2.4.20 Analog to Digital Converter

The SoM-iMX6M has an onboard four channel 12-bit analog to digital converter. The SoM uses a Microchip MCP3204 A/D converter. The A/D converter is interfaced through ECSPI1 bus and is connected to ECSPI1_SS0 (GPIO5_IO25). The A/D converter is capable of 50Ksps with 2.7V supply and 100Ksps with 5V supply. The MCP3204 is powered by 3.3V so a sample rate of over 50Ksps is guaranteed. An external ADC voltage reference must be supplied to the SoM through SoM Pin# 35. A maximum of 3.3V for the ADC voltage reference may be used.

Table 38: ADC

SODIMM Pin#	SoM Pin Name	MCP3204 Pin Name(s)	Port Line	Description
78	ADC_1	CH0	N/A	Analog to Digital Converter Channel 1
80	ADC_2	CH1	N/A	Analog to Digital Converter Channel 3
82	ADC_3	CH2	N/A	Analog to Digital Converter Channel 4
33	ADC_4	CH3	N/A	Analog to Digital Converter Channel 5
35	ADC_VREF	VREF	N/A	External ADC Reference Voltage, 3.3V Max

2.4.21 Touch Screen Interface

A resistive touch screen interface is provided on the SoM-iMX6M by use of a TSC2004 touch screen controller. The TSC2004 is connected to the i.MX6 processor through the I2C3 interface. The I2C data pin of the TSC2004 is connected to the i.MX6 processor through I2C3_SDA (GPIO3_IO18) and the I2C clock pin of the TSC2004 is connected to the i.MX6 processor through I2C3_SCL (GPIO3_IO17). The default address for the touch screen controller is 0x90. The address of the TSC2004 can be changed through alternate populations of pull up resistors R83 and R84 which are connected to address lines 1 and 0 respectively and pull down resistors R87 and R88 which are connected to address lines 1 and 0 respectively. By default, both address lines are pulled low. The touch controller interrupt is connected to the i.MX6 processor through port pin GPIO1_IO27.

Table 39: Touch Screen Interface

SODIMM Pin#	SoM Pin Name	TSC2005 Pin Name(s)	Port Line	Description
36	TOUCH_X+	X+	N/A	Resistive Touch X+ Sense
38	TOUCH_X-	X-	N/A	Resistive Touch X- Sense
40	TOUCH_Y+	Y+	N/A	Resistive Touch Y+ Sense
44	TOUCH_Y-	Y-	N/A	Resistive Touch Y- Sense

2.5 Power Connections

The SoM-iMX6M can be powered from a single 5V supply. The VCC_RTC pin is for connecting a battery for the real time clock and requires a 3.7V lithium battery.

Table 40: Power Connections

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
E1_1, E2_1	5V_VSB	5V_VSB	5 Volt Standby Supply
281	VCC_RTC	VCC_RTC	Real Time Clock Battery Backup
E1_2, E2_2, E1_3, E2_3, E1_4, E2_4, E1_5, E2_5, E1_6, E2_6, E1_7, E2_7, E1_8, E2_8, E1_9, E2_9, E1_10, E2_10	5V_VCC	5V_VCC	5 Volt Power Supply
266, 265, 250, 249, 239, 232, 229, 220, 217, 204, 201, 198, 185, 184, 177, 166, 154, 153, 148, 171, 147, 124, 121, 101, 100, 95, 94, 89, 88, 83, 77, 66, 65, 60, 59, 54, 53, 48, 47, 42, 41, 30, 25, 24, 19, 18, 13, 12, 7, 6, 1, E4_10, E3_8, E4_7, E4_4, E3_4, E4_1, E3_1	GND	GND	Ground

2.6 Boot Options

The SoM-iMX6M provides four lines for boot selection. BOOT_0 and BOOT_1 are connected directly to the i.MX6 processor. MS1 and MS2 are connected to internal logic to allow for additional boot modes.

Table 41: Boot Modes

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
74	BOOT_0	BOOT_MODE0	GPIO3_IO06	Processor Boot Options Select 0
76	BOOT_1	BOOT_MODE1	N/A	Processor Boot Options Select 1
276	MS1	BOOT_MODE2	GPIO3_IO05	Additional Boot Options Select 2
278	MS2	BOOT_MODE3	N/A	Additional Boot Options Select 3

The SoM-iMX6M can be configured to boot from one of four different methods by using the four boot pins provided through the SoM card edge. The USB Serial Downloader provides a method for initial programming of the SoM, through the USB OTG port, using the Manufacturing Tool available from Freescale. The SATA boot option will attempt to boot from an externally connected SATA drive. The Onboard serial NOR flash boot option will attempt to boot from the serial flash on ECSPI3 using chip select 0. This is the same ECSPI interface that is connected to the card edge SPI B. The SD4 boot option will attempt to boot from media present on SDIO port 4 that is connected to the card edge through SDIO B. The last boot option will attempt to boot from SDIO port 3 that is connected to the onboard eMMC. If the selected boot device does not contain bootable media then the SoM-iMX6M will fall back to the USB Serial Downloader. For more boot options, the internal fuses can be blown to select a wider range of boot options. These fuses are OTP and once they are blown they cannot be reprogrammed.

Table 42: Boot Options

MS_2	MS_1	BOOT_1	BOOT_0	Boot Media
X	X	0	X	USB Serial Downloader
0	1	1	0	SATA
1	1	1	0	Onboard Serial NOR Flash ECSPI3 Using Chip Select 0
X	0	1	1	SD4 / SDIO B
X	1	1	1	SD3 / Onboard eMMC

2.7 Serial NOR Flash

The SoM-iMX6M has a 16MB serial NOR flash that can be used to boot the SoM. The Serial NOR Flash is connected to ECSPI3 and uses pin DISP0_DATA03/ECSPI3_SS0 to enable it. The SPI interface is also routed to the card edge for Serial Peripheral Interface B. The Serial NOR Flash also has a Write Protect Provision. To Write Protect the Serial NOR Flash pull SoM pin# 279 low. This pin is pulled up by a 10K ohm resistor on the module so if write protect is not desired the SoM pin can simply be left floating.

If this feature is required it would be implemented on the carrier as a jumper or an I/O line.

2.8 eMMC

The SoM-iMX6M has up to an 8GB eMMC onboard that can be used to boot from and also the OS may reside on this media. The eMMC is connected to the SD3 port of the i.MX6 processor. See the Boot Options section for information on booting the SoM-iMX6M from the onboard eMMC.

2.9 Module Status LED

A green status LED (LD1) is active-high and is controlled by port line GPIO1_IO26.

3 Design Considerations

One of the goals of the SoM-iMX6M is to provide a modular, flexible and inexpensive solution capable of delivering high-end microcontroller performance.

3.1 Power

The SoM-iMX6M requires a voltage of 5.0V at 2500mA. For a bare-bones population, users can get away with using only 5.0V, and simply provide this to all the voltage inputs listed in Power Connections section. This however, will not provide battery backup for the RTC.

3.1.1 Battery Backup

The SoM-iMX6M real-time clock (RTC) requires a backup voltage to maintain its data. This backup voltage comes from SoM Pin# 281, VCC_RTC, and should be connected to 3.3 volts.

The RTC will draw approximately 41uA when the processor is not powered by the 5.0V supply. When the module is powered no current is drawn from the backup battery supply. If the RTC is not needed, this can be tied to 3.3V.

3.1.2 Analog Reference

The reference voltage for the analog to digital converter must be supplied on the carrier if the ADC is to be used. The ADC reference voltage should be supplied to SoM pin #35 and can range in value from 0 to 3.3v. For best results this signal should be properly filtered using a ferrite bead and 0.1uF capacitor placed as close as possible to the SoM socket pin.

4 Software

The SoM-iMX6M offers a wide variety of software support from both open source and proprietary sources. The hardware core utilizes the Freescale/NXP/Qualcomm i.MX6 microcontroller, which is supported by Linux.

For more information on Linux Software Support, please visit the EMAC Wiki Software Section at:

http://wiki.emacinc.com/wiki/Product_wiki

4.1 Das U-Boot

EMAC utilizes Das U-Boot for its ARM based products. U-Boot is an open source/cross-architecture platform independent bootloader. It supports reading and writing to the flash, auto-booting, environmental variables, and TFTP. Das U-boot can be used to upload and run and/or reflash the OS or to run stand-alone programs without an OS. Products are shipped with a valid MAC address installed in flash in the protected U-boot environmental variable “ethaddr”. At boot time U-Boot automatically stores this address in a register within the MAC, which effectively provides it to any OS loaded after that point.

4.2 Embedded Linux

EMAC Open Embedded Linux (EMAC OE Linux) is an open source Linux distribution for use in embedded systems. The EMAC OE Linux Build is based on the Open Embedded (www.openembedded.org) and Yocto (www.yoctoproject.org) Linux build systems. Open Embedded is a superior Linux distribution for embedded systems. Custom Linux builds are also available on request.

The distribution contains everything a user could expect from a standard Linux kernel: powerful networking features, advanced file system support, security, debugging utilities, and countless other features.

The basic root file system includes:

- Busybox
- Hotplugging support
- APM utilities for power management
- Openssh SSH server
- lighttpd HTTP server
- JJFS2 or EXT4 file system with utilities

4.2.1 Linux with Xenomai Real Time Extensions

Xenomai provides real time extensions to the kernel and can be used to schedule tasks with hard deadlines and µs latencies. The Xenomai build is an additional module that can be added to the standard Linux kernel and is available for a one-time inexpensive support/installation fee.

http://www.xenomai.org/

4.2.2 Linux Packages

EMAC provides support for many Linux Packages such as: PHP, SQLite, Perl, SNMP, DHCP Server, etc. As with the Xenomai Package, other Packages can be added to the standard Linux file system and are available for a one-time inexpensive support/installation fee.

4.2.3 Linux Patches

In addition to standard Embedded Linux support, EMAC has released a number of patches and device drivers from the open source community and from internal EMAC engineering into its standard distribution. Along with kernel patches, EMAC provides the binaries for the kernel and root file system.

4.3 Qt Creator

Qt Creator is a cross-platform IDE (Integrated Development Environment) tailored to the needs of Qt developers but works well for Headless applications as well. EMAC provides sample code as projects that can be imported into Qt Creator. Qt Creator supports remote deployment and source debugging.

http://wiki.qt.io/Main

4.4 ARM EABI Cross Compiler

The popular open source gcc compiler has a stable build for the ARM family. EMAC uses the 4.9.1 version of the ARM EABI compiler. The Embedded Linux kernel and EMAC Qt Creator projects use this compiler for building ARM stand alone, and OS specific binaries. The EMAC Qt Creator provides source level debugging over Ethernet or serial using gdbserver. The Linux binaries for the ARM EABI cross compiler are available online along with the SDK. See the EMAC wiki for further information.

5 Dimensions