SoM-3517M

User Manual

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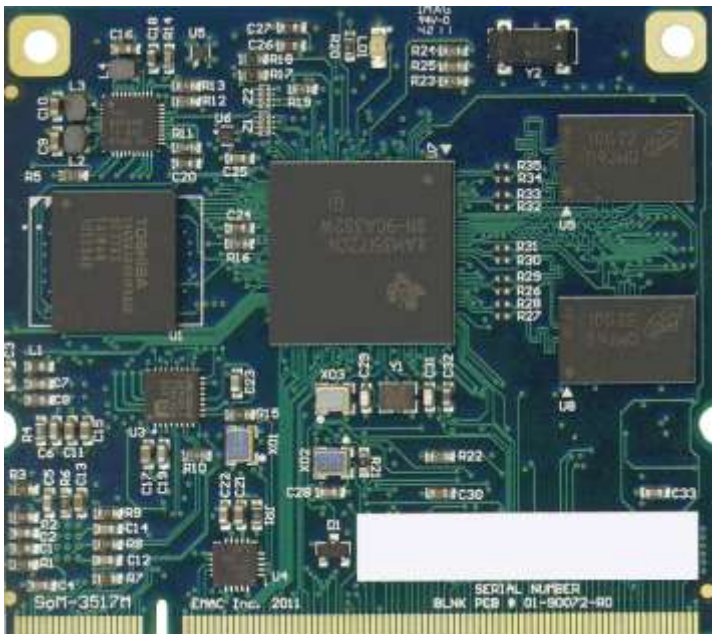
2. Introduction



This document describes the EMAC SoM-3517M System on Module. The SoM-3517M is designed to be compatible with EMAC's 200-pin SODIMM form factor. This module is built around the Texas Instruments AM3517 ARM Cortex A8 based microprocessor, which provides several of its key features.

The SoM-3517M has an on-board Ethernet PHY, 5 serial ports, 4-wire touchscreen controller, RTC, eMMC, USB PHY/Switch, NAND flash, and DDR2 SDRAM.

In addition to these standard SoM features, the SoM-3517M also features a fast 32-bit core, hardware graphics accelerators, open source software support, and a wide range of controller IO pins.

2.1. Features

- **Small, 200 pin SODIMM form factor (2.66" x 2.375")**
- **Texas Instruments AM3517 600Mhz ARM Cortex A8 based Processor**
- **10/100BaseT Ethernet with on-board PHY**
- **4 Serial ports with handshake**
- **1 USB 2.0 (High Speed) Host port with 2 port USB switch**
- **1 USB 2.0 (High Speed) OTG Host/Device port**
- **Up to 512 MB of SDRAM**
- **Up to 512 MB of NAND Flash**
- **Up 2GB eMMC Flash**
- **1 SD/MMC Flash Card Interfaces**
- **Battery backed Real Time Clock**
- **2 SPI and 1 I2C port**

- **2 I2S Audio ports**
- **1 CAN port**
- **Timer, Counters, and Pulse Width Modulation (PWM) ports**
- **4-wire Touchscreen Interface with 1 Channel 12-bit Analog-to-Digital converter**
- **Timer/Counters and Pulse Width Modulation (PWM) ports**
- **Graphic LCD Interface with 2D/3D acceleration up to 1280 x 860 Resolution**
- **True Random Number Generator**
- **JTAG for debug, including real-time trace**
- **FREE Eclipse IDE with GCC & GDB development tools**
- **WinCE 6.0 BSP**

3. Hardware

3.1. Specifications

- **CPU:** Texas Instruments AM3517 processor running at 600 MHz.
- **Flash:** Up to 2GB of eMMC and 512 MB NAND Flash.
- **RAM:** Up to 512 MB, 133 MHz DDR2 (256MB standard).
- **Video:** 2D/3D Accelerated 24 Bit LCD Video Interface with up to 1280 x 860 resolution.
- **Touchscreen:** 12-Bit, 4-wire analog resistive touchscreen interface.
- **Flash Disk:** Up to 4 GB of eMMC (2 GB standard).
- **System Reset:** Processor Internal Reset Management with External Reset Button provision.
- **RTC:** Battery backed Real Time Clock/Calendar using 32-bit free running counter.
- **Timers/Counters:** 11 Internal General Purpose Timers, 4 available externally for Timer Counters/PWM.
- **Watchdog Timer:** 2 Internal Watchdog Timers.
- **Digital I/O:** Many general purpose I/Os multiplexed with peripheral interfaces.
- **Analog I/O:** 1 channel, 12-bit A/D.
- **Power:** Power Management Controller allows selective shutdown capability on processor I/O functionality and running from a slow clock.
- **JTAG**: JTAG for debug, including real-time trace.
- **Video Input:** CCD video input interface.

Serial Interfaces

- **UARTS:** 4 serial TTL level serial ports, 3 with RTS/CTS handshaking, 1 with full handshaking. (each UART requires external RS level shifting)
- **SPI:** 2 High-Speed SPI ports with Chip Selects.
- **I2C:** 2 multi-mode I2C port.
- **Audio:** 2 I2S Synchronous Serial Controller with analog interface support
- **USB:**
  - 1 USB 2.0 High Speed Host port with 2 port USB switch (2 Host Ports one of which is USB 1.1 compatible)
  - 1 USB 2.0 High Speed Host or Device (USB OTG) software configurable
- **CAN:** Processor Internal, High End CAN Controller (HECC).

Ethernet Interface

- **MAC:** Ethernet on chip MAC
- **PHY:** Micrel KSZ8041 with software PHY shutdown control
- **Interface:** IEEE 802.3u 10/100 BaseT Fast Ethernet (requires external magnetics and jack)

Bus Interface

- ARM EBI accessible through SODIMM provides 11 address lines, 16 data bus lines, and control lines.

Mechanical and Environmental

- **Dimensions:** SODIMM form factor with the length dimension extended (2.66" x 2.375")
- **SODIMM TYPE:** 200 Pin DDR1 (not compatible with DDR2)
- **Power Supply Voltage:** +3.3 Volts DC +/- 5%
- **Power Requirements (Typical):** (128MB SoM-3517)
  - 3.3 Volts @ 470mA.
  - Max current draw during boot process: 482mA.
  - Constant busy loop: 485mA.
  - Constant busy loop with Ethernet PHY disabled: TBD
  - Idle system: 465mA.
  - Idle system with Ethernet PHY disabled: TBD
  - APM sleep mode using slow clock with Ethernet PHY disabled: TBD
  - APM sleep mode using slow clock with Ethernet PHY enabled: TBD
- **Operating Temperature:**
  - -40 ~ 85° C (-40 ~ 185 ° F), fanless operation for SOM-3517M-339R and SOM-3517M-341R.
  - 0 ~ 70° C (32 ~ 158 ° F), fanless operation for SOM-3517M-130R, SOM-3517M-131R and SOM-3517M-141R
- **Operating Humidity:** 0% ~ 90% relative humidity, non-condensing

3.2. Real Time Clock

The external RTC is based on the I2C PCA8565TS chip from NXP. The chip is connected to the AM3517 processor via I2C channel 1.

3.3. Watchdog Timer

A 32 kHz clock drives the AM3517 internal watchdog timers. Each timer contains a free-running, 32bit up counter. Each counter has an 8 bit, programmable clock divider. Timeout events can trigger reset and interrupt events.

3.4. Status LED

The SoM-3517M provides a user programmable, green, status LED. To control this LED, use GPIO port line GPIO_25. Setting the port line high will turn on the LED.

3.5. External Connections

The SoM-3517M connects to a carrier board containing its connectors, power supply and any expansion IO, through a standard gold-plated SODIMM 200-pin connection shown below.

The SoM model will fit in any standard 200-pin SODIMM socket. These connections are designed to be compatible with all EMAC 200-pin SoM products, see EMAC SoM 200-pin SODIMM Pinout Specification to compare other 200-pin SoMs pinouts to the SoM-9G45/9M10M's pinout.

The use of the DDR SODIMM form-factor for EMAC's SoMs is a sound choice that has been proven rugged and reliable in the laptop and embedded SBC markets.

The remainder of this section describes the pinout as it applies specifically to the SoM-9G45/9M10M processor.

3.5.1. System Control & External Bus

The SoM-3517M provides a flexible external bus for connecting peripherals. The CPLD of the SoM-200ES Carrier board connects through a subset of these connections. The external bus interface section of the SoM-3517 is also used to bring out some of the CCD video input lines from the processor.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
145	GP_CSA	GPMC_NCS1	GPIO_52	General Purpose Chip Select CS1
146	GP_CSB	GPMC_NCS2	GPIO_53	General Purpose Chip Select CS2
147	GP_CSC	GPMC_NCS3	GPIO_54	General Purpose Chip Select CS3
148	GP_CSD/Shutdown	GPMC_NCS4	GPIO_55	General Purpose Chip Select CS4
149	~WR	GPMC_NWE		Write Signal
150	~RD/TIP	GPMC_NOE		Read Signal
151	~RST_IN	NRST_IN		Processor Reset
152	~RST_OUT	NRST_OUT		Processor Reset
153	~WAIT	GPMC_WAIT3	GPIO_65	Shutdown Control
154	~FLASH WP	NFLASH_WP	GPIO_62	Flash Write Protect
54	WAKEUP	SYS_NIRQ	GPIO_0	Processor Wakeup Input
157	BOOT_OPTION0	SYS_BOOT[5:0]		Boot0 Option Select
158	BOOT_OPTION1	SYS_BOOT[5:0]		Boot1 Option Select
175	A0	GPMC_NADV_ALE		Address Control Line
176 – 185	A1 – A10	GPMC_A1 – GPMC_A10	GPIO_34-43	Address Bus
159 – 166	D0 – D7	GPMC_D0 – GPMC_D7		Data Bus
167 – 174	D8 – D15	GPMC_D8 – GPMC_D15	GPIO_44-51	Data Bus
186	A11	CCDC_PCLK	GPIO_94	CCDC PCLK Line
187	A12	CCDC_FIELD	GPIO_95	CCDC Field Line
188	A13	CCDC_WEN	GPIO_98	CCDC WEN Line
189-196	A14-A21	CCDC_DATA0 – CCDC_DATA7	GPIO_99 - GPIO_106	CCDC Data Lines

3.5.2. USB

The SoM 200-pin specification provides for 2 USB hosts and 1 USB device or OTG port. The AM3517 provides a USB 2.0 OTG port and a USB 2.0 host port interface. The Host port interface is connected to a USB PHY (USB3320). The USB 2.0 Host PHY is then connected on-board to a USB 2.0 switch (USB2512) to allow for use of both Host ports as per the specification.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
5	Host_A+	HDPA1		Host USB Switch Port0 + pin
7	Host_A-	HDMA1		Host USB Switch Port0 – pin
6	Host_B+	HDPA2		Host USB Switch Port1 + pin
8	Host_B-	HDMA2		Host USB Switch Port1 – pin
9	Host/Device/OTG_C-	USB0_DM		OTG USB 2.0 Port0 - pin
11	Host/Device/OTG_C+	USB0_DP		OTG USB 2.0 Port0 + pin
10	USB_OTG_VBUS	USB0_VBUS		OTG VBUS
40	USB_OTG_ID	USB0_ID		OTG ID

3.5.3. JTAG

The SoM specifications allow for access to the JTAG lines for the AM3517 processor. These connections will allow the Flash to be programmed in circuit via a program running from the processor and also the capability to debug software.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
139	JTAG_TCK	JTAG_TCK	JTAG clock
140	JTAG_TDI	JTAG_TDI	JTAG serial in
141	JTAG_TDO	JTAG_TDO	JTAG serial out
142	JTAG_TMS	JTAG_TMS	JTAG operation mode
143	JTAG_TRST	JTAG_NTRST	Test Reset Signal
144	JTAG_RTCK	JTAG_RTCK	Dynamic clock sync

3.5.4. Ethernet

The SoM-3517M provides a Micrel KSZ8041 Ethernet 10/100 PHY IC on board. Carrier designers need only to run these lines through the appropriate magnetics layer to have a functional Ethernet connection. Remember, the RX and TX lines are differential pairs and need to be routed as such.

The LED/configuration pins' state at reset determines the Ethernet's configuration (10-baseT, 100-baseT, autoconfig) and the function of the LED's. The SoM-200ES pulls them all high, which configures the chip for network autoconfig; with LED2 functioning as an active low link and LED3 functioning as active low Activity status (Refer to Carrier schematics).

Note: The KSZ8041 only provides two LEDs. Labeling of the LEDs (1-3) was due to a legacy PHY used on other SoMs.

SODIMM Pin#	SoM Pin Name	PHY Pin Name	Description
12	GIG D-	NC	GIG Ethernet D- pin
14	GIG D+	NC	GIG Ethernet D+ pin
13	GIG C- /Host/Device/OTG_C-	NC	GIG Ethernet C- pin
15	GIG C+	NC	GIG Ethernet C+ pin
16	Ethernet_Rx-/GIG B-	Etherent_Rx-	Low differential Ethernet receive line
18	Ethernet_Rx+/GIG B+	Ethernet_Rx+	High differential Ethernet receive line
17	Etherent_Tx-/GIG A-	Etherent_Tx-	Low differential Ethernet transmit line
19	Ethernet_Tx+/GIG A+	Ethernet_Tx+	High differential Ethernet transmit line
38	LED_LINK/CFG_2	ETH_LED1	Ethernet Link LED/Configuration pin
39	LED_ACT/CFG_3	ETH_LED2	Ethernet Activity LED/Configuration pin

3.5.5. I^2C

The SoM-200 specification calls for a two-wire I^2C port. The SoM-9G45/9M10M does not have a native hardware I^2C port but does provide two general purpose lines that can be used in this capacity when "bit-banged". Both Linux and CE provide this functionality.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
29	I2CCLK	I2C2_SCL	GPIO_168	Clock pin
30	I2CDATA	I2C2_SDA	GPIO_183	Data pin

3.5.6. SPI

The AM3517 processor provides 4 SPI channels for communicating with peripheral devices. Two of the SPI channels have been provided via the SoM edge connector. The first table below lists the lines for the dedicated SPI channel.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
22	SPI_MI	MCSPI1_SOMI	GPIO_173	SPI1 serial data in
23	SPI_MO	MCSPI1_SIMO	GPIO_172	SPI1 serial data out
24	SPI_SCK	MCSPI1_CLK	GPIO_171	SPI1 serial clock out
25	SPI_CS0	MCSPI1_CS0	GPIO_174	SPI1 slave select line 0
26	SPI_CS1	MCSPI1_CS1	GPIO_175	SPI1 slave select line 1
27	SPI_CS2	MCSPI1_CS2	GPIO_176	SPI1 slave select line 2
28	SPI_CS3/SPI _Frame	MCSPI1_CS3	GPIO_177	SPI1 slave select line 3

The Table below documents the SPI channel 2, which shares pins in the GPIO pin section.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
125	GPIO11	MCSPI2_CLK	GPIO_178	SPI2 serial data in
126	GPIO12	MCSPI2_SIMO	GPIO_179	SPI2 serial data out
127	GPIO13	MCSPI2_SOMI	GPIO_180	SPI2 serial clock out
128	GPIO14	MCSPI2_CS0	GPIO_181	SPI2 slave select line 0
134	GPIO15	MCSPI2_CS1	GPIO_182	SPI2 slave select line 1

3.5.7. CAN

The AM3517 provides a High-End CAN Controller (HECC) internally. The CAN interface lines are directed to the dedicated CAN pads on the SoM connector as shown in the table below.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Pin Description
93	CANTX	HECC1_TXD	GPIO_130	CAN Transmit
94	CANRX	HECC1_RXD	GPIO_131	CAN Receive

3.5.8. IRQs

The SoM-200 specification allocates three pins as IRQs. The AM3517 processor can use virtually any GPIO pin to trigger an interrupt. EMAC used the following GPIO lines for general purpose IRQs:

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	SoM Description
129	IRQA	JART1_CTS/MCBSP1_CLKS	GPIO_160	Interrupt A
130	IRQB	MCBSPI4_CS0/MCBSP1_FSX	GPIO_161	Interrupt B
131	IRQC	MCBSP1_CLKX	GPIO_162	Interrupt C

3.5.9. Oscillators

The SoM-200 specification provides for two general-purpose oscillators. These frequencies can vary slightly between modules depending on how they are generated and some modules may not provide 50% duty cycles. The AM3517 uses its internal, general-purpose timers to generate these frequencies. The frequencies are programmable via software. These outputs may be used as may be used as PWM or counters if required in the target application.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	SoM Description
132	OSC0 (high)	GPT10_PWM_EVT	GPIO_145	~ 8 MHz
133	OSC1 (low)	GPT09_PWM_EVT	GPIO_144	~ 200 KHz

3.5.10. SD/Multimedia Card

The AM3517 processor provides multiple 4-bit MMC/SD card interface using the MCI lines. The SoM-200ES & 210ES Carrier boards can use a parallel MMC/SD interface if available.

The SoM-200 specification provides for three optional SD/MMC control lines. Since these lines are optional and will not always be used they are not part of the SD/MMC group, but, instead, are part of the GPIO group. SoM pin#s 122, 123, and 124 can be used as SD_LED, SD_Power, and SD_protect respectively.

MMC2 is allocated to the SoM Pin Specification in the SD/MMC section as the default SD port. This port should be used to maintain compatibility with past and future modules. As mentioned about the AM3517 processor provides multiple SD ports. The MMC1 port is allocated to the on-module eMMC chip.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
31	SDCLK	MMC2_CLK	GPIO_130/GPIO_139	MCI Clock
32	CMD	MMC2_CMD	GPIO_131	MCIA Command
33	DAT0	MMC2_DAT0	GPIO_132	MCIA D0
34	DAT1	MMC2_DAT1	GPIO_133	MCIA D1
35	DAT2	MMC2_DAT2	GPIO_134	MCIA D2
36	DAT3	MMC2_DAT3	GPIO_135	MCIA D3
37	Card_Detect	MMC1_DAT5	GPIO_127	Card Detect

3.5.11. I2S Audio

The AM3517 provides multiple I2S audio ports that are accommodated within the SoM specification. Note that there is no CODEC on the SoM and therefore must be provided on the Carrier. In addition the CODEC will require either SPI or I2C for control.

The Master clock is derived by an On-Module 24.576 MHz oscillator divided by two to produce the 12.288 MHz Master clock. This oscillator is off by default and must be turned on via setting GPIO port line PD4 High. To reduce power the oscillator should be turned off when not required.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
86	AudioA_SCLK	MCBSP2_CLKX	GPIO_117	I2S Serial Clock
87	AudioA_LRCLK/Frame	MCBSP2_FSX	GPIO_116	I2S Left / Right Clock
88	AudioA_MCLK	12.288 MHz Clock		I2S Master Clock
89	AudioA_DIN	MCBSP2_DR	GPIO_118	I2S Data Input
90	AudioA_DOUT	MCBSP2_DX	GPIO_119	I2S Data Output

MCBSP2 is allocated to the SoM Pin Specification in the Audio section as the default I2S port. This port should be used to maintain compatibility with past and future modules. As mentioned, the AM3517 processor provides multiple I2S ports; however, other processors may only offer one. The table below documents the 2nd I2S port that shares pins in the GPIO pin section. The master clock of the second interface is not dedicated and should be driven by a stand-alone oscillator or SoM output clock.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
121	GPIO7	MCBSP4_CLKX	GPIO_152	I2S Serial Clock
124	GPIO10	MCBSP4_FSX	GPIO_155	I2S Left / Right Clock
123	GPIO9	MCBSP4_DX	GPIO_154	I2S Data Output
122	GPIO8	MCBSP4_DR	GPIO_153	I2S Data Input

3.5.12. Serial Ports

The SoM-200 pin specification has the provision for 4 serial ports. The AM3517 processor does not provide full modem handshaking for COMA as called for in the SoM-200 pin specification; therefore EMAC has utilized processor GPIO lines for this function. The RTS lines for each port can be used to achieve automatic RS485 directional control.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	SoM Description
95	COMA_TXD	UART1_TX	GPIO_148	COMA transmit/GPIO
96	COMA_RXD	UART1_RX	GPIO_151	COMA receive/GPIO
97	COMA_CTS	UART1_CTS	GPIO_150	COMA CTS/GPIO
98	COMA_RTS	UART1_RTS	GPIO_149	COMA RTS/GPIO
99	COMA_DTR	MMC1_DAT4/DTR	GPIO_126	COMA DTR/GPIO
100	COMA_DSR	MMC1_DAT6/DSR	GPIO_128	COMA DSR /GPIO
101	COMA_RI	MMC1_DAT7/RI	GPIO_129	COMA RING/GPIO
102	COMB_TXD	UART3_TX_IRTX	GPIO_166	COMB transmit/GPIO
103	COMB_RXD	UART3_RX_IRRX	GPIO_165	COMB receive/GPIO
104	COMB_CTS	UART3_CTS_RCTX	GPIO_163	COMB CTS/GPIO
105	COMB_RTS	UART3_RTS_SD	GPIO_164	COMB RTS/GPIO
106	COMC_TXD	UART2_TX	GPIO_142	COMC transmit/GPIO
107	COMC_RXD	UART2_RX	GPIO_143	COMC receive/GPIO
108	COMC_CTS	UART2_CTS	GPIO_140	COMC CTS/GPIO
109	COMC_RTS	UART2_RTS	GPIO_141	COMC RTS/GPIO
110	COMD_TXD	UART4_TX	GPIO_63	COMD transmit/GPIO
111	COMD_RXD	UART4_RX	GPIO_64	COMD receive/GPIO
112	COMD_CTS	UART4_CTS/CCDC_VD	GPIO_97	COMD CTS/GPIO
113	COMD_RTS	UART4_RTS/CCDC_HD	GPIO_96	COMD RTS/GPIO

3.5.13. GPIO

This section provides for the SoM general purpose IO section. All of these pins can be configured to be general-purpose digital ports. They can also be configured to take advantage of several alternate functions of the AM3517 processor. Alternate functions include Timer/Counters, SPI, I2S, and I2C.

Five of these GPIO lines have been delineated for other optional functionality. For compatibility with other SoMs it is a good idea to not utilize these lines as GPIO unless required. Additionally, the five signals marked with '*' can be used for a second SPI port.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
114	GPIO0	GPT8_PWM_EVT	GPIO_146	GPIO/LCD Backlight On/Off
115	GPIO1	SYS_CLKOUT2	GPIO_186	GPIO
116	GPIO2	MCBSPI4_SIMO	GPIO_158	GPIO
117	GPIO3	MCBSPI4_SOMI	GPIO_159	GPIO
118	GPIO4	HDQ_SIO	GPIO_170	GPIO
119	GPIO5	I2C3_SCL	GPIO_184	GPIO
120	GPIO6	I2C3_SDA	GPIO_185	GPIO
121	GPIO7	MCBSP4_CLKX	GPIO_152	GPIO/USB_Power_Enable
122	GPIO8	MCBSP4_DR	GPIO_153	GPIO/SD_LED
123	GPIO9	MCBSP4_DX	GPIO_154	GPIO/SD_Power
124	GPIO10	MCBSP4_FSX	GPIO_155	GPIO/SD_Protect
125	GPIO11	MCBSPI2_CLK	GPIO_178	GPIO*
126	GPIO12	MCBSPI2_SIMO	GPIO_179	GPIO*
127	GPIO13	MCBSPI2_SOMI	GPIO_180	GPIO*
128	GPIO14	MCBSPI2_CS0	GPIO_181	GPIO*
134	GPIO15	MCBSPI2_CS1	GPIO_182	GPIO*

3.5.14. Touchscreen / Analog-to-Digital Convertor (ADC)

The SoM-200 Pin Specification allocates SoM pins that can be utilized as Touchscreen or ADC inputs. The AM3517 has an external 4 four-wire resistive touchscreen controller (TSC2004). The touchscreen controller has one additional auxiliary ADC input.

SODIMM Pin#	SoM Pin Name	TS2004 Pin Name(s)	Description
45	X+/Xr/ADC0	X+	X+
46	X-/Xl/ADC1	X-	X-
47	Y+/Yu/ADC2	Y+	Y+
48	Y-/Yd/ADC3	Y-	Y-
49	SX+/ADC4	AUX	AUX ADC
50	SX-/ADC5	NC	NC
51	SY+/ADC6	NC	NC
52	SY-/ADC7	NC	NC

3.5.15. LCD

The SoM-200 specification has provision for up to 24-bit LCDs (8-bits per RGB color). These lines can also be used to provide analog VGA connectivity for use with a conventional monitor by adding a video DAC to the Carrier. A Brightness PWM is also provided to allow for software control of the LCD's Brightness. SoM pin# 114 can be used to turn the LCD backlight On and Off if desired.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	SoM Description
57	LCD_BLUE0	DSS_DOUT0	GPIO_70	LCD BLUE0
58	LCD_BLUE1	DSS_DOUT1	GPIO_71	LCD BLUE1
59	LCD_BLUE2	DSS_DOUT2	GPIO_72	LCD BLUE2
60	LCD_BLUE3	DSS_DOUT3	GPIO_73	LCD BLUE3
61	LCD_BLUE4	DSS_DOUT4	GPIO_74	LCD BLUE4
62	LCD_BLUE5	DSS_DOUT5	GPIO_75	LCD BLUE5
63	LCD_BLUE6	DSS_DOUT6	GPIO_76	LCD BLUE6
64	LCD_BLUE7	DSS_DOUT7	GPIO_77	LCD BLUE7
65	LCD_GREEN0	DSS_DOUT8	GPIO_78	LCD GREEN0
66	LCD_GREEN1	DSS_DOUT9	GPIO_79	LCD GREEN1
67	LCD_GREEN2	DSS_DOUT10	GPIO_80	LCD GREEN2
68	LCD_GREEN3	DSS_DOUT11	GPIO_81	LCD GREEN3
69	LCD_GREEN4	DSS_DOUT12	GPIO_82	LCD GREEN4
70	LCD_GREEN5	DSS_DOUT13	GPIO_83	LCD GREEN5
71	LCD_GREEN6	DSS_DOUT14	GPIO_84	LCD GREEN6
72	LCD_GREEN7	DSS_DOUT15	GPIO_85	LCD GREEN7
73	LCD_RED0	DSS_DOUT16	GPIO_86	LCD RED0
74	LCD_RED1	DSS_DOUT17	GPIO_87	LCD RED1
75	LCD_RED2	DSS_DOUT18	GPIO_88	LCD RED2
76	LCD_RED3	DSS_DOUT19	GPIO_89	LCD RED3
77	LCD_RED4	DSS_DOUT20	GPIO_90	LCD RED4
78	LCD_RED5	DSS_DOUT21	GPIO_91	LCD RED5
79	LCD_RED6	DSS_DOUT22	GPIO_92	LCD RED6
80	LCD_RED7	DSS_DOUT23	GPIO_93	LCD RED7
81	LCD_HORZ/LP	DSS_HSYNC	GPIO_67	Horizontal Sync
82	LCD_VERT/FP/FLM	DSS_VSYNC	GPIO_68	Vertical Sync
83	LCD_ENABLE/DE/M	DSS_ACBIAS	GPIO_69	Enable
84	LCD_CLK/SFK/SHFCLK	DSS_PCLK	GPIO_66	LCD Clock
85	BCKLIGHT/PWM	GPT11_PWM_EVT	GPIO_146	Backlight Brightness Control

3.5.16. Boot Options

The SoM specification provides two pins for boot-time configuration. On the SoM-3517M they are used to select between four boot modes.

BOOT1	BOOT0	SYS_BOOT[5:0]	BOOT MODE	Description
0	0	000011	MMC2	Boot from external SD/MMC.
0	1	000110	MMC1	Boot from on-board eMMC.
1	0	000001	NAND	Boot from on-board NAND.
1	1	100100	USB	USB Peripheral Boot.

The SoM-3517M is capable of booting out of 2 GB eMMC, external SD/MMC, or NAND flash.

When booting from NAND or USB, a high capacity (4 GB +) eMMC is accessible from U-Boot and Linux. Boot from serial flash may appear in subsequent revisions to overcome limitations coded into the AM3517's ROM and the availability of NAND flash.

3.5.17. Power Connections

The SoM-9G45/9M10M requires a 3.3V supply for the bus and I/O voltages. The 1.8V core voltage is regulated on module from the 3.3V. Unlike some other modules, no supply voltage other than 3.3V is required.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
3,4,43,44,135, 136,197,198	3.3VCC	3.3VCC	3.3 Volt SoM Supply Voltage
1,2,20,21,41,42, 91,92,137,138, 155,156,199,200	GND	GND	Digital Ground
53	ANALOG_GND	AGND	Analog Ground
56	VSTBY	Vstandby_3.3	Voltage standby, this is the backup voltage provided to the SoM's RTC. If RTC readings are not important for the application, this can be attached to the 3.3V rail.
55	AV_REF	NC	The analog reference for the touchscreen controller is internally connected to 3.3V.

4. Design Considerations

One of the goals of the SoM-3517M is to provide a modular, flexible, and inexpensive solution capable of delivering high-end microcontroller performance.

4.1. The EMAC SoM Carrier-SoM-200ES

EMAC provides an off the shelf carrier for the SoM-3517M module, the SoM-200ES, which provides power to the SoM module as well as wealth of peripheral I/O, including audio and LCD. This board comes with full schematics and BOM, and can be used as is, or as a reference for a customer's own design.

http://www.emacinc.com/som/som200ES.htm

NOTE: When designing a carrier be sure to use a 200 pin DDR1 SODIMM socket instead of the more common DDR2 socket. The DDR2 socket is keyed in such a way as to prevent the SoM from being inserted into it. The part number for a compatible DDR1 socket made by Tyco is 1473005-1. This socket will provide 3.0 mm of height from the top of carrier PCB to the bottom of the module PCB. The module specification allows for a 1.5mm maximum height for bottom components. Therefore, this gives the user less than 1.5mm for placing components safely under the module. If more height is needed, Tyco, as well as other manufacturers, make SODIMM sockets with additional height, though they are more expensive.

If using the SoM-3517's external bus, it is highly recommended buffering the bus on the carrier board in close proximity to the SoM SODIMM connector, (see the SoM-200 carrier schematics for reference).

EMAC also offers a semi-custom, engineering service. By modifying an existing design, EMAC can offer quick-turn, low-cost engineering, for your specific application. Additionally, another off-the-shelf SoM 200 pin carrier is available, the SoM-210ES which is used in the PPC-E4.

4.2. Power

The SoM-3517M requires a voltage of 3.3V at 470mA for normal operation. Users can get away with using only 3.3V and simply provide this to all the voltage inputs listed in 4.1. This, however, will not provide battery backup for the RTC. Additionally, 5V is required if USB Host capability is necessary.

4.2.1. Battery Backup

The real time clock requires a backup voltage to maintain its data. This backup voltage comes from the VSTBY SoM pin and should be connected to 3.3V.

The RTC will draw approximately 8uA when the processor is not powered by the 3.3V supply. Be aware that the static current can rise if the temperature increases to 85° C. When the module is powered, no current is drawn from the backup battery supply. If RTC backup is not needed, this can be tied to 3.3V.

The SoM-200ES provides battery backup voltage through a replaceable BR2032, which is a standard 3V 190mA/H 20MM coin battery that can be picked up from most electronics stores.

4.2.2. Shutdown Logic Pins

The SHDN is a digital output only (0 to 3.3V, pulled up on-module), which is driven by the Shutdown Controller on the processor.

The WKUP pin has a Maximum input voltage of 3.3V, but cannot exceed VDDBU.

Both of these pins are connected directly to the processor.

5. Software

The SoM-3517M offers a wide variety of software support from both open source and proprietary sources. The hardware core was designed to be software compatible with the TI AM3517 reference design, which is supported by Linux and WinCE 6.0.

For more information on Linux Software Support, please visit the EMAC Wiki Software Section at:

http://wiki.emacinc.com/wiki/product_wiki

5.1. Das U-Boot

EMAC utilizes Das U-Boot for its ARM based products. U-Boot is an open source/cross-architecture platform independent bootloader. It supports reading and writing to the flash, auto-booting, environmental variables, and TFTP. Das U-boot can be used to upload and run and/or reflash the OS or to run stand-alone programs without an OS. Products are shipped with a valid MAC address installed in flash in the protected U-boot environmental variable “ethaddr”. At boot time U-Boot automatically stores this address in a register within the MAC, which effectively provides it to any OS loaded after that point.

5.2. Embedded Linux

EMAC Open Embedded Linux is an open source Linux distribution for use in embedded systems. The EMAC OE Linux Build is based on the Open Embedded (www.openembedded.org) Linux build system. Open Embedded is a superior Linux distribution for embedded systems. Custom Linux builds are also available on request.

The distribution contains everything a user could expect from a standard Linux kernel: powerful networking features, advanced file system support, security, debugging utilities, and countless other features.

The basic root file system includes:

- Busybox
- Hotplugging support
- APM utilities for power management
- Openssh SSH server
- lighttpd HTTP server
- JJFS2 or EXT4 file system with utilities

5.2.1. Linux with Xenomai Real Time Extensions

Xenomai provides real time extensions to the kernel and can be used to schedule tasks with hard deadlines and μs latencies. The Xenomai build is an additional module that can be added to the standard Linux kernel and is available for a one-time inexpensive support/installation fee.

http://www.xenomai.org/

5.2.2. Linux Packages

EMAC provides support for many Linux Packages such as: PHP, SQLite, Perl, SNMP, DHCP Server, etc. As with the Xenomai Package, other Packages can be added to the standard Linux file system and are available for a one-time inexpensive support/installation fee.

5.2.3. Linux Patches

In addition to standard Embedded Linux support, EMAC has released a number of patches and device drivers from the open source community and from internal EMAC engineering into its standard distribution. Along with kernel patches, EMAC provides the binaries for the kernel and root file system.

5.3. Qt Creator

Qt Creator is a cross-platform IDE (Integrated Development Environment) tailored to the needs of Qt developers but works well for Headless applications as well. EMAC provides sample code as projects that can be imported into Qt Creator. Qt Creator supports remote deployment and source debugging.

https://qt-project.org/wiki/Category:Tools::QtCreator

5.4. ARM EABI Cross Compiler

The popular open source gcc compiler has a stable build for the ARM family. EMAC uses the 4.9.1 version of the ARM EABI compiler. The Embedded Linux kernel and EMAC Qt Creator projects use this compiler for building ARM stand alone, and OS specific binaries. The EMAC Qt Creator provides source level debugging over Ethernet or serial using gdbserver. The Linux binaries for the ARM EABI cross compiler are available online along with the SDK. See the EMAC wiki for further information.