SoM-3354M

User Manual

REV. 1.2

EMAC, inc.
EQUIPMENT MONITOR AND CONTROL
2390 EMAC Way, Carbondale, Illinois 62902
Phone: (618) 529-4525 Fax: (618) 457-0110
http://www.emacinc.com

Table of Contents

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1. Introduction

This document describes the EMAC SoM-3354M System on Module. The SoM-3354M is designed to be compatible with EMAC's 200-pin SODIMM form factor. This module is built around the Texas Instruments AM3354 ARM Cortex-A8 based microprocessor, which provides several of its key features.

The SoM-3354M has an on-board Ethernet PHY, 4 serial ports, eMMC, USB Switch, SPI flash, and DDR3 SDRAM.

In addition to these standard SoM features, the SoM-3354M also features a fast 32-bit core, hardware graphics accelerators, open source software support, and a wide range of controller IO pins.

1.1. Features

- **Small, 200 pin SODIMM form factor (2.66" x 2.375")**
- **Texas Instruments AM3354 ARM Cortex-A8 1Ghz processor (s-PBGA 324)**
- **10/100BaseT Ethernet with on-board PHY**
- **3 Serial ports with RTS/CTS handshake (transceiver on carrier)**
- **1 Serial port with full handshake (transceiver on carrier)**
- **2 USB 2.0 (High Speed) Host ports (uses a USB Hub chip)**
- **1 USB 2.0 (High Speed) OTG Host/Device port**
- **512 MB of DDR3L SDRAM**
- **16 MB of SPI Flash**
- **4GB eMMC Flash**
- **External MMC/SD card interface with card detect**
- **Real-Time Clock Internal with battery backed provision**
- **2 SPI port**
- **I2C hardware port**
- **Synchronous I2C analog audio interface port**
- **1 CAN port (transceiver on carrier)**
- **2 Timer/Counter/PWM**
- **Internal Resistive Touchscreen Controller with 4-Channel 12-bit Analog-to-Digital converter**
- **16-bit TFT LCD interface**
- **True Random Number Generator**
- **JTAG for debug, including real-time trace**
- **FREE Qt Creator based IDE**

2. Hardware

2.1. Specifications

- **CPU:** Texas Instruments AM3354 processor running at 1 GHz.
- **Flash:** 4GB of eMMC and 16 MB SPI Flash.
- **RAM:** 512MB of DDR3L SDRAM
- **Video:** 2D/3D Accelerated 16 Bit LCD Video Interface with up to 2048 x 2048 resolution.
- **Touchscreen:** 12-Bit, up to 4-wire, 5-wire, 8-wire analog resistive touchscreen interface.
- **Flash Disk:** Up to 16 GB eMMC Flash upgrade.
- **System Reset:** Processor Internal Reset Management with External Reset Button provision.
- **RTC:** Real-Time Clock Internal with battery-backed provision.
- **Timers/Counters:** 2 Timer/Counter/PWM
- **Digital I/O:** Many general purpose I/Os multiplexed with peripheral interfaces.
- **Analog I/O:** 8 channels total, 4 of which is shared by the resistive touchscreen.
- **Power:** Power Management Controller allows selective shutdown capability on processor I/O functionality and running from a slow clock.
- **JTAG**: JTAG for debug, including real-time trace.

Serial Interfaces

- **USB:**
  - 2 USB 2.0 High Speed Host ports.
  - 1 USB 2.0 High Speed Host or Device (USB OTG) software configurable.
- **UARTS:** 3 with RTS/CTS handshaking, 1 with full handshaking.
- **SPI:** 2 High-Speed SPI ports with 4 Chip Slave Selects.
- **I2C:** I2C hardware port
- **Audio:** 2 I2S Synchronous Serial Controller with analog interface support.
- **CAN:** Processor Internal, High End CAN Controller (HECC).

Ethernet Interface

- **MAC:** Ethernet on chip MAC
- **PHY:** Micrel KSZ8041NL with software PHY shutdown control
- **Interface:** IEEE 802.3u 10/100 BaseT Fast Ethernet (requires external magnetics and jack)

Bus Interface

- ARM EBI accessible through SODIMM provides 11 address lines, 8 data bus lines, and control lines.

Mechanical and Environmental

- **Dimensions:** SODIMM form factor with the length dimension extended (2.66" x 2.375")
- **SODIMM TYPE:** 200 Pin DDR1 (not compatible with DDR2 sockets)
- **Power Supply Voltage:** +3.3 Volts DC +/- 5%

- **Typical Power Requirements:**
  - 3.3 Volts @ TBD.
  - Current draw during boot process: TBD.
  - Constant busy loop: TBD.
  - Constant busy loop with Ethernet PHY disabled: TBD
  - Idle system: TBD.
  - Idle system with Ethernet PHY disabled: TBD
  - APM sleep mode using slow clock with Ethernet PHY disabled: TBD
  - APM sleep mode using slow clock with Ethernet PHY enabled: TBD

- **Operating Temperature:** -40 ~ 85° C (-40 ~ 185 ° F), fanless operation.
- **Operating Humidity:** 0% ~ 90% relative humidity, non-condensing

2.2. External Connections

The SoM-3354M connects to a carrier board containing its connectors, power supply and any expansion IO, through a standard gold-plated SODIMM 200-pin connection shown below.

The use of the DDR SODIMM form-factor for EMAC's SoMs is a sound choice that has been proven rugged and reliable in the laptop and embedded SBC markets.

The SoM model will fit in any standard 200-pin DDR1 SODIMM socket (but not DDR2 sockets). These connections are designed according to the 200-pin SoM specification "SOM200_specpublic_xxxxx.pdf" in order to be compatible with all EMAC 200-pin SoMs. See "SOM200_specpublic_xxxxx.pdf" to compare other 200-pin SoM pinouts to the SoM-3354M's pinout.

The remainder of this section describes the pinout as it applies specifically to the SoM-3354M.

2.2.1. System Control & External Bus

The SoM-3354M provides a flexible external bus for connecting peripherals. The CPLD of the SoM-200ES Carrier board connects through a subset of these connections.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
145	GP_CSA	GPMC_CSN1	GPIO 1_30	General Purpose Chip Select CS1
146	GP_CSB	GPMC_CSN2	GPIO 1_31	General Purpose Chip Select CS2
147	GP_CSC	GPMC_CSN3	GPIO 2_0	General Purpose Chip Select CS3
148	GP_CSD/Shutdown	GPMC_CSN6	GPIO 1_28	General Purpose Chip Select CS4
149	~WR	GPMC_WE	GPIO 2_4	Write Signal
150	~RD/TIP	GPMC_OE	GPIO 2_3	Read Signal
151	~RST_IN	SYS_RESETN		Processor Reset
152	~RST_OUT	SYS_RESETN		Processor Reset
153	~WAIT	GPMC_WAIT1	GPIO 2_1	Shutdown Control
154	~FLASH WP	NC		Flash Write Protect
54	WAKEUP	NC		Processor Wakeup Input
157	BOOT_OPTION0	SYS_BOOT[4:0]		Boot0 Option Select
158	BOOT_OPTION1	SYS_BOOT[4:0]		Boot1 Option Select
175-186	A0 – A11	GPMC_A0 – GPMC_A10	GPIO 1_16-1_27	Address Bus
159 – 166	D0 – D7	GPMC_AD0 – GPMC_AD7	GPIO 1_0-1_7	Data Bus
167 – 174	D8 – D15	NC		Data Bus
187-196	A12- A21	NC		Address Bus

2.2.2. USB

The 200-pin SoM specification provides for 2 USB hosts and 1 USB device or OTG port. The AM3354 provides a USB 2.0 OTG port and a USB 2.0 host port interface.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
5	Host_A+	HDPA1		Host USB Switch Port0 + pin
7	Host_A-	HDMA1		Host USB Switch Port0 – pin
6	Host_B+	HDPA2		Host USB Switch Port1 + pin
8	Host_B-	HDMA2		Host USB Switch Port1 – pin
9	Host/Device/OTG_C-	USB0_DM		OTG USB 2.0 Port0 – pin
11	Host/Device/OTG_C+	USB0_DP		OTG USB 2.0 Port0 + pin
10	USB_OTG_VBUS	USB0_VBUS		OTG VBUS
40	USB_OTG_ID	USB0_ID		OTG ID

2.2.3. JTAG

The SoM specification allows for access to the JTAG lines for the AM3354 processor. These connections will allow the Flash to be programmed in circuit via a program running from the processor and also the capability to debug software.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
139	JTAG_TCK	JTAG_TCK	JTAG clock
140	JTAG_TDI	JTAG_TDI	JTAG serial in
141	JTAG_TDO	JTAG_TDO	JTAG serial out
142	JTAG_TMS	JTAG_TMS	JTAG operation mode
143	JTAG_TRST	JTAG_TRST	Test Reset Signal
144	JTAG_RTCK	NC	Dynamic clock sync

2.2.4. Ethernet

The SoM-3354M provides a Micrel KSZ8041 Ethernet 10/100 PHY IC on board. Carrier designers need only to run these lines through the appropriate magnetics layer to have a functional Ethernet connection. Remember, the RX and TX lines are differential pairs and need to be routed as such.

The state of the LED/configuration pins at reset determines the Ethernet's configuration (10-baseT, 100-baseT, autoconfig) and the function of the LED's. The SoM-200ES pulls them all high, which configures the chip for network autoconfig, with ETH_LED1 functioning as an active low link and ETH_LED2 functioning as active low Activity status (Refer to Carrier schematics).

SODIMM Pin#	SoM Pin Name	PHY Pin Name	Description
12	GIG D-	NC	GIG Ethernet D- pin
14	GIG D+	NC	GIG Ethernet D+ pin
13	GIG C- /Host/Device/OTG_C-	NC	GIG Ethernet C- pin
15	GIG C+	NC	GIG Ethernet C+ pin
16	Ethernet_Rx-/GIG B-	Etherent_Rx-	Low differential Ethernet receive line
18	Ethernet_Rx+/GIG B+	Ethernet_Rx+	High differential Ethernet receive line
17	Etherent_Tx-/GIG A-	Etherent_Tx-	Low differential Ethernet transmit line
19	Ethernet_Tx+/GIG A+	Ethernet_Tx+	High differential Ethernet transmit line
38	LED_LINK/CFG_2	ETH_LED1	Ethernet Link LED/Configuration pin
39	LED_ACT/CFG_3	ETH_LED2	Ethernet Activity LED/Configuration pin

2.2.5. I²C

The 200-pin SoM specification calls for a two-wire I²C port. The SoM-3354M has a native hardware I²C port.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
29	I2CCLK	I2C2_SCL	GPIO 3_6	Clock pin
30	I2CDATA	I2C2_SDA	GPIO 3_5	Data pin

2.2.6. SPI

The AM3354 processor provides 4 SPI channels for communicating with peripheral devices. Two of the SPI channels have been provided via the SoM edge connector. The first table below lists the lines for the dedicated SPI channel.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
22	SPI_MI	SPI0_D0	GPIO 0_3	SPI1 serial data in
23	SPI_MO	SPI0_D1	GPIO 0_4	SPI1 serial data out
24	SPI_SCK	SPI0_SCLK	GPIO 0_2	SPI1 serial clock out
25	SPI_CS0	GPMC_AD15	GPIO 1_15	SPI1 slave select line 0
26	SPI_CS1	EMU1	GPIO 3_8	SPI1 slave select line 1
27	SPI_CS2	GPMC_AD14	GPIO 1_14	SPI1 slave select line 2
28	SPI_CS3/SPI _Frame	MCASP0_ACLKR	GPIO 3_18	SPI1 slave select line 3

The table below documents the SPI channel 2, which shares pins in the GPIO pin section.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
125	GPIO11	UART0_CTSn	GPIO 1_8	SPI2 serial data in
126	GPIO12	UART0_RTSn	GPIO 1_9	SPI2 serial data out
127	GPIO13	ECAP0_IN_PWM0_OUT	GPIO 0_7	SPI2 serial clock out

2.2.7. CAN

The AM3354 provides a High-End CAN Controller (HECC) internally. The CAN interface lines are directed to the dedicated CAN pads on the SoM connector as shown in the table below.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Pin Description
93	CANTX	MII1_TXD3	GPIO 0_16	CAN Transmit
94	CANRX	MII1_TXD2	GPIO 0_17	CAN Receive

2.2.8. IRQs

The 200-pin SoM specification allocates three pins as IRQs. The AM3354 processor can use virtually any GPIO pin to trigger an interrupt. EMAC used the following GPIO lines for general purpose IRQs:

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	SoM Description
129	IRQA	XDMA_EVENT_INTR0	GPIO 0_19	Interrupt A
130	IRQB	MCASP0_FSR	GPIO 3_19	Interrupt B
131	IRQC	MCASP0_AHCLKX	GPIO 3_21	Interrupt C

2.2.9. Oscillators

The 200-pin SoM specification provides for two general-purpose oscillators. These frequencies can vary slightly between modules depending on how they are generated and some modules may not provide 50% duty cycles. The AM3354 uses a clock generator chip (Si5351A) to generate these frequencies. The frequencies are programmable via software. The Si5351A also provides the clock source for the on-board Dual UART (TL16C2550IPFB) chip.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	SoM Description
132	OSC0 (high)	N/A	Si5351A (CLK_1)	~ 8 MHz
133	OSC1 (low)	GPMC_BEn0_CLE	GPIO 1_15	~ 200 KHz

2.2.10. SD/Multimedia Card

The AM3354 processor provides multiple 4-bit MMC/SD card interface using the MCI lines. The SoM-200ES & 210ES Carrier boards can use a parallel MMC/SD interface if available.

The 200-pin SoM specification provides for three optional SD/MMC control lines. Since these lines are optional and will not always be used they are not part of the SD/MMC group, but, instead, are part of the

GPIO group. SoM pin#s 122, 123, and 124 can be used as SD_LED, SD_Power, and SD_protect, respectively.

MMC2 is allocated to the SoM Pin Specification in the SD/MMC section as the default SD port. This port should be used to maintain compatibility with past and future modules. As mentioned about the AM3354 processor provides multiple SD ports. The MMC1 port is allocated to the on-module eMMC chip.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
31	SDCLK	GPMC_CSn1	GPIO 1_30	MCI Clock
32	CMD	GPMC_CSn2	GPIO 1_31	MCIA Command
33	DAT0	GPMC_AD8	GPIO 0_22	MCIA D0
34	DAT1	GPMC_AD9	GPIO 0_23	MCIA D1
35	DAT2	GPMC_AD10	GPIO 0_26	MCIA D2
36	DAT3	GPMC_AD11	GPIO 0_27	MCIA D3
37	Card_Detect	GPMC_AD12	GPIO 1_12	Card Detect

2.2.11. I2S Audio

The AM3354 provides multiple I2S audio ports that are accommodated within the SoM specification. Note that there is no CODEC on the SoM and therefore must be provided on the Carrier. In addition the CODEC will require either SPI or I2C for control.

The Master clock is derived by a clock generator chip to drive the Si5351A (CLK_2) 12.288MHZ oscillator. The Si5351A provides the clock source for on board Dual UART (TL16C2550IPFB) chip.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
86	AudioA_SCLK	MCASP0_ACLKX	GPIO 3_14	I2S Serial Clock
87	AudioA_LRCLK/Frame	MCASP0_FSX	GPIO 3_15	I2S Left / Right Clock
88	AudioA_MCLK	N/A	Si5351A (CLK_2)	I2S Master Clock
89	AudioA_DIN	MCASP0_AXR0	GPIO 3_16	I2S Data Input
90	AudioA_DOUT	MCASP0_AXR1	GPIO 3_20	I2S Data Output

2.2.12. Serial Ports

The 200-pin SoM specification has the provision for 4 serial ports. The AM3354 processor provides full modem handshaking for COMA. The SoM-3354M uses a Dual UART (TL16C2550IPFB) chip to provide additional serial ports.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	SoM Description
95	COMA_TXD	EUART0_TX		COMA transmit/GPIO
96	COMA_RXD	EUART0_RX		COMA receive/GPIO
97	COMA_CTS	EUART0_CTS		COMA CTS/GPIO
98	COMA_RTS	EUART0_RTS		COMA RTS/GPIO
99	COMA_DTR	EUART0_DTR		COMA DTR/GPIO
100	COMA_DSR	EUART0_DSR		COMA DSR /GPIO
101	COMA_RI	EUART0_RI		COMA RING/GPIO

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	SoM Description
102	COMB_TXD	UART0_TXD	GPIO 1_11	COMB transmit/GPIO
103	COMB_RXD	UART0_RXD	GPIO 1_10	COMB receive/GPIO
104	COMB_CTS	NC		COMB CTS/GPIO
105	COMB_RTS	NC		COMB RTS/GPIO
106	COMC_TXD	UART1_TXD	GPIO 0_15	COMC transmit/GPIO
107	COMC_RXD	UART1_RXD	GPIO 0_14	COMC receive/GPIO
108	COMC_CTS	UART1_CTSn	GPIO 0_12	COMC CTS/GPIO
109	COMC_RTS	UART1_RTSn	GPIO 0_13	COMC RTS/GPIO
110	COMD_TXD	EUART1_TX		COMD transmit/GPIO
111	COMD_RXD	EUART1_RX		COMD receive/GPIO
112	COMD_CTS	EUART1_CTS		COMD CTS/GPIO
113	COMD_RTS	EUART1_RTS		COMD RTS/GPIO

2.2.13. GPIO

This section provides for the SoM general purpose IO section. All of these pins can be configured to be general-purpose digital ports. They can also be configured to take advantage of several alternate functions of the AM3354 processor.

The SoM-3354M uses a GPIO Expander chip (MCP23S08-E/ML) to provide additional GPIO.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
114	GPIO0	GPMC_AD13	GPIO 1_13	GPIO/LCD Backlight On/Off
115	GPIO1	EGPIO0	GPIO EXPANDER	GPIO
116	GPIO2	EGPIO1	GPIO EXPANDER	GPIO
117	GPIO3	EGPIO2	GPIO EXPANDER	GPIO
118	GPIO4	EGPIO3	GPIO EXPANDER	GPIO
119	GPIO5	EGPIO4	GPIO EXPANDER	GPIO
120	GPIO6	EGPIO5	GPIO EXPANDER	GPIO
121	GPIO7	EGPIO6	GPIO EXPANDER	GPIO
122	GPIO8	EGPIO7	GPIO EXPANDER	GPIO
123	GPIO9	EMU0	GPIO 3_7	GPIO/SD_Power
124	GPIO10	USB0_DRVVBUS	GPIO 0_18	GPIO/SD_Protect
125	GPIO11	UART0_CTSn	GPIO 1_8	GPIO
126	GPIO12	UART0_RTSn	GPIO 1_9	GPIO
127	GPIO13	ECAP0_IN_PWM0_OUT	GPIO 0_7	GPIO
128	GPIO14	GPMC_ADVn_ALE	GPIO 2_2	GPIO
134	GPIO15	XDMA_EVENT_INTR1	GPIO 0_20	GPIO

2.2.14. Touchscreen / Analog-to-Digital Convertor (ADC)

The 200-pin SoM specification allocates SoM pins that can be utilized as Touchscreen or ADC inputs. The AM3354 has a resistive touchscreen controller that can be configured to operate as a 4, 5 or 8-wire interface.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
45	X+/Xr/ADC0	AIN0	X+
46	X-/Xl/ADC1	AIN1	X-
47	Y+/Yu/ADC2	AIN2	Y+
48	Y-/Yd/ADC3	AIN3	Y-
49	SX+/ADC4	AIN4	SX+
50	SX-/ADC5	AIN5	SX-
51	SY+/ADC6	AIN6	SY+
52	SY-/ADC7	AIN7	SY-

2.2.15. LCD

The 200-pin SoM specification has provision for up to 16-bit LCDs (565 RBG mode). These lines can also be used to provide analog VGA connectivity for use with a conventional monitor by adding a video DAC to the Carrier. A Brightness PWM is also provided to allow for software control of the LCD's Brightness. SoM pin# 114 can be used to turn the LCD backlight On and Off if desired.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	SoM Description
57	LCD_BLUE0	LCD_DATA0	GPIO 2_6	LCD BLUE0
58	LCD_BLUE1	LCD_DATA0	GPIO 2_6	LCD BLUE1
59	LCD_BLUE2	LCD_DATA0	GPIO 2_6	LCD BLUE2
60	LCD_BLUE3	LCD_DATA0	GPIO 2_6	LCD BLUE3
61	LCD_BLUE4	LCD_DATA1	GPIO 2_7	LCD BLUE4
62	LCD_BLUE5	LCD_DATA2	GPIO 2_8	LCD BLUE5
63	LCD_BLUE6	LCD_DATA3	GPIO 2_9	LCD BLUE6
64	LCD_BLUE7	LCD_DATA4	GPIO 2_10	LCD BLUE7
65	LCD_GREEN0	LCD_DATA5	GPIO 2_11	LCD GREEN0
66	LCD_GREEN1	LCD_DATA5	GPIO 2_11	LCD GREEN1
67	LCD_GREEN2	LCD_DATA5	GPIO 2_11	LCD GREEN2
68	LCD_GREEN3	LCD_DATA6	GPIO 2_12	LCD GREEN3
69	LCD_GREEN4	LCD_DATA7	GPIO 2_13	LCD GREEN4
70	LCD_GREEN5	LCD_DATA8	GPIO 2_14	LCD GREEN5
71	LCD_GREEN6	LCD_DATA9	GPIO 2_15	LCD GREEN6
72	LCD_GREEN7	LCD_DATA10	GPIO 2_16	LCD GREEN7
73	LCD_RED0	LCD_DATA11	GPIO 2_17	LCD RED0
74	LCD_RED1	LCD_DATA11	GPIO 2_17	LCD RED1
75	LCD_RED2	LCD_DATA11	GPIO 2_17	LCD RED2
76	LCD_RED3	LCD_DATA11	GPIO 2_17	LCD RED3
77	LCD_RED4	LCD_DATA12	GPIO 0_8	LCD RED4
78	LCD_RED5	LCD_DATA13	GPIO 0_9	LCD RED5
79	LCD_RED6	LCD_DATA14	GPIO 0_10	LCD RED6
80	LCD_RED7	LCD_DATA15	GPIO 0_11	LCD RED7
81	LCD_HORZ/LP	LCD_HSYNC	GPIO 2_23	Horizontal Sync
82	LCD_VERT/FP/FLM	LCD_VSYNC	GPIO 2_22	Vertical Sync
83	LCD_ENABLE/DE/M	LCD_AC_BIAS_EN	GPIO 2_25	Enable
84	LCD_CLK/SFK/SHFCLK	LCD_PCLK	GPIO 2_24	LCD Clock
85	BCKLIGHT/PWM	MCASP0_AHCLKR	GPIO 3_17	Backlight Brightness Control

2.2.16. Boot Options

The 200-pin SoM specification provides two pins for boot-time configuration. On the SoM-3354M they are used to select between four boot modes.

BOOT1	BOOT0	SYS_BOOT[4:0]	BOOT MODE	Description
0	0	10110	SPI0	Boot from SPI Flash.
0	1	10111	MMC0	Boot from on-board eMMC (see note)
1	0	10110	UART0/EMAC1	Boot from Serial/Ethernet.
1	1	10111	UART0/USB0	Boot from Serial/USB.

The SoM-3354M is capable of booting out of Serial, Ethernet, SPI Flash, or USB. Booting from eMMC is only possible with a custom populated version. Contact EMAC for more details. Minimum purchase quantities apply.

2.2.17. Power Connections

The SoM-3354M requires a 3.3V supply for the bus and I/O voltages. The 1.8V core voltage is regulated on module from the 3.3V. Unlike some other modules, no supply voltage other than 3.3V is required.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
3,4,43,44,135, 136,197,198	3.3VCC	3.3VCC	3.3 Volt SoM Supply Voltage
1,2,20,21,41,42, 91,92,137,138, 155,156,199,200	GND	GND	Digital Ground
53	ANALOG_GND	AGND	Analog Ground
56	VSTBY	Vstandby_3.3	Voltage standby, this is the backup voltage provided to the SoM's RTC. If RTC readings are not important for the application, this can be attached to the 3.3V rail.
55	AV_REF	NC	The analog reference for the touchscreen controller is internally connected to 3.3V.

2.3. Real-Time Clock

The real-time clock is a precise timer which can generate interrupts on intervals specified by the user. The RTC is internal and on the AM3354 processor.

2.4. Watchdog Timer

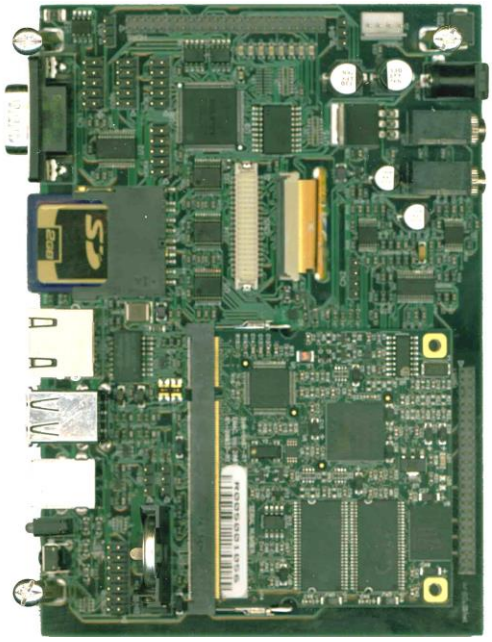
A 32 kHz clock drives the AM3354 internal watchdog timers. Each timer contains a free-running, 32-bit up counter. Each counter has an 8-bit, programmable clock divider. Timeout events can trigger reset and interrupt events.

2.5. Status LED

The SoM-3354M provides a user programmable, green, status LED. To control this LED, use GPIO port line GPIO3_4. Setting the port line high will turn on the LED.

3. Design Considerations

One of the goals of the SoM-3354M is to provide a modular, flexible, and inexpensive solution capable of delivering high-end microcontroller performance.



3.1. The EMAC SoM Carrier-SoM-200ES

EMAC provides an off the shelf carrier for the SoM-3354M module, the SoM-200ES, which provides power to the SoM module as well as wealth of peripheral I/O, including audio and LCD. This board comes with full schematics and BOM, and can be used as is, or as a reference for a customer's own design.

http://www.emacinc.com/som/som200ES.htm

NOTE: When designing a carrier be sure to use a 200 pin DDR1 SODIMM socket instead of the more common DDR2 socket. The DDR2 socket is keyed in such a way as to prevent the SoM from being inserted into it. The part number for a compatible DDR1 socket made by Tyco is 1473005-1. This socket will provide 3.0 mm of height from the top of carrier PCB to the bottom of the module PCB. The module specification allows for a 1.5mm maximum height for bottom components. Therefore, this gives the user less than 1.5mm for placing components safely under the module. If more height is needed, Tyco, as well as other manufacturers, make SODIMM sockets with additional height, though they are more expensive.

If using the SoM-3354M's external bus, it is highly recommended buffering the bus on the carrier board in close proximity to the SoM SODIMM connector, (see the SoM-200 carrier schematics for reference).

EMAC also offers a semi-custom, engineering service. By modifying an existing design, EMAC can offer quick-turn, low-cost engineering, for your specific application. Additionally, another off-the-shelf SoM 200 pin carrier is available, the SoM-210ES which is used in the PPC-E4.

3.2. Power

The SoM-3354M requires a voltage of 3.3V at 650mA for normal operation. Users can get away with using only 3.3V and simply provide this to all the voltage inputs listed in section 2.2.17 of this manual. This, however, will not provide battery backup for the real-time clock. Additionally, 5V is required if USB Host capability is necessary.

3.2.1. Battery Backup

The real-time clock (RTC) requires a backup voltage to maintain its data. This backup voltage comes from the VSTBY SoM pin and should be connected to 3.3V.

The RTC will draw approximately 8uA when the processor is not powered by the 3.3V supply. Be aware that the static current can rise if the temperature increases to 85° C. When the module is powered, no current is drawn from the backup battery supply. If RTC backup is not needed, this can be tied to 3.3V.

The SoM-200ES provides battery backup voltage through a replaceable BR2032, which is a standard 3V 190mA/H 20MM coin battery that can be picked up from most electronics stores.

3.2.2. Shutdown Logic Pins

- GP_CSD/ShutDown is used only as GP_CSD. This is implemented using gpmc_csn6 (GPMC chip select 6).
- WKUP is not connected.

4. Software

The SoM-3354M offers a wide variety of software support from both open source and proprietary sources. The hardware core was designed to be software compatible with the TI AM3354 reference design, which is supported by Linux.

4.1. Qt Creator

Qt Creator is a cross-platform IDE (Integrated Development Environment) tailored to the needs of Qt developers but works well for Headless applications as well. EMAC provides sample code for the SoM-3354M as projects that can be imported into Qt Creator. Qt Creator supports remote deployment and source debugging.

https://qt-project.org/wiki/Category:Tools::QtCreator

EMAC provides a custom version of Qt Creator based on the 3.1.0 release. This custom version includes examples and documentation relevant to EMAC customers. EMAC also provides a getting started guide for Qt Creator as a separate document.

4.2. Das U-Boot Bootloader

The SoM-3354M is distributed with Das U-Boot installed. U-Boot is an open source/cross-architecture platform independent bootloader. It supports reading and writing to the flash, auto-booting, environmental variables, and TFTP. Das U-boot can be used to upload, run, and/or re-flash the OS on the SoM-3354M or to run stand-alone programs without an OS. SoM-3354M modules are shipped with a valid MAC address installed in flash in the protected ethaddr environmental variable of U-Boot. At boot time, U-Boot automatically stores this address in a register within the MAC, which effectively provides it to any OS loaded after that point.

4.3. Embedded Linux

EMAC Open Embedded Linux is an open source Linux distribution for use in embedded systems. The current SoM-3354M build uses a Linux 4.x kernel that has been has been patched to support the SoM-3354M and SoM-200ES devices.

The distribution contains everything a user could expect from a standard Linux kernel: powerful networking features, advanced file system support, security, debugging utilities, and countless other features.

The SoM-3354M will work out of the box with EMAC's Embedded Linux distribution, and EMAC provides the most up to date distribution via GIT. The SoM-3354M comes preinstalled with a version 4.x or later Linux kernel.

The Bootloader / Linux Console Port defaults to:

- COMB
- 115200 Baud
- N-8-1
- No Handshaking

4.3.1. Linux with Xenomai Real Time Extensions

Xenomai provides real time extensions to the kernel and can be used to schedule tasks with hard deadlines and μs latencies. The Xenomai build is an additional module that can be added to the standard Linux kernel and is available for a one-time, inexpensive support/installation fee.

http://www.xenomai.org/

4.3.2. Linux Modules

EMAC provides support for many Linux modules such as: Lighttpd Web Server, PHP, SQLite, Perl, SNMP, DHCP Server, etc. Also, other modules can be added to the standard Linux file system and are available for an inexpensive, one-time support/installation fee.

4.3.3. Linux Patches

In addition to standard Embedded Linux support, EMAC has released a number of patches and device drivers from the open source community and from internal EMAC engineering into its standard distribution. Along with kernel patches, EMAC provides the binaries for the kernel and root file system upon request.

4.4. Open Embedded

The Linux build for the SoM-3354M is based on the Open Embedded (www.openembedded.org) Linux build system. The current kernel is Linux 3.19.0 or higher patched to support the SoM-3354M. Open Embedded is a Linux distribution for embedded systems. Custom Linux builds are also available on request.

The basic root file system includes:

- Busybox
- Hotplugging support
- APM utilities for power management
- Openssh SSH server
- lighttpd HTTP server
- EXT4 filesystem with utilities

4.5. ARM EABI Cross Compiler

The popular open source GCC compiler has a stable build for the ARM family. EMAC uses the 4.9.1 version of the ARM EABI compiler. The Embedded Linux kernel and EMAC Eclipse CDT projects use this compiler for building ARM stand alone and OS specific binaries. The EMAC Eclipse SDK provides source level debugging over either the JTAG port, over Ethernet, or serially using gdbserver. The Linux binaries for the ARM EABI cross compiler are available online along with the SDK for the SoM-3354M at the following location.