Chapter 4

Driver Installation

4.1 Software Drivers

This chapter describes the operation and installation of the display drivers supplied on the Supporting CD-ROM that are shipped with your product. The onboard VGA adapter is based on the AMD LX VGA Flat Panel/CRT controller. This controller offers a large set of extended functions and higher resolutions. The purpose of the enclosed software drivers is to take advantage of the extended features of the AMD LX VGA Flat Panel/CRT controller.

Hardware Configuration

Some of the high-resolution drivers provided in this package will work only in certain system configurations. If a driver does not display correctly, try the following:

1. Change the display controller to CRT-only mode, rather than flat panel or simultaneous display mode. Some high-resolution drivers will display correctly only in CRT mode.

2. If a high-resolution mode does not support your system, try to use a lower-resolution mode. For example, 1024 x 768 mode will not work on some systems, but 800 x 600 mode supports the most.

4.2 Necessary to Know

The instructions in this manual assume that you understand elementary concepts of MS-DOS and the IBM Personal Computer. Before you attempt to install any driver from the *Supporting CD-RO*M, you should:

- Know how to copy files from a CD-ROM to a directory on the hard disk
- Understand the MS-DOS directory structure

  If you are uncertain about any of these concepts, please refer to the DOS or OS/2 user reference guides for more information before you proceed with the installation.

Before you begin

The Supporting CD-ROM contains different drivers for corresponding Windows OS, please choose the specific driver for your Windows OS.

4.3 Installing VGA Driver

Win XP / Win XPe VGA

Place the Driver CD-ROM into your CD-ROM drive and follow the steps below to install.

1. Click on **Start** button.
2. Click on **Settings** button.
3. Click on **Control Panel** button.
4. Click on **System** button.
5. Select **Hardware** and click on **Device Manager…**.
6. Double click on **Video Controller (VGA Compatible)**.
7. Click on **Update Driver…**.
8. Click on **Next**.
9. Select **Search for a suitable driver…**, then click on **Next**.
10. Select **Specify a location**, then click on **Next**.
11. Click on **Browse**.
12. Select "l**x_win"** file from CD-ROM **(Driver/Step 1 – LX_Graphics)** then click on **Open**.
13. Click on **OK**.
14. Click on **Next**.
15. Click on **Yes**.
16. Click on **Finish**.

Note: The user must install this system driver before install other device drivers.

4.4 Installing AES Driver

Win XP / Win XPe Geode LX AES Crypto

Place the Driver CD-ROM into your CD-ROM drive and follow the steps below to install.

1. Click on **Start** button.
2. Click on **Settings** button.
3. Click on **Control Panel** button.
4. Click on **System** button.
5. Select **Hardware** and click on **Device Manager…**.
6. Double click on **Entertainment Encryption/Decryption Controller**.
7. Click on **Update Driver…**.
8. Click on **Next**.
9. Select **Search for a suitable driver…**, then click on **Next**.
10. Select **Specify a location**, then click on **Next**.
11. Click on **Browse**.
12. Select **"GeodeLX_XP_WDM_AES_v2.01.00"** file from CD-ROM **(Driver/Step 2 – AES)** then click on **Open**.
13. Click on **OK**.
14. Click on **Next**.
15. Click on **Yes**.
16. Click on **Finish**.

4.5 Installing PCI to ISA Bridge Driver

Win XP / Win XPe System

Place the Driver CD-ROM into your CD-ROM drive and follow the steps below to install.

1. Click on **Start** button.
2. Click on **Settings** button.
3. Click on **Control Panel** button.
4. Click on **System** button.
5. Select **Hardware** and click on **Device Manager…**.
6. Double click on **Other PCI Bridge Device**
7. Click on **Update Driver…**.
8. Click on **Next**.
9. Select **Search for a suitable driver…**, then click on **Next**.
10. Select **Specify a location**, then click on **Next**.
11. Click on **Browse**.
12. Select "**Ite**" file from CD-ROM **(Driver/Step 3 – PCI to ISA Bridge)** then click on **open**.
13. Click on **OK**.
14. Click on **Next**.
15. Click on **Finish**.

4.6 Installing Ethernet Driver

Place the Driver CD-ROM into your CD-ROM drive and follow the steps below to install.

1. Click on **Start** button.
2. Click on **Settings** button.
3. Click on **Control Panel** button.
4. Click on **System** button.
5. Select **Hardware** and click on **Device Manager…**.
6. Double click on **Ethernet Controller**.
7. Click on **Update Driver…**.
8. Click on **Next**.
9. Select **Search for a suitable driver…**, then click on **Next**.
10. Select **Specify a location**, then click on **Next**.
11. Click on **Browse**.
12. Select **"**Select "**Intel 82551ER Driver**" folder from CD-ROM (**Driver/Step 4 - Intel LAN driver**) then click on **Open**.
13. Click on **OK**.
14. Click on **Next**.
15. Click on **Yes**.
16. Click on **Finish**

Appendix

A

Programming the Watchdog Timer

A.1 Programming

PFM-541I utilizes SCH3114-NU chipset as its watchdog timer controller.

The SCH311X WDT (Watch Dog Timer) has a programmable time-out ranging from 1 to 255 minutes with one minute resolution, or 1 to 255 second resolution. The unit of the WDT timeout value are selected via bit[7] of the WDT_TIMEOUT register. The WDT time-out value is set through the WDT_VAL Runtime register. Setting The WDT_VAL register to 0x00 disables the WDT function (this is its power on default).
Setting the WDT_VAL to any other non-zero value will cause the WDT to reload and begin counting down from the value loaded. When the WDT count value reaches zero the counter stops and sets the Watchdog time-out status bit in the WDT_CTRL Runtime register. Note: Regardless of the current state of the WDT, the WDT time-out status bit can be directly set or cleared by the Host CPU.

The related register for configuring WDT is list as follows:

NAME	REG OFFSET (HEX)	DESCRIPTION
GP60 Default = 0x01 on VTR POR	47 (R/W)	General Purpose I/O bit 6.0 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11=WDT 10=Either Edge Triggered Interrupt Input 4 (Note 26.20) 01=LED1 00=GPIO Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

WDT_TIME_OUT Default = 0x00 on VCC POR, VTR POR, and PCI Reset	65 (R/W)	Watch-dog Timeout Bit[0] Reserved Bit[1] Reserved Bits[6:2] Reserved, = 00000 Bit[7] WDT Time-out Value Units Select = 0 Minutes (default) = 1 Seconds
WDT_VAL Default = 0x00 on VCC POR, VTR POR, and PCI Reset	66 (R/W)	Watch-dog Timer Time-out Value Binary coded, units = minutes (default) or seconds, selectable via Bit[7] of WDT_TIME_OUT register (0x52). 0x00 Time out disabled 0x01 Time-out = 1 minute (second) ..... 0xFF Time-out = 255 minutes (seconds)

NAME	REG OFFSET (HEX)	DESCRIPTION
WDT_CFG Default = 0x00 on VCC POR, VTR POR, and PCI Reset	67 (R/W)	Watch-dog timer Configuration Bit[0] Reserved Bit[1] Keyboard Enable =1 WDT is reset upon a Keyboard interrupt. =0 WDT is not affected by Keyboard interrupts. Bit[2] Mouse Enable =1 WDT is reset upon a Mouse interrupt. =0 WDT is not affected by Mouse interrupts. Bit[3] Reserved Bits[7:4] WDT Interrupt Mapping 1111 = IRQ15 ..... 0011 = IRQ3 0010 = IRQ2 (Note) 0001 = IRQ1 0000 = Disable Note: IRQ2 is used for generating SMI events via the serial IRQ's stream. The WDT should not be configured for IRQ2 if the IRQ2 slot is enabled for generating an SMI event.
WDT_CTRL Default = 0x00 on VCC POR and VTR POR Default = 0000000xb on PCI Reset Note: Bit[0] is not cleared by PCI Reset	68 (R/W) Bit[2] is Write-Only	Watch-dog timer Control Bit[0] Watch-dog Status Bit, R/W =1 WD timeout occurred =0 WD timer counting Bit[1] Reserved Bit[2] Force Timeout, W =1 Forces WD timeout event; this bit is self-clearing Bit[3] P20 Force Timeout Enable, R/W = 1 Allows rising edge of P20, from the Keyboard Controller, to force the WD timeout event. A WD timeout event may still be forced by setting the Force Timeout Bit, bit 2. **Note**: If the P20 signal is high when the enable bit is set a WD timeout event will be generated. = 0 P20 activity does not generate the WD timeout event. Note: The P20 signal will remain high for a minimum of 1us and can remain high indefinitely. Therefore, when P20 forced timeouts are enabled, a self-clearing edge-detect circuit is used to generate a signal which is OR'ed with the signal generated by the Force Timeout Bit. Bit[7:4] Reserved. Set to 0

The following is a sample code to set WDT for 3 seconds.

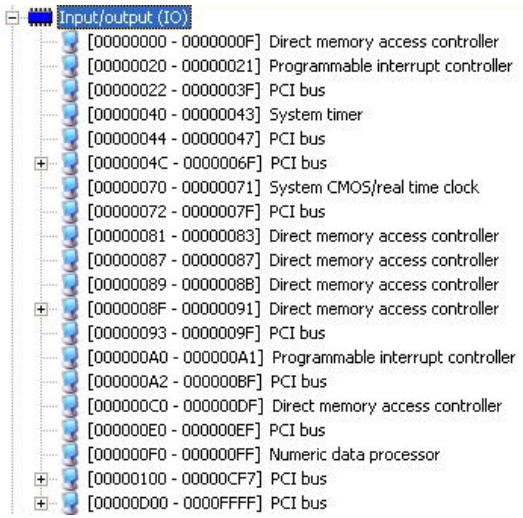
```
;Runtime register I/O base address
SUPERIO_GPIO_PORT        EQU    800h
.MODEL      SMALL
.CODE

begin:
      ;enable WDT
         mov  dx, SUPERIO_GPIO_PORT + 47h
        mov   al, 0Ch
        out     dx, al
      ;WDT_TIME_OUT register
         mov  dx, SUPERIO_GPIO_PORT + 65h
        mov   al, 80h                          ;unit is second
        out     dx, al
      ;WDT_VAL register
        mov   dx, SUPERIO_GPIO_PORT + 66h
        mov    al, 03h                         ;3 seconds
        out     dx, al
       ;exit
        mov   ah,4ch
        int      21h

        END  begin
```

Appendix

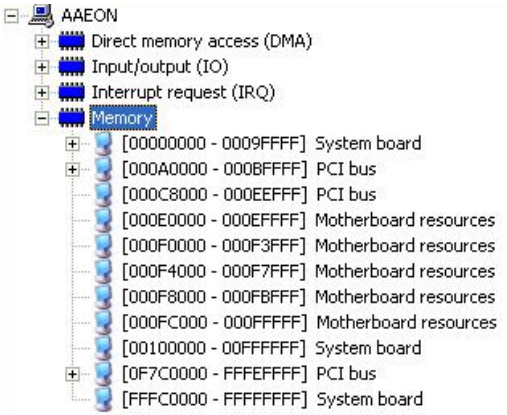
B

I/O Information

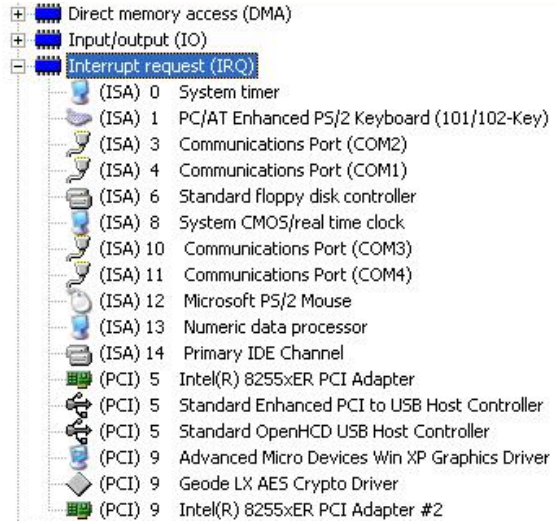
B.1 I/O Address Map



B.2 1st MB Memory Address Map



B.3 IRQ Mapping Chart



B.4 DMA Channel Assignments

Appendix C

Mating Connecotor