EmbedDisk UltraDMA Datasheet

Version 1.0

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DMP Electronics Inc.
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A. Product Information

Dependable and secure

Designed with advanced IDE flash controller technology, EmbedDisk is 100% compatible with the standard IDE/ATA storage interface without the need for special device driver. This advanced multi-tasking IDE flash controller's integrated error-detection, error-correction, re-mapping and wear-leveling technologies with power hold-up circuit greatly improves data reliability. Its low-power requirement, advanced UltraDMA modes, multi-sector transfer support and LBA addressing can satisfy application with high performance and reliability requirements.

Anti Shock & Anti Vibration

Using advanced solid-state storage technology, without moving parts, EmbedDisk is able to perform all of its designated function without being affected by shock and vibration.

Wide Operating Temperature

EmbedDisk is designed to support commercial and industrial applications operating in environment exposed to extreme temperature range. The EmbedDisk series supports **-20ºC to +75ºC** operating temperature.

B. System Features

- -20 ºC to +75ºC extended temp range
- RoHS (Lead-free) ready
- Low power operation
- Ultra DMA Mode 4
- Unitized 40/44 pin IDE
- Industry ATAPI-5 Standard compliant
- Wear-leveling algorithm ensure
- 16-bit NAND flash devices supported
- Dual channel operation for performance enhancement
- High reliability internal ECC function
- Power & Active LEDs
- Completely solid state – no moving parts
- Entirely bootable for current embedded O/S
- 1000G operating shock
- 20G operating vibration

Specifications:

◆ **Compatibility**	PC ATA and True IDE	
◆ **Flash technology**	NAND Type SLC flash base	
◆ **Form factor**	40-pin vertical type	
	40-pin horizontal type right forwards	
	40-pin horizontal type left forwards	
	44-pin vertical type	
	44-pin horizontal type right forwards	
	44-pin horizontal type left forwards	
◆ **Connector types**	40-pin 2.54mm female IDE connector	
	44-pin 2.00mm female IDE connector	
◆ **Capacity supported**	128MB , 256MB, 512MB, 1GB, 2GB, 4GB	
◆ **Master/Slave setup**	By switch	
◆ **System performance**		
Data transfer mode	PIO mode 4	
	UltraDMA Mode 4	
Sequential read	20 Mbytes/sec Max.	
Sequential write	19 Mbytes/sec Max.	
Average access time	2ms(estimated)	
◆ System Performance		
Temperature	Operation Temperature -20°C ~ +75°C	
	Non-operating Temperature -20°C ~ +80°C	
Humidity	5 ~ 95% non-condensing	
Vibration	20G	
Shock	1500G	
◆ Reliability		
MTBF	>1,000,000 hours	
ECC	4 bits ECC Code	
Endurance	Greater than 1,000,000 Cycles Logically	
	Contributed by Wear-leveling and Advanced	
	Bad Sector Management Algorithms	
Data reliability	< 1 Non-recoverable Error 10^{14} bits read	
Data retention	10 years	
◆ Power Consumption		
Power voltage	+3.3V ± 5%	+5.0V ± 10%
Read	32mA(Typ)	36mA(Typ)
Write	44mA(Typ)	48mA(Typ)
Sleep mode	14.3mA(Typ.)	16.2mA(Typ)
◆ Certification	CE、FCC、ROHS	
◆ Warrantee	3 Years	

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Configuration:

The specific capacity for the various models and the default number of heads, sectors/track and cylinders

Unformatted Capacity	Default Cylinder	Default Head	Default Sector	Default CHS Capacity
128MB	978	8	32	128,188,416
256MB	978	16	32	256,376,832
512MB	993	16	63	512,483,328
1,024MB	1,985	16	63	1,024,450,560
2.04GB	3,954	16	63	2,040,643,584
4GB	7,889	16	63	4,071,481,344

Pin Assignments:

Pin No.	Signal	Function	Pin No.	Signal	Function
1	RESET	Host reset	2	GND	Ground
3	HD07	Host data bus bit 7	4	HD08	Host Data Bus Bit 8
5	HD06	Host data bus bit 6	6	HD09	Host Data Bus Bit 9
7	HD05	Host data bus bit 5	8	HD10	Host Data Bus Bit 10
9	HD04	Host data bus bit 4	10	HD11	Host Data Bus Bit 11
11	HD03	Host data bus bit 3	12	HD12	Host data bus bit 12
13	HD02	Host data bus bit 2	14	HD13	Host data bus bit 13
15	HD01	Host data bus bit 1	16	HD14	Host data bus bit 14
17	HD00	Host data bus bit 0	18	HD15	Host data bus bit 15
19	GND	Ground	20	KEYPIN	Cut pin
21	DMARQ	DMA request	22	GND	Ground
23	DIOW	Host i/o write	24	GND	Ground
25	DIOR	Host i/o read	26	GND	Ground
27	IORDY	I/O ready	28	CSEL	Master/slave select
29	DMACK	DMA acknowledge	30	GND	Ground
31	INTRQ	Interrupt request	32	IOCS16	CS I/O 16 bit
33	A01	Host address bit 1	34	PDIAG	Passed diagnostics
35	A00	Host address bit 0	36	A02	Host address bit 2
37	CS0	Chip select 0	38	CS1	Chip select 1
39	DASP	Drive active/ Drive 1 present	40	GND	Ground
41	NC	Not connected	42	VCC	Supply voltage
43	GND	Ground	44	RESERVED	Reserved

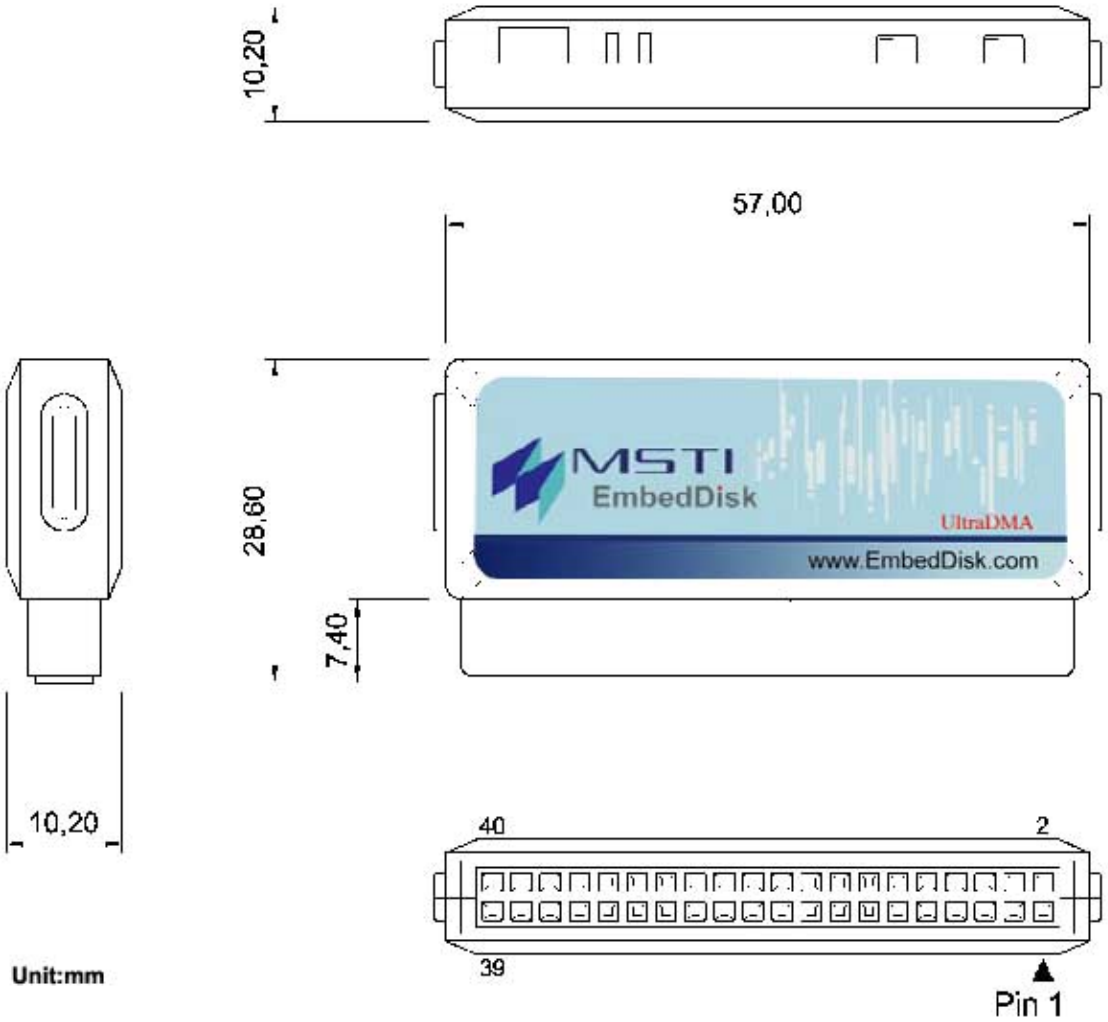
Pin Description:

Signals	Pin No.	Description	Signal Type
HD15 –HD0	3-18	Host Data bus [15:0]. 16 –bit bi-directional data input / output bus. HD15 is the most significant bit, while DH0 is the least significant bit. This bus carries data, commands and status information between the host and EMBEDDISK. The lower 8 bits are used for 8-bit register transfers. Data transfers are 16 bits wide.	I/O
HA2 –HA0	33,35,36	Host Address bus HA[2:0]. Select the registers in the EMBEDDISK controller.	Input
DIOW	23	Device I/O Write: Active low. Gates the data form the bus to EMBEDDISK. The clocking occurs on the rising edge of the signal.	Input
DIOR	25	Device I/O Read: Active low. Gates the data to the bus from EMBEDDISK. The clocking occurs on the falling edge of the signal.	Input
CSEL	28	Configuration Select: Determines the device configuration as either Master or Slave. If CESL is negated, then the device address is Master; if CSEL is asserted, then the device address is Slave.	Input
CS0	37	Host Chip Select 0: Active low. Selects the Command Block registers.	Input
CS1	38	Host Chip Select 1: Active low. Selects the Command Block registers.	Input
RESET	1	Host reset: Active low.	Input
IORDY	27	I/O Ready: Negated by EMBEDDISK to extend the host transfer cycle (read or write) when the device is not ready to respond to a data transfer request.	Output
DMARQ	21	DMA Request: This signal, used for DMA data transfers between the host and EMBEDDISK, is asserted by EMBEDDISK when it is ready to transfer data to or from the host. The direction of data transfer is controlled by DIOR# and DIOW#. This signal is used in a handshake manner with DMACK#, meaning EMBEDDISK waits until the host asserts DMACK# before negating DMARQ, and re-asserting DMARQ if there is more data to transfer. This line is released (high impedance state) whenever EMBEDDISK is not selected, or is selected and no DMA command is in progress. When enabled by DMA transfer, DMARQ is driven high and low by the device.	Output

		When a DMA operation is enabled, CS0# and CS1# are asserted and transfers are 16 bits wide.	
DMACK	29	DMA Acknowledge: This signal shell be used by the host in response to DMARQ to initiate DMA transfers	Input
INTRQ	31	Interrupt Request: Interrupt request from EMBEDDISK to the host. The output of this signal is tri-stated if the host disables the interrupt. When asserted, this signal is negated by the device within 400 nsec of the negation of the DIOR# signal that reads the Status register. When asserted, this signal is negated by the device within 400 nsec of the negation of the DIOW# signal that writes the Command register.	Output
IOCS16	32	I/O IS I6-Bit: Active low. Asserted (low) by EMBEDDISK to indicate to the host that the current cycle is a 16-bit (word) data transfer. When the signal is negated (high), an 8-bit data transfer is performed.	Output
PDIAG	34	Passed Diagnostics: Active low. Informs the Master drive that the self-diagnostic of the Slave drive has ended.	I/O
DASP	39	Drive Active/Drive1 Present: Active low. This is a time-multiplexed signal that indicates that a device is active, or that Device 1 is present.	I/O
GND	2,19,22,24, 26,30,40,43	Ground	Ground
VCC	42	Power Supply	Supply
NC	41,42	Not connected	N/A

Physical Specifications

Type	40V0 Type	40HL & 40HR	44V0 Type	44HL & 44HR
Length:	57.2mm	51.85mm	49.95mm	45.05mm
Width:	28.60mm	26.50mm	27.35mm	27.00mm
Thickness:	10.20mm	8.70mm	9.90mm	5.75mm
Weight:	20g	15g	15g	10g



40 Pin Vertical

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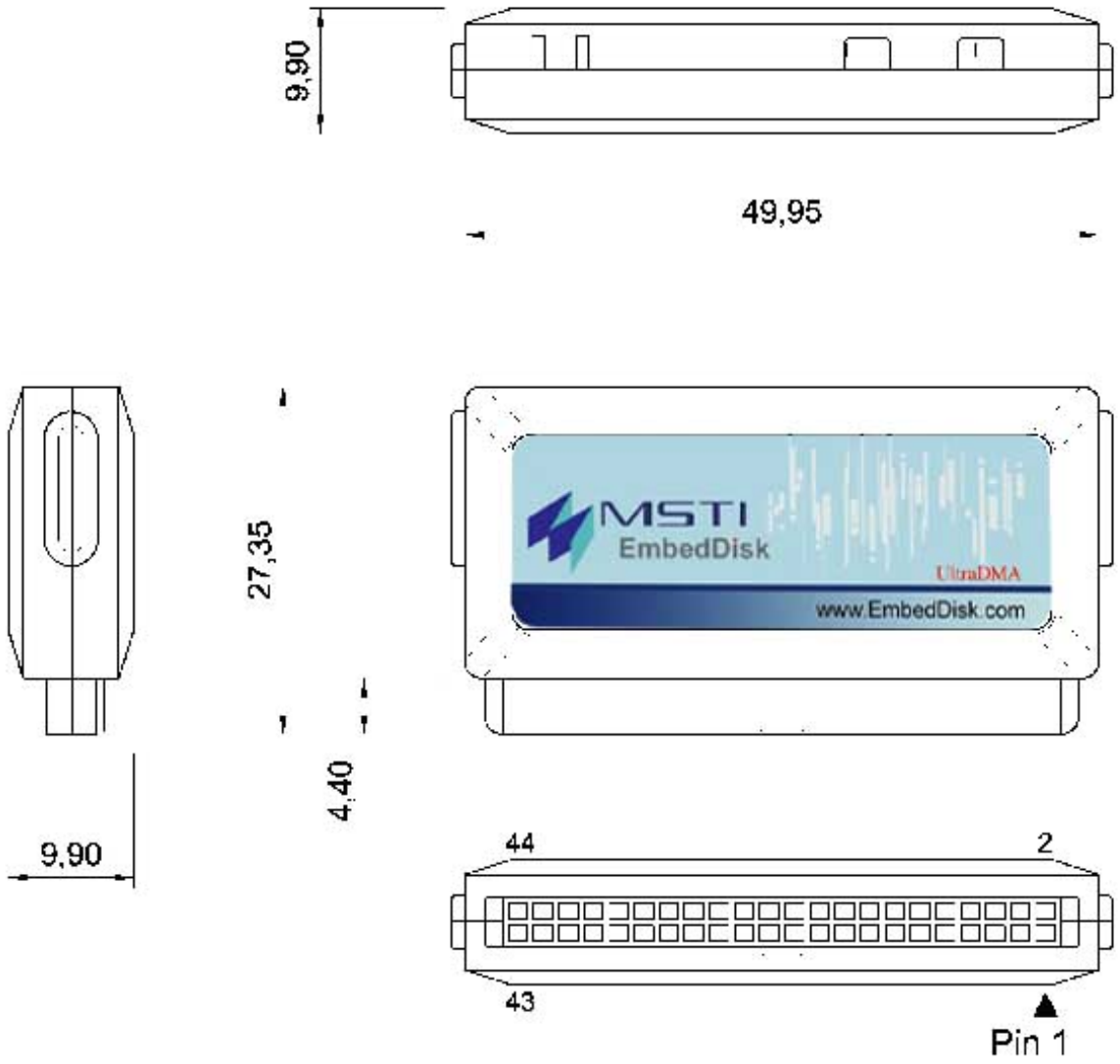

44 Pin Vertical

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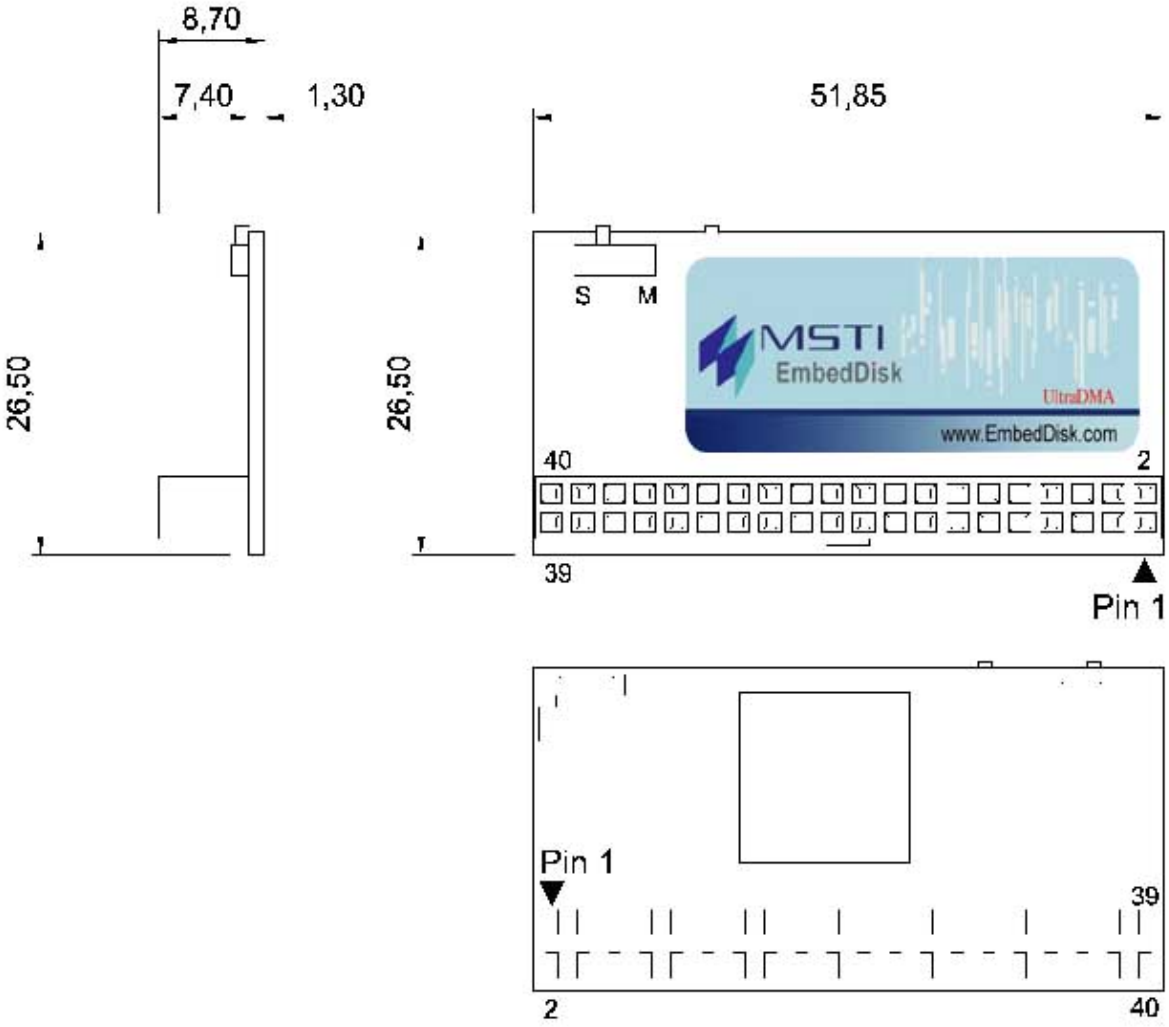

40 Pin Horizontal

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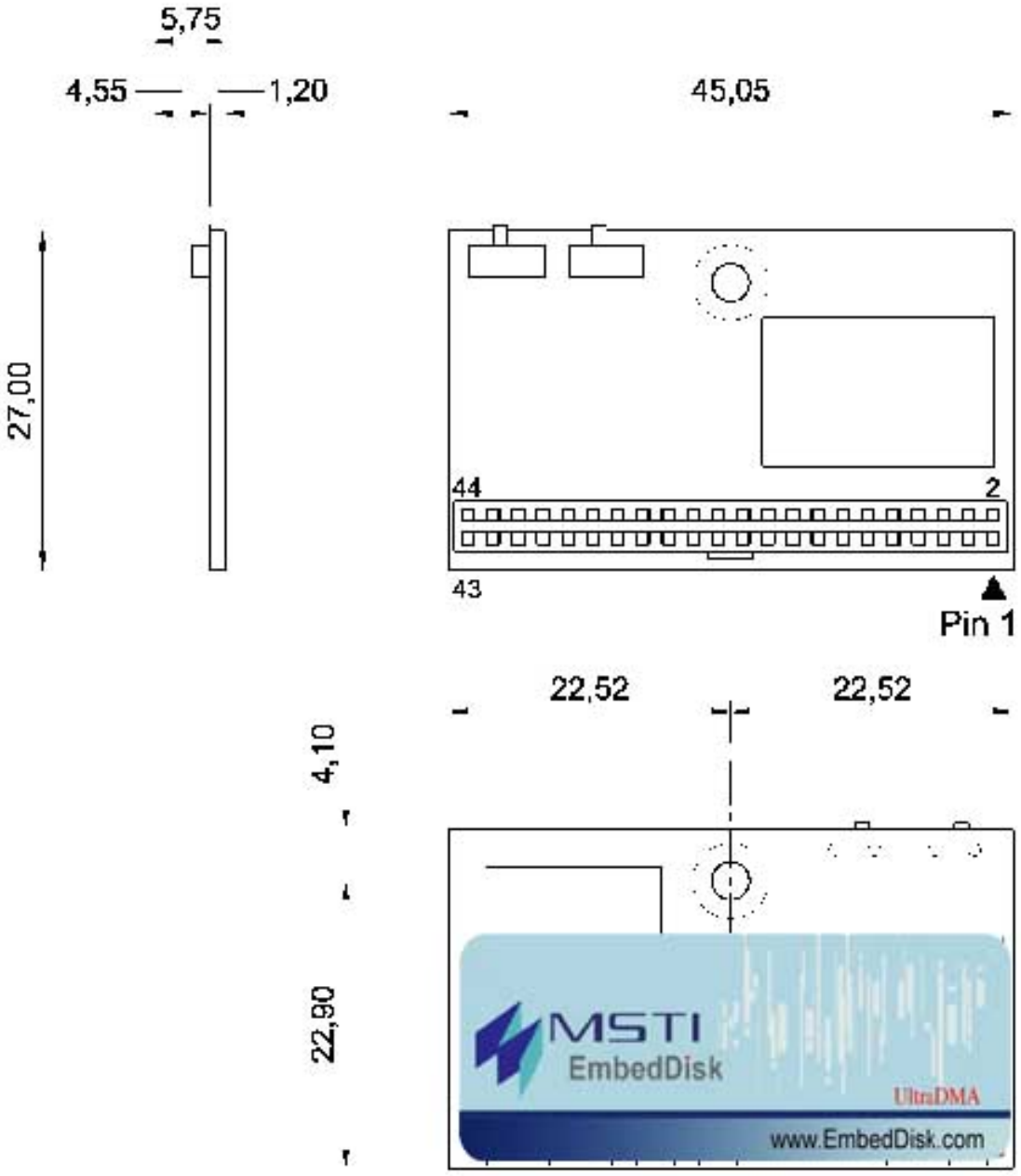

44 Pin Horizontal

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