SoM-NE64M

User Manual

REV. 0.2

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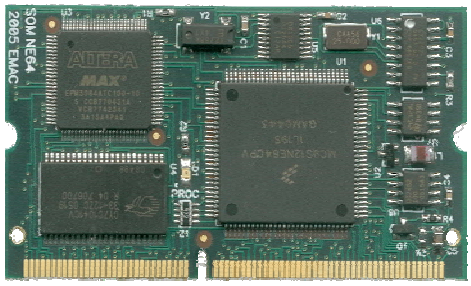
2 Introduction



This document describes EMAC's SoM-NE64M (SBC) module that is built around Freescale Semiconductor's MC9S12NE64 which is a 16-bit 25MHz ethernet-ready HC12 derivative. The SoM-NE64M is part of EMAC's SODIMM form factor System on Module (SoM) product family. The standard form factor and pinout allows for an easy migration path when an application's processing requirements grow, or when additional features are needed. Like all SoM modules, the SoM-NE64 is designed to plug into a Carrier board such as the SoM-100ES. Schematics of the SoM-100ES Carrier board are available for customers wishing to design their own Carrier boards.

The SoM module not only contains the Processor, but Memory (Flash/RAM), Ethernet MAC/PHY, Clock/Calendar, and some digital/analog I/O. The Carrier board provides the connectors for the various I/O plus additional I/O such as 12 bit A/D & D/A, keypad/LCD interface, digital I/O etc. The module must be plugged into a carrier in order to be used.

2.1 Features

- **Small, SoM compatible SODIMM form factor 2.66" x 1.50"**
- **10/100 Base-T Ethernet with on-board PHY**
- **Real-Time Clock**
- **64KB Flash**
- **8K SRAM**
- **Optional additional 512KB SRAM**
- **Optional 1-Wire port**
- **PLL synthesized clocks, 14.3MHz, 8MHz, 200KHz**
- **Freescale MC9S12NE64 core with:**
    - **16-bit bus with 50MHz core clock and 25MHz bus clock**
    - **Debug port**
    - **SPI Port**
    - **2 Asynchronous Serial Ports**
    - **8 channels of 10-bit A/D**
    - **4-channel timer external interface for Input capture/output compare**
    - **16-bit pulse accumulator**

3 Hardware

3.1 Specifications

- **VOLTAGE REQUIREMENTS:** 3.3V
- **CURRENT REQUIREMENTS:** 320mA typical with 25MHz bus clock or 265mA at 16MHz.
- **OPERATING TEMPERATURE:** 0 - 70 degrees Centigrade, humidity range without condensation 0% to 90% RH.
- **DIMENSIONS:** SODIMM form factor with dimensions of 2.66" x 1.50".
- **PROCESSOR:** Freescale MC9S12NE64 microcontroller
- **10/100 Base-T Ethernet with on-chip PHY**
- **FLASH:** 64K
- **SRAM:** 8K
- **Optional additional 512KB SRAM**
- **Optional 1-Wire® Port**
- **Real-Time Clock**
- **I/O:** 144 pin SODIMM connection providing
  - **External Bus Interface**: 20 address x 16 data with 3 chip selects or 24 GPIO in single-chip mode
  - **BDM**: standard "single-wire" background debug module interface
  - **Ethernet:** onboard PHY provides 10/100 base-T Ethernet signals.
  - **SPI**: SPI port with 3 multiplex-able chip selects
  - **Serial Ports**: 2 native and 1 switched serial port or 12 pins of GPIO
  - **A/D:** 8 ADC inputs or 8 digital inputs
  - **External IRQs:** 6 external IRQs or 6 GPIO
  - **Timer/Counters:** 4 input capture/output compare timer pins or 4 GPIO
  - **CLOCKS**: PLL synthesized 8MHz, 200KHz, 14.3MHz clock outputs

3.2 Real-Time Clock/Calendar

The SoM-NE64M provides a DS1305 real-time clock/calendar on-board. The RTC can be battery backed by supplying power to the VSTBY pin.

3.3 External Connections

The SoM-NE64M connects to a carrier board containing its connectors, power supply and any expansion IO, through a standard gold-plated SODIMM 144 pin connection (processor side shown below).

The SoM-NE64M is designed to fit in a standard SODIMM socket on any EMAC 144 pin SODIMM SoM carrier. These connections are designed to be compatible with all EMAC 144 pin SODIMM SoM products.

The remainder of this section describes the pinout as it applies specifically to the SoM-NE64M module.

3.3.1 External Bus

The SoM-NE64M provides a flexible external bus for connecting peripherals. The CPLD of the SoM-100ES connects through a subset of these connections.

SODIMM Pin#	Pin Name	Dir.	CPU Pin	Description
100	GP_CS1	OUT	N/A	General purpose Chip select 1 from the CPLD
98	GP_CS2	OUT	N/A	General purpose Chip select 2 from the CPLD
108	GP_CS3	OUT	N/A	General purpose Chip select 3 from the CPLD
16	~OE	OUT	N/A	Output enable, asserts when the processor is ready for an external device to drive the data bus
83	~WR	OUT	N/A	Write enable, asserts after the processor has output data to the bus and it is has settled. Used when writing to an external device on the data bus
6	~RST_IN	IN	N/A	External reset input to the CPLD processor.
43	~RST_OUT	OUT	N/A	Reset output from the CPLD (which also resets the processor)
44	~EA	OUT	N/A	Not used on the SoM-NE64M
85	~RD/TIP	OUT	R/~W/PE2	Defines data direction on bus transactions[1]
72	ALE/~TS	OUT	PK6/~XCS	Asserted on external bus read/write transactions[1]
26,35,33,31,28,109,111,113,10,12,18,14,37,5,11,9,7,13,97,17,15, 104	A0-A21	OUT	PK0/XA14-PK5/XA19	Address bus. A0–A13 are latched address lines. A14-A19 are from the processor or can be used as GPIO in “normal single-chip mode”. A20-A21 are tied to ground.
29,27,25,22,23,21,19, 20,8,24,34, 70,77,81,84,86	D0-D15	BIDIR	DATA0-DATA15	Data bus from the processor used for word or byte transactions with peripherals or memory, or can be used as GPIO in “normal single-chip mode”.

[1] These pins are not used in most external memory or peripheral applications.

The following list shows the configuration of the external memory map.

Device	Address Range	Description
EXT_SRAM	0x00000 to 0x7FFFF	Optional on-board 512KB SRAM
GP_CS1	0x80000 to 0x8FFFF	External active-low chip select #1
GP_CS2	0x90000 to 0x9FFFF	External active-low chip select #2
GP_CS3	0xA0000 to 0xAFFFF	External active-low chip select #3 (used for selecting peripherals on the SoM-100ES)
SERSLCT	0xB0000 to 0xBFFFF	Writing to any one of the addresses will select which COM port is connected to SCI1. See Serial Ports for more details.

Typically when connecting to external memory or peripherals, ~GP_CSx will connect to the device's ~CE or ~CS pin. For external word-wide devices, typically the device's A0 line will connect to the SoM's A1 line, device's A1 to SoM's A2 and so-on. Byte-wide devices will connect in a conventional manner.

See Boot Options for information on the different operating modes and how they affect the method of accessing external memory.

3.3.2 BDM – Module Specific Interface

The SoM-NE64M brings out the Background Debug Module (BDM) communication line of the processor. This module is implemented in the processor for sophisticated debugging with minimal processor intervention. This debug interface requires an external PC based debug "wiggler/dongle" and PC based debugging software.

As an alternative to using a BDM "wiggler", Freescale has a free firmware-based serial port debugger that works with Codewarrior development and debugging tools. This firmware requires a RUN/~LOAD input (in this case, ~XIRQ/PE0) to select whether on power-up the program will RUN immediately, or LOAD (enable loading the program or debugging).

On the SoM-NE64M, these pins are part of the pins that have been designated "module specific" in the SoM specification.

SODIMM Pin#	Pin Name	CPU Pin	Description
60	MS11	BKGD/MODC	Single-wire Background Debug Module communication
61	MS12	~XIRQ/PE0	For configuring firmware based debugging tools (instead of BDM). Pull this pin to ground to LOAD, or pull to Vcc (or let it float) to RUN. This can also be used as a general purpose input or XIRQ.

3.3.3 1-Wire®

The SoM specification calls for a 1-Wire® port. On the SoM-NE64M this is an optional feature implemented by a DS2482 driven by the MCS9S12NE64's IIC port.

SODIMM Pin#	Pin Name	Description
116	LOCAL1W	1-Wire® network signal

3.3.4 Ethernet

The SoM-NE64M has a 10/100base-T Ethernet PHY built into the processor. Carrier designers need only run these lines through the appropriate magnetics layer to have a functional Ethernet connection.

SODIMM Pin#	Pin Name	CPU Pin	Description
88	LED_TX/ CFG_0	N/A	No connection
89	LED_LINK/ CFG_1	PL0/ACTLED	Ethernet LED indicating an established link with another device or GPIO[1]
90	LED_RX/ CFG_2	PL1/LNKLED	Ethernet LED indicating when data is received by the device or GPIO[1]
94	Ethernet_Rx-	Ethernet_Rx-	Low differential Ethernet receive line
92	Ethernet_Rx+	Ethernet_Rx+	High differential Ethernet receive line
93	Ethernet_Tx-	Ethernet_Tx-	Low differential Ethernet transmit line
91	Ethernet_Tx+	Ethernet_Tx+	High differential Ethernet transmit line

[1] There is no PHY configuration capability via the LED pins as there is in other SoMs.

3.3.5 SPI

The processor provides an SPI module for communicating with peripheral devices. This bus is connected internally to the RTC.

SODIMM Pin#	Pin Name	CPU Pin	Description
122	SPI_MI	SPI_MISO/PS4	SPI serial data in
121	SPI_MO	SPI_MOSI/PS5	SPI serial data out
120	SPI_SCK	SPI_SCK/PS6	SPI serial clock out
123	SPI_CS0	KWJ0/PJ0	SPI device select line 0
124	SPI_CS1	KWJ1/PJ1	SPI device select line 1
110	SPI_CS2	KWJ2/PJ2	SPI device select line 2

3.3.6 Serial Ports

The serial ports in the MCS9S12NE64 have the following features:

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths
- 13-bit baud rate selection
- Programmable 8-bit or 9-bit data format
- Separately enabled transmitter and receiver
- Programmable transmitter output parity
- Two receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
- Interrupt-driven operation with eight flags:
- Transmitter empty
- Transmission complete
  - Receiver full
  - Idle receiver input
  - Receiver overrun
  - Noise error
  - Framing error
  - Parity error

- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection

The SoM specification provides for 3 serial ports, but the MCS9S12NE64 only has 2, so a multiplexing scheme was employed to provide transmit and receive lines for a third port. In this scheme COM1 (SCI0) is always available. By default after reset, COM2 is connected to SCI1 and COM3 is in the inactive state. If a 1 is written to the SERSLCT port (an external memory mapped I/O port within the CPLD), SCI1 is connected to COM3 and COM2 is now in the inactive state. The inactive state behaves the same on both COM2 and COM3 in that the transmit line is held at the UART's typical inactive level and the receive line is ignored. Writing a 0 to the COMSLCT port will restore COM2 and COM3 to their default state again.

Care must be taken not to switch between COM2 and COM3 in the middle of receiving and/or transmitting data otherwise the data could be corrupted. The TC (transmission complete) bit of the SCISR1 register in SCI1 can be monitored to see if a character is currently being transmitted (the TDRE bit is not appropriate to determine this). Likewise, the IDLE bit of the same register can be used to determine if a character is currently being received (the RDRF bit is not appropriate to determine this). If the IDLE bit is used the ILT bit of SCICR1 should be set as appropriate for your application.

There is no direct support in the hardware for automatic handshake line control, so if this is required by your application, it can be simulated in software.

SODIMM Pin#	Pin Name	CPU Pin	Description
71	COM1_RXD	SCI0_RXD/PS0	COM1 receive/GPIO
73	COM1_TXD	SCI0_TXD/PS1	COM1 transmit/GPIO
38	COM2_RXD	SCI1_RXD/PS2[1]	COM2 receive
36	COM2_TXD	SCI1_TXD/PS3[1]	COM2 transmit
82	COM2_RTS/GPIO	KWG0/PG0	COM2 RTS/GPIO
78	COM2_CTS/GPIO	KWG1/PG1	COM2 CTS/GPIO
103	COM3_RXD	SCI1_RXD/PS2[1]	COM3 receive
102	COM3_TXD	SCI1_TXD/PS3[1]	COM3 transmit
107	COM3_DSR/GPIO	KWG5/PG5	COM3 DSR /GPIO
106	COM3_DTR/GPIO	KWG6/PG6	COM3 DTR/GPIO
76	COM3_RI/GPIO	KWG7/PG7	COM3 RING/GPIO
30	COM3_DCD/GPIO	KWG4/PG4	COM3 DCD/GPIO
39	COM3_RTS/GPIO	KWG2/PG2	COM3 RTS/GPIO
79	COM3_CTS/GPIO	KWG3/PG3	COM3 CTS/GPIO

[1] These are not directly connected to the CPU pin but are multiplexed via the CPLD.

3.3.7 GPIO

This section provides for the SoM general purpose IO section. All of the internal ADC ports are brought out here, as well as all of the available IRQs and the timer/counter pins and the clock outputs.

3.3.7.1 Analog to Digital Converter

The 8 channels of the ADC, when using an ADC clock of 2MHZ, are capable of 7 to 14uS conversions at 10-bit resolution or 6 to 13uS at 8-bit resolution.

3.3.7.2 Timer/Counter

The input capture/output compare (IOC) ports can be used for a variety of functions. The input captures can be used to measure input waveforms and at the same time on another port the output compares can be used to output a waveform (PWM). The output compares can also be used for timers.

The pulse accumulator can be used as a 16 bit counter or a timer (independent of the IOC timer). The PT7/IOC7 pin can be configured as the pulse accumulator input for use as a counter input or event timer.

3.3.7.3 Clock Outputs

There are three useful clock frequencies generated by the on-board clock synthesizer which are made available for use on the SoM carrier.

For more information on the ADC and Timer functions of the processor, please refer to the *MC9S12NE64 Data Sheet*.

SODIMM Pin#	Pin Name	Processor Pin	Description
75	IRQ1/GPIO	KWH0/PH0	IRQ 1/GPIO
32	IRQ3/GPIO	KWH1/PH1	IRQ 3/GPIO
40	GPIO0/IRQ4*	KWH2/PH2	IRQ 4/GPIO0
42	GPIO1/IRQ5*	KWH3/PH3	IRQ 5/GPIO1
87	GPIO2/IRQ6*	KWH4/PH4	IRQ 6/GPIO2
80	GPIO3/IRQ7*	KWH5/PH5	IRQ7/GPIO3
125	GPIO4	PT4/IOC4	IOC4 or GPIO4
126	GPIO5	PT5/IOC5	IOC5 or GPIO5
127	GPIO6	PT6/IOC6	IOC6 or GPIO6
128	GPIO7	PT7/IOC7	IOC7, pulse accumulator input or GPIO7
129	GPIO8	PAD0/AN0	Analog or digital input 0
130	GPIO9	PAD1/AN1	Analog or digital input 1
131	GPIO10	PAD2/AN2	Analog or digital input 2
132	GPIO11	PAD3/AN3	Analog or digital input 3
133	GPIO12	PAD4/AN4	Analog or digital input 4
134	GPIO13	PAD5/AN5	Analog or digital input 5
135	GPIO14	PAD6/AN6	Analog or digital input 6
136	GPIO15	PAD7/AN7	Analog or digital input 7
105	~LDAC/GPIO	KWH5/PH5	LDAC control for external DAC, IRQ or GPIO
114	8MHz	8MHz	General purpose 8MHz clock
115	200KHz	200KHz	General purpose 200KHz clock
117	14.3MHz	14.3MHz	General purpose 14.3MHz clock

3.3.8 CAN

CAN is not available on the MC9S12NE64, therefore SODIMM pins 95 and 96 are not connected.

3.3.9 Power

The SoM-NE64M requires a 3.3V power supply to power the on-board circuitry. There are also 2 other optional supply inputs (see table below).

SODIMM Pin#	Pin Name	Description
3,4,141,142	3.3Vcc	3.3V main supply input
1,2,52,53, 58,59, 62,63,68,69, 143,144	GND	Ground
119	VSTBY	Voltage standby: This is an input pin for providing backup voltage to the RTC. The voltage should be in the range of 2.0 to Vcc-0.2 If the RTC is not used in the application, this should be attached to the 3.3V rail.
118	VPULLUP	This is used to provide external 5V power to the optional 1-Wire® interface.

3.3.10 Boot Options

The SoM specification provides two pins for boot time configuration as shown in the table below.

SODIMM Pin#	Pin Name	Description
41	BOOT_OPTION1	This sets the processor mode. If this pin is floating (it has a pull-up to Vcc), it invokes “normal single-chip mode”. If tied to ground, “normal expanded wide mode” is selected.
74	BOOT_OPTION2	This sets the frequency that drives the EXTAL pin of the processor. If this pin is floating (it has a pull-up to Vcc), the frequency is 25MHZ. If tied to ground, the frequency is 16MHZ.

In “normal single-chip mode”, the processor is capable of running at the full 25MHz rated bus clock speed and is able to support 10/100 Base-T Ethernet. In this mode the software must control the address and data bus and related control lines by manipulating the respective port registers (there are C drivers available which perform this).

In “normal expanded wide mode” the MC9S12NE64 is only rated for 16MHz bus clock operation and at that rate can only support 10 Base-T Ethernet. The processor controls the address and data bus and related control lines automatically.

The BOOT_OPTIONx pins have been designed to be moved together to the same potential (i.e. both to ground or both to Vcc) so that the proper operating frequency is chosen for the selected mode.

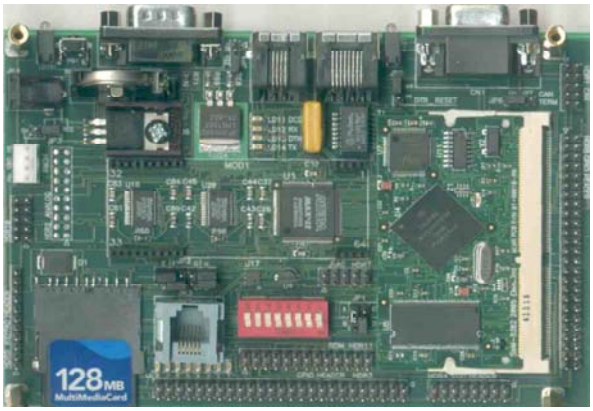
4 Development Tools

4.1 Hardware

4.1.1 SoM-100ES

EMAC provides an off-the-shelf carrier for its SoM modules, the SoM-100ES, which provides power to SoM modules and provides them with an extended range of I/O. This board comes with full schematics and BOM, and can be used as is, or as a reference for a customer’s own design.

http://www.emacinc.com/som/som100es.htm



EMAC also offers a semi-custom engineering service. By modifying an existing design, EMAC can offer quick-turn, low-cost engineering for your specific application.

4.2 Software

The SoM-NE64M offers a wide variety of software support from both open source and proprietary sources.

4.2.1 Eclipse

EMAC provides sample code and drivers for the SoM-NE64M as CDT projects within the free Eclipse IDE. Eclipse is a powerful open-source Java based IDE. It has plug-ins for Java and C, development and debugging, as well as several other languages.

http://www.eclipse.org/

EMAC offers a free download of Eclipse, complete with JDK, the Eclipse CDT plug-in, and the pre-integrated TINI distribution. We also offer the CTD projects standalone, for easy integration with Eclipse for Linux and Mac users.

ftp://SoM:sompublic@ftp.emacinc.com/index.html

4.2.2 Eclipse CDT plug-in

The Eclipse CDT plug-in provides a powerful graphical IDE for C development. This plug-in relies on GNU Make to build its files, so its projects are highly portable to other IDE's. It also offers a MI based debugger, for plugging into the newer gdbs.

http://www.eclipse.org/cdt/

4.2.3 M6811-Elf-Tools

The popular open source gcc compiler has a stable build for the HC11/HC12 family, which can be used for building applications using the **-m68hcs12** flag.
http://gcc.gnu.org/

4.2.4 Codewarrior

Codewarrior offers both an expensive professional, and a Free 32K code-size, Special Edition Development Environment. This Integrated Development Environment (IDE) includes a C compiler and an excellent debugger. The debugger does not require a BDM "wiggler dongle", though it can use one. All that is needed is serial port SCI0.

http://www.metrowerks.com/MW/Develop/Embedded/HC12/Downloads

