REVISION HISTORY :

REVISION	DATE	DESCRIPTION	MOTIVATION	STUFF ADDED/DROPPED/CHANGED	SHEET AFFECTED
4.00.00	09/06/05	ECO37 connect cathode of GPIO high drive directly to port	Allows a wider variety of control	Dropped ZD2 and R1	GPIO
4.00.00	09/07/05	ECO38 Mirror GPIO LED location	previous placement was misleading	Mirrored LD1-LD8	GPIO
4.00.00	09/06/05	ECO39 convert socket modem socket part number to phantom	easier on manufacturing	Attribute change to MOD1	Serial IFs
4.00.00	09/06/05	ECO40 Move lines on schematics to make JP2 options more visable	asthetic change to schematic	JP2 schematic drawing modified	Carrier
4.00.00	09/06/05	ECO41 Add pull-up to MMC/SDIO CD line	CPLD has internal pull-up, but this is more robust and obvious	Added R41	Serial IFs
4.00.00	09/07/05	ECO42 Add BDM translation cable to the rail	Debug support for the NE64, which has a different BDM dimension	Added BDM-Trans sheet	BDM-Trans
4.00.00	09/06/05	ECO43 Drive U3 with 3.3V instead of 5.	Multi-voltage chip. 5V inputs are not officially supported by MMC/SD	Changed VCC net for U3	Carrier/Serial IFs
4.00.00	09/06/05	ECO44 Drive both transformer center taps with filtered 3.3V	Required for NE64 module, doesn't hurt the other 2	Connected NC center tap of ethernet transformer to filtered 3.3V	Ethernet
4.00.00	09/06/05	ECO45 Update title blocks to use automatic PCAD fields	Automation reduces chance of error and saves time	Changed hard coded fields in title blocks to PCAD fields	All
4.00.00	09/08/05	ECO46 Modify Female com port pattern to more accurately reflect part dimen	Components dimensions cause incompatibily with some chassis	Modified component dimensions	PCB
4.00.00	09/12/05	ECO47 Bump LED tree to better fit chassis	LED tree placement caused some problems with standard chassis	moved MMC/PWR LED tree and reset switch slightly	PCB
4.00.00	09/08/05	ECO48 move HDR11 .05" to give extra space to BDM cable	BMD cable came right up to the edge of the module, provides extra clearance	Moved HDR11 .05"	PCB
4.00.00	09/08/05	ECO49 move JP2 away from OW header	hard to insert jumpers	swapped locations of OW IC's and JP2	PCB
4.00.00	09/12/05	Rotate OW header	Asthetic	rotated JK3 180	PCB

REVISION KEY:

PCB REV . SCHEMATIC REV MODWIRE REV

X.XX.XX

PCB1

MISC. PART

BLANK PCB REV 4
01-6601-R4

OPTION KEY:
0 ALWAYS POPULATED
1 AtoD
2 DtoA
5 SD/MMC card
6 CAN
7 AtoD and DtoA shared circuitry, required for options 1 and/or 2 to work.
8 Modem
9 Thermometer
10 GPIO
11 Never populated, legacy part
12 SOM100ESR1 legacy populations, not normally populated
13 Power options - Floppy connector, battery, and LED
14 485/422 components
15 SoM-5282 config. buffer
16 NE64 BDM adaptor

Title	SoM-100ES		
Size C	Number 01-6601-R4		Rev 4.00.00
Date	Tue Sep 13, 2005	Drawn by	Nathan Z. Gustavson
Filename	SoM-100ESR4.00.00_9-13-05.sch	Sheet	1 of 9

JUMPER TABLE

LOCATION	STYLE	FUNCTION	DEFAULT SETTING(S)	QTY OF JUMPERS REQUIRED PER LOCATION
JP1	2 X 3 0.1 INCH	LCD CONFIGURATION	A&D – BACKLIGHT EN	2
JP2	2 X 3 0.1 INCH	CONFIG OPTIONS	E B H D	4
JP3	1 X 3 0.1 INCH	POWER SOURCE 5V/VIN	REG	1
JP4	1 X 3 0.1 INCH	RS–232 / RS–422 /RS–485 SERIALPORT CONFIG	232 – NO JUMPER, This has no park location	1
JP5	1 X 3 0.1 INCH	DTR RESET	ON	1
JP6	1 X 3 0.1 INCH	CAN PORT LINE TERMINATION	ON	1

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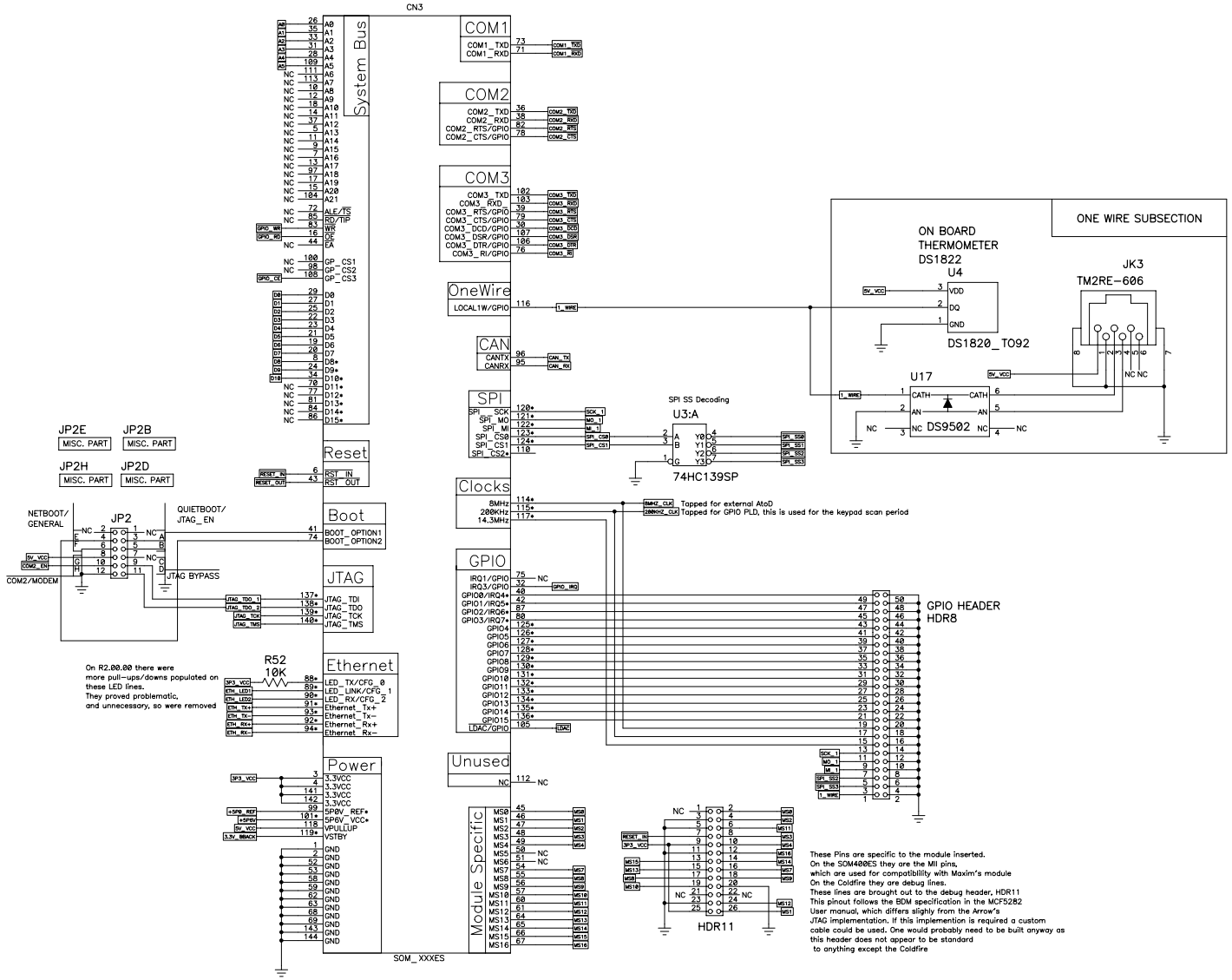

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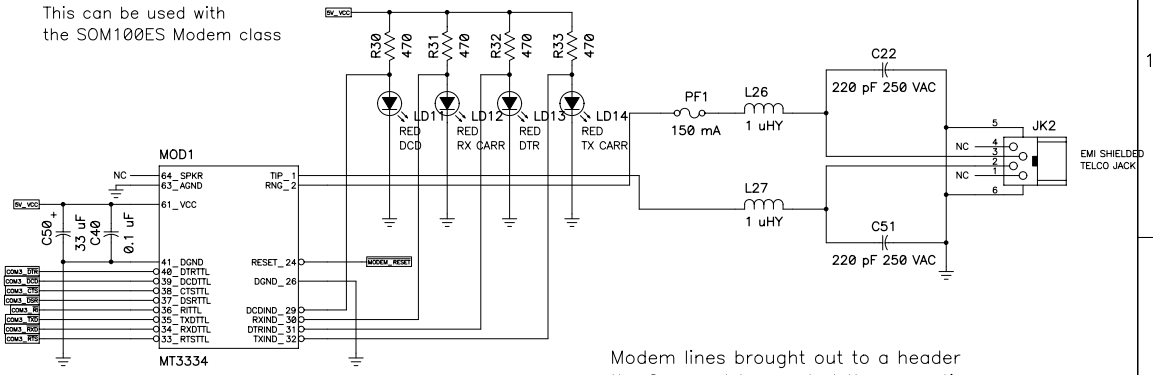
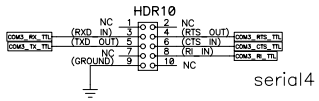
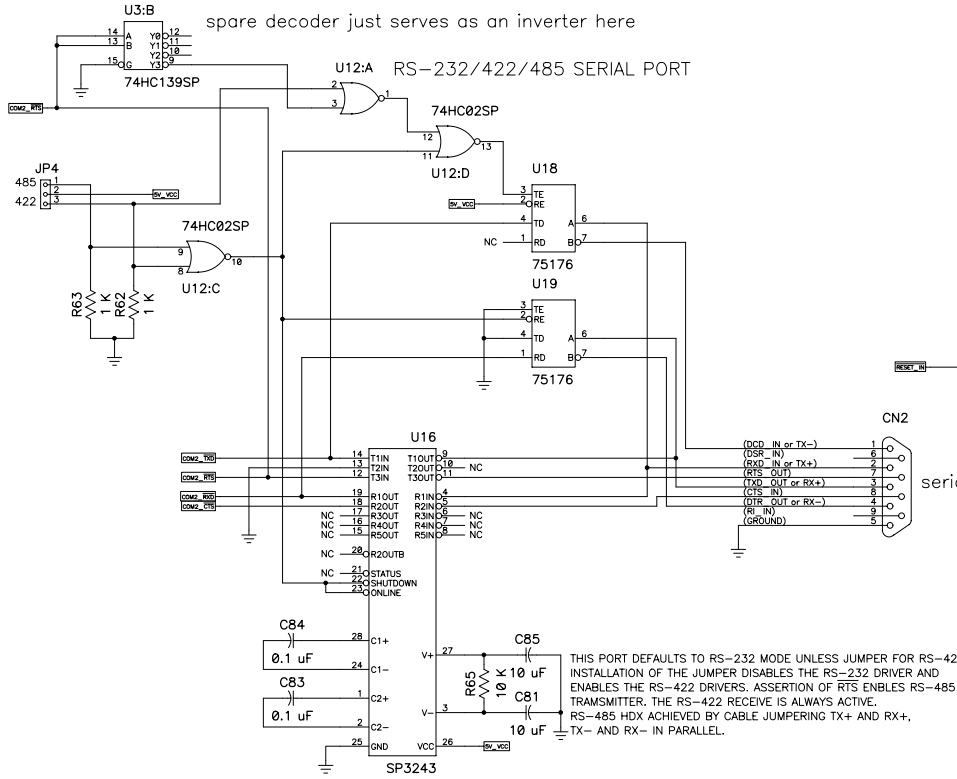
Standard Multitech Modem socket
Compatible with the Multitech 56K modem and Multitech wireless modem.
COM4 in the Tini OS.
This can be used with
the SOM100ES Modem class

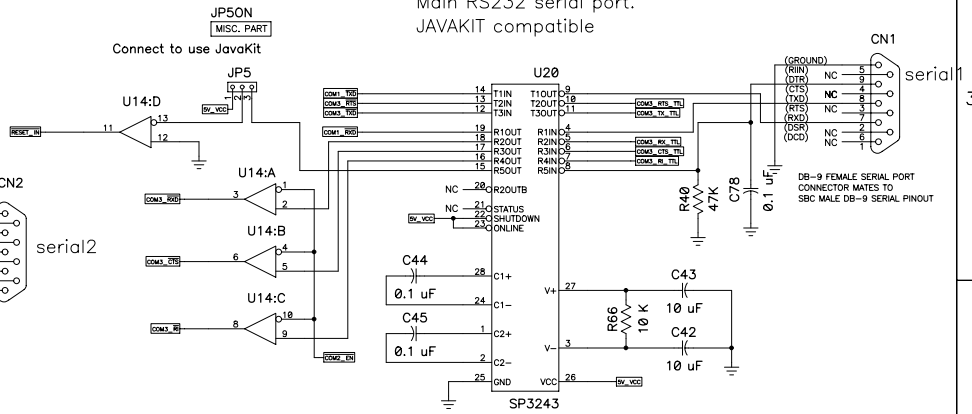


Modem lines brought out to a header
the 2 cannot be used at the same time.
Note that this is serial4 in the TiniOS.
This naming is based on the serial part convention
used by the Tini OS, which skips serial3 for some
reason.





Main RS232 serial port.
JAVAKIT compatible



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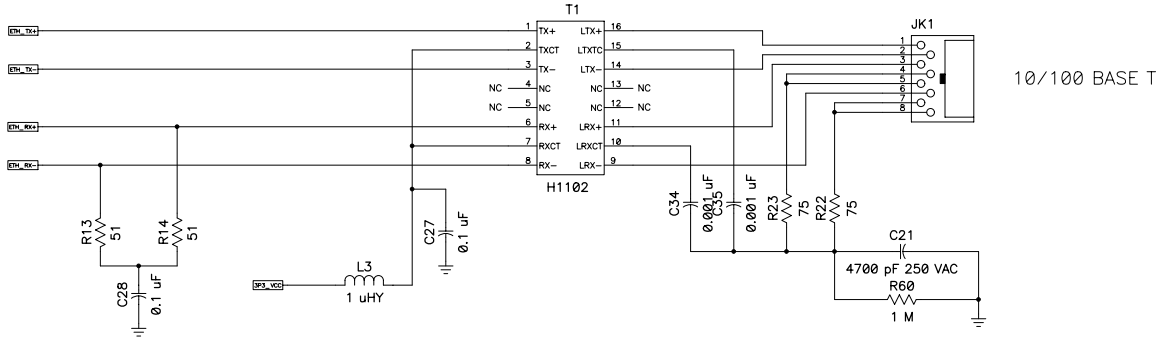
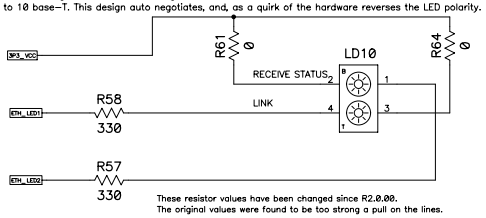


10/100 BASE T

ethernet LED'S and configuration options

new LED polarity – auto-negotiation.
This is changed from the Rev1 design which hard coded the board
to 10 base-T. This design auto negotiates, and, as a quirk of the hardware reverses the LED polarity.



These resistor values have been changed since R2.0.00.
The original values were found to be too strong a pull on the lines.

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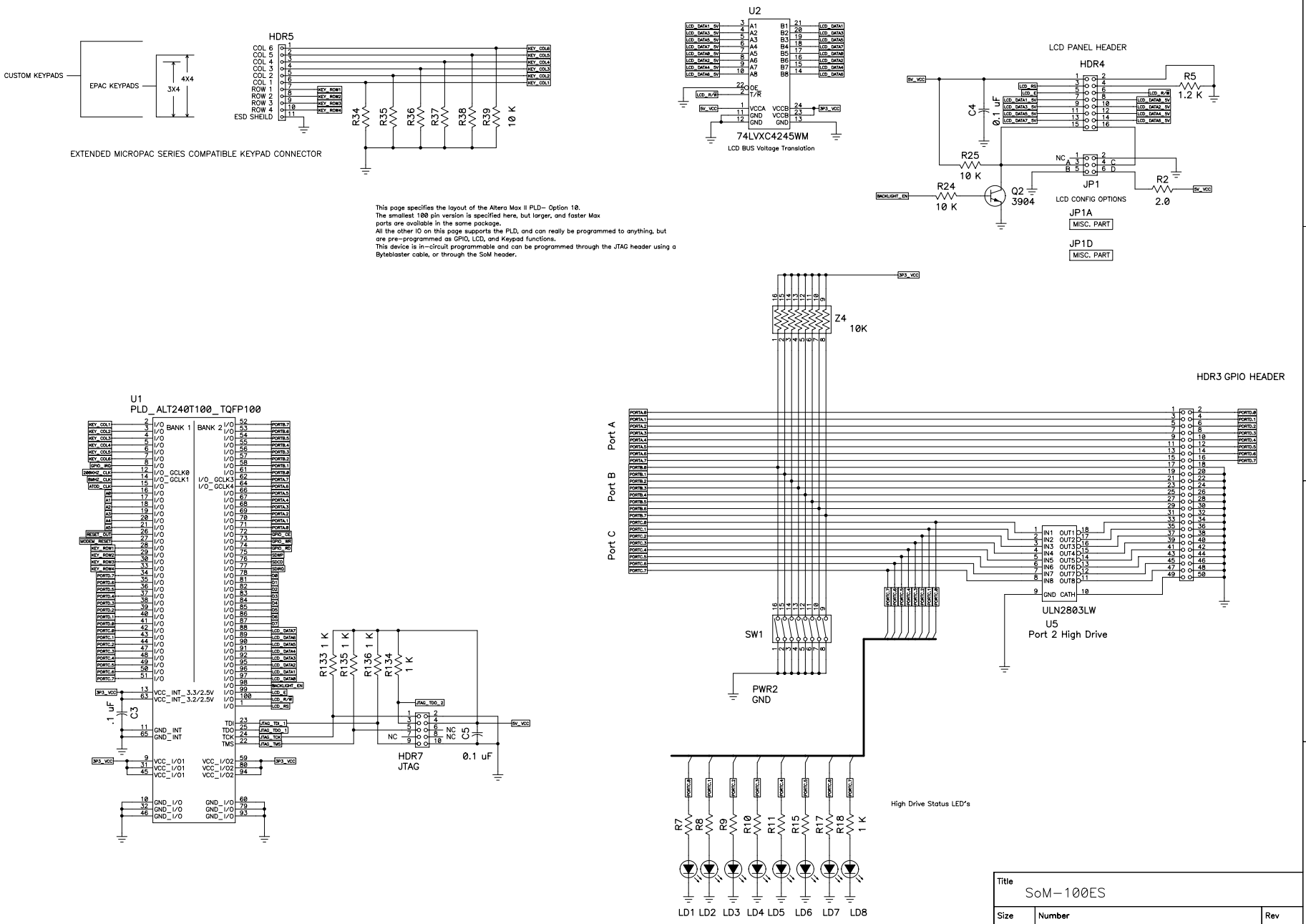

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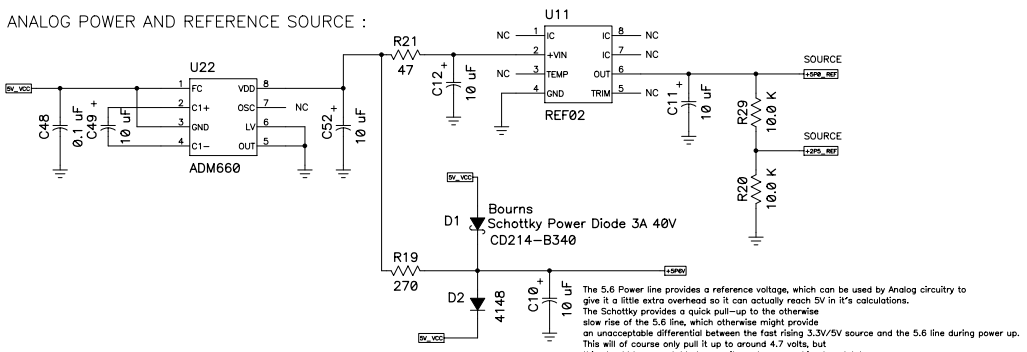
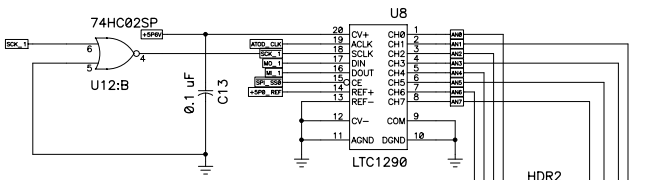
ANALOG POWER AND REFERENCE SOURCE :

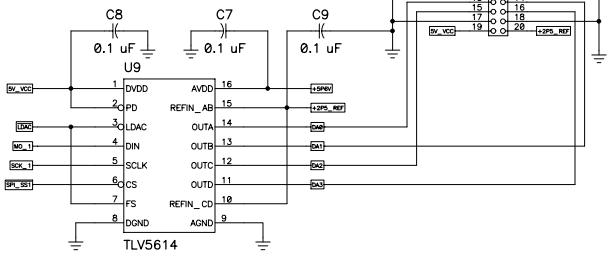


The 5.6 Power line provides a reference voltage, which can be used by Analog circuitry to give it a little extra overhead so it can actually reach 5V in it's calculations.
The Schottky provides a quick pull-up to the otherwise slow rise of the 5.6 line, which otherwise might provide an unacceptable differential between the fast rising 3.3V/5V source and the 5.6 line during power up. This will of course only pull it up to around 4.7 volts, but this should be acceptable to permit most reverse-bias type latch-ups.

OPTIONAL 12 BIT 4 CHAN SERIAL A/D



OPTIONAL 12 BIT 4 CHAN SERIAL D/A



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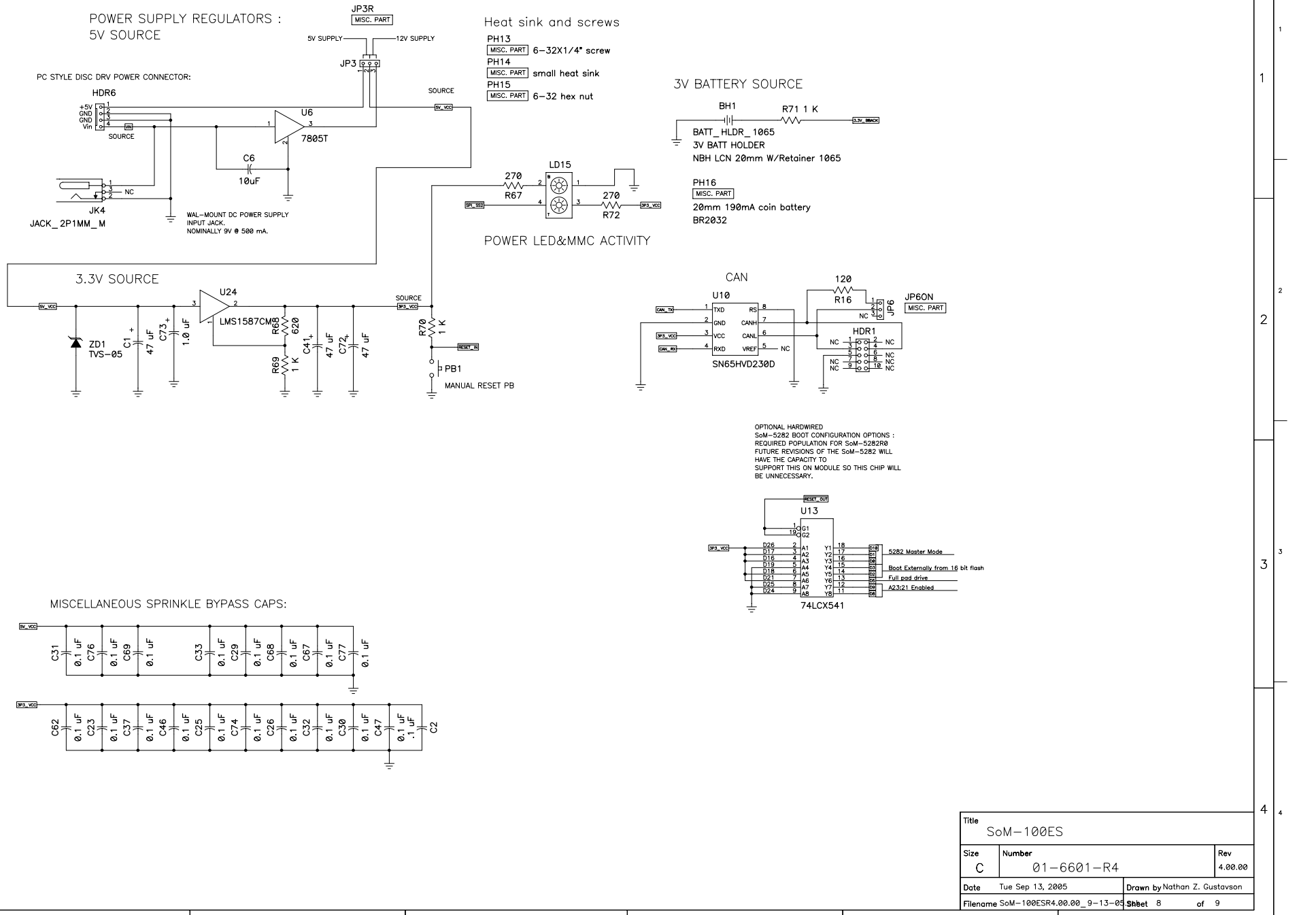

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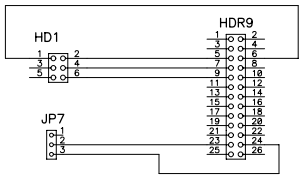

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