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SoM-100ES
Users Manual

For

PCB Revision 2 & 3

Table of Contents

1. Introduction

This document describes EMAC's SoM-100ES (SBC) module. The SoM-100ES is versatile SoM Carrier board ideal for evaluation and early development work. This Carrier is designed to work with all EMAC SODIMM type SoMs.

The SoM-100ES provides access to all the SoM's I/O through on-board connectors as well as a number of additional I/O expansion blocks such as A/D, D/A, Digital I/O, Modem, and MMC flash disk. Full schematics of the SoM-100ES are provided giving the user a solid base with which to design their own SoM Carrier.

Although a good deal of customers will want a Carrier that is unique and is designed specifically for their application, the SoM-100ES, when coupled with a SODIMM SoM makes for a powerful Remote Data Acquisition and Control system with Modem and Ethernet capabilities. This allows the user to gather data and respond with Control commands via the Internet. An Enclosure and Power Supply are available options for the SoM-100ES.

When a unique custom board is required, the amount of design work required is greatly minimized by the SoM approach. The custom Carrier designer does not have to worry about the processor, memory, and standard I/O functions and can concentrate on the I/O and dimensional aspects required for the application.

In situations where a custom Carrier is required, but the customer does not have the capability to design such a board in-house, EMAC's Custom to Order Services (COS) can be utilized. Using COS the customer can select from a library of standard I/O blocks. These blocks can be put together quickly into a form-factor of the customer's choosing, providing prototypes in as little as 30 days.

1.1. SoM Benefits:

- Faster time to market
- Cost savings
- Reduced risk
- Scalable CPU choices
- Decreased customer design requirements
- Small footprint

1.2. Features

- **Small, Half EBX form factor (4.0" x 5.75")**
- **10/100 BaseT Ethernet with on-board Magnetics and RJ45**
- **2 serial RS232 ports and 1 RS232/422/485 port (ports must also be supported by the SoM)**
- **32 PLD controlled General Purpose digital I/O lines in addition to any SoM I/O lines**
- **8 digital lines with dipswitch provision**
- **8 High Drive digital output lines (500 ma. sink) with status LED's**
- **24 key, keypad interface**
- **Character LCD interface**
- **Battery for nonvolatile RAM and Real Time Clock**
- **MMC/SD Flash Card Socket**
- **CAN port**
- **Dallas standard 1-Wire access port with on-board Temperature Sensor**
- **Mulititech Socket Modem socket supporting 56K, 56K fax, and wireless modems.**
- **System Reset button**

1.3. Options

ON-BOARD OPTIONS

- **ANALOG:** Analog I/O Upgrade Includes:
- 8 channel 12-bit A/D
- 4 channel 12-bit D/A

1.4. Other Options

- **MBPC- 200 Enclosure:** This MicroBox metal chassis is an ideal housing for the SoM-100ES and SoM.
- **PS-50A Power Supply:** A 50 watt switching power supply that has an AC input of 100 to 240 volts and DC outputs of +5 volts and +12 volts. The PS-50A is especially designed to operate with the MBPC-200 MicroBox chassis.
- **Wall-Mount Power Supply:** An inexpensive 9 Volt DC supply capable of 500 ma. of current.

2. Hardware

2.1. Specifications

- **VOLTAGE REQUIREMENTS:** Onboard regulation allows 5 volt or 7.5 - 15 volt DC board input voltage.
- **CURRENT REQUIREMENTS:** 300 ma. @ 5 Volts Typical including SoM.
- **OPERATING TEMPERATURE:** 0 - 70 degrees Centigrade, humidity range without condensation 0% to 90% RH.
- **DIMENSIONS:** Half EBX form factor with dimensions of 4.0" x 5.75".
- **DIGITAL I/O:** 8 general purpose digital pins, 8 digital pins with dipswitch provision and 5V pull-ups, 8 digital pins with 5V pull-ups, 8 open collector High-Drive Digital outputs with 500 ma. sink drive capability, status LEDs, and a maximum total I/O drive of 1500 ma. for these 8 lines. All Digital I/O lines terminate to standard 50 pin, I/O Rack compatible header connectors.
- **OPTIONAL ANALOG INPUTS:** 8 analog inputs are multiplexed into a single 12-bit A/D converter with Sample & Hold. The analog input voltage range for each channel is 0 - 5 Volts.
- **OPTIONAL ANALOG OUTPUTS:** 4 analog outputs implemented using a 4 channel, 12-bit D/A. The analog output voltage range for each output is 0 - 5 Volts with a drive capability of 5 mA.

2.2. Jumpers

This section describes the Jumpers and Jumper Blocks of the SoM-100ES.

2.2.1. JP1

LCD Configuration. LCD configuration jumpers. These Jumpers allow for different types of LCDs and backlight control.

Jumpers	B&D	backlight always on
Jumpers	A&D	port line control (BACKLIGHT_EN) of backlight through software
Jumper A&C	allows the use of certain graphic LCDs	

2.2.2. JP2

Configuration Options

A.

B. These jumpers are SoM dependent and are used to configure the SoM modules. Refer to the SoM manual for further details on these jumpers.

C. JTAG Bypass off – connects the JTAG daisy chain to the module when inserted.

D. JTAG Bypass on – allows the PLD to be programmed when no module is inserted.

E.
F. These jumpers are SoM dependent and are used to configure the SoM modules. Refer to the SoM manual for further details on these jumpers.

G. Modem Enable – This connects the third COM port to the modem socket.
H. Modem Disable – This connects the third com port to HDR10 as a standard EMAC IDC to DB9 male

2.2.3. JP3

Input Voltage This jumper allows the selection of the input voltage used to power the board. With the jumper in the 5V position the regulator is bypassed directly feeding 5 Volts DC from the power connector HDR6 pin labeled 5V to the board. With the jumper in the REG position the regulator is now in place allowing 7 – 15 DC Volts from the power connector pin, or barrel jack to power the board.

2.2.4. JP4

485/422 This jumper determines which interface Serial COM 1 Port utilizes. Place the jumper in the 485 position for use as an RS/485 port and place the jumper in the 422 position for use as a RS 422 interface. Remove the jumper (default) for RS/232.

2.2.5. JP5

DTR Reset. Place a jumper in the ON position to connect the DTR line from the first serial port to the Reset-In line.
This is required to be compatible with the DS-400EM's Javakit serial program.

2.2.6. JP6

CAN Term. Place a jumper in the ON position to terminate the CAN bus.

2.3. JTAG Header

This multipurpose header provides an in-circuit programming interface to the Max II CPLD that resides on the SoM-100ES as well as any PLD or Debug port on the SoM itself. This header can be used to reprogram the onboard CPLD and any other CPLDs detected on the chain (on the module). This requires an interface cable, such as the ByteBlasterMV. Several models are available from P&E Microcomputer Systems http://www.pemicro.com/. Also more inexpensive versions and open schematics can be obtained via the Internet, i.e. http://www.cmosexod.com/.

Table 1: JTAG Header (HDR10)

Pin	Signal	Pin	Signal
1	JTAG_TCK	2	GND
3	JTAG_TDO	4	5V (Vcc)(Sourced)
5	JTAG_TMS	6	NC/Reserved
7	NC/Reserved	8	NC/Reserved
9	JTAG_TDI	10	GND

2.4. Module Based IO

The Module I/O connector, HDR8 is made up primarily of direct connections from the modules SODIMM connector. This 50-pin connector consists of grounds on one side allowing 25 signals on the other side and maintaining compatibility with standard 50 pin, I/O Rack compatible header connectors. The only signals that do not directly come from the module are the Slave Selects, which are decoded from the first 2 SPI slave selects of the module.

Table 2: SoM I/O Connector (HDR8)

Pin	SODIMM Pin	Pin	Signal
1	(One Wire)116	2	GND
3	(SPI Slave Select 3)	4	GND
5	(SPI Slave Select 2)	6	GND
7	(SPI MISI) 122	8	GND
9	(SPI MOSI) 121	10	GND
11	(SPI CLK) 120	12	GND
13	(14.3 MHZ CLK) 117	14	GND
15	(200 KHZ CLK) 115	16	GND
17	(8 MHZ CLK) 114	18	GND
19	(GPIO 15) 136	20	GND
21	(GPIO 14) 135	22	GND
23	(GPIO 13) 134	24	GND
25	(GPIO 12) 133	26	GND
27	(GPIO 11) 132	28	GND
29	(GPIO 10) 131	30	GND
31	(GPIO 9) 130	32	GND
33	(GPIO 8) 129	34	GND
35	(GPIO 7) 128	36	GND
37	(GPIO 6) 127	38	GND
39	(GPIO 5) 126	40	GND
41	(GPIO 4) 125	42	GND
43	(GPIO 3/IRQ7) 80	44	GND
45	(GPIO 2/IRQ6) 87	46	GND
47	(GPIO 1/IRQ5) 42	48	GND
49	(GPIO 0/IRQ4) 40	50	GND

2.5. CPLD Based General Purpose Digital I/O

The SoM-100ESR2 provides 53 general-purpose 3.3V IO pins connected to headers of the SoM-100ES. These pins are controlled by an Altera Max II device, which is an in-circuit programmable instant on, CPLD. By default this is the EPM240T100C5 model, which provides 240 internal logic elements, but it is pin-compatible with some larger devices. This CPLD provides powerful reconfigurable combinational and sequential logic, for an almost unlimited number of applications. Through Altera's free Quartus II environment this device can be easily reconfigured as digital IO, counters, uarts, spi, even flash and RAM! The CPLD interfaces through the address/data bus of the carrier, and has access to clocks and an IRQ for advanced control logic. When the SoM-100ES is built, it is pre-loaded with a configuration that it stores in its internal flash, and instantly loads on power-up. This configuration uses the pins in a specific manner, which is described in the rest of this section, but could be easily reprogrammed to be something else. EMAC provides free drivers and development software for interfacing with the standard configuration.

2.5.1. Legacy

The SoM-100ES used an older Altera PLD, the 3064. This device was much less dense, so only provided a subset of the current functionality. The new memory map requires minimal software changes, however, for software compatibility reasons, a configuration compatible with the old software is available upon request.

2.5.2. General purpose digital ports

The default program creates 4 digital ports, Ports A, B, C, and D.
These ports are all bit configurable as input/output ports and default to input on reset. If programmed as inputs the input lines should not exceed 5 V dc and if programmed as outputs, these lines are capable of driving 25 mA. loads. The open collector high drive output port PC0 – PC7 has drive 500 mA. sink drive capability and a maximum total I/O drive of 1500 ma. The PLD has it input capabilities on these 8 lines for modularity reasons, but they are not useable as such in the actual system. PD0-PD7 is located on the GND side of the I/O rack connection, so if a standard I/O rack is used, these pins should be left as inputs.

Table 3: CPLD Based Digital I/O Connector (HDR3)

Pin	Signal	Pin	Signal
1	PA0(3.3V)	2	PD0(3.3V)
3	PA1(3.3V)	4	PD1(3.3V)
5	PA2(3.3V)	6	PD2(3.3V)
7	PA3(3.3V)	8	PD3(3.3V)
9	PA4(3.3V)	10	PD4(3.3V)
11	PA5(3.3V)	12	PD5(3.3V)
13	PA6(3.3V)	14	PD6(3.3V)
15	PA7(3.3V)	16	PD7(3.3V)
17	PB0(3.3V)	18	GND
19	PB1(3.3V)	20	GND
21	PB2(3.3V)	22	GND
23	PB3(3.3V)	24	GND
25	PB4(3.3V)	26	GND
27	PB5(3.3V)	28	GND
29	PB6(3.3V)	30	GND
31	PB7(3.3V)	32	GND
33	PC0(High D)	34	GND
35	PC1(High D)	36	GND
37	PC2(High D)	38	GND
39	PC3(High D)	40	GND
41	PC4(High D)	42	GND
43	PC5(High D)	44	GND
45	PC6(High D)	46	GND
47	PC7(High D)	48	GND
49	5V(Vcc)	50	GND

2.5.3. Memory Map

The SoM-100ES's PLD is connected to the SoM's processor data bus and uses SODIMM pin 108 as its select line. The Base Address of the PLD is SoM dependent.
For the EMAC SoM-400EM it is mapped to CS4, which gives it a base address of 0x800000.

See the manual that accompanied the SoM for further details. Additional PLD registers exist. See the Keypad and LCD section for details on these PLD registers.

Within the PLD are several registers that are referenced as offsets from the PLD Base address. They are defined as follows:

Table 4: Default CPLD Memory Map

Pin	Register	Description
0	PortA Data	Digital State
1	PortA Configuration	Input/Output Mapping
2	PortB Data	Digital State
3	PortB Configuration	Input/Output Mapping
4	PortC Data	Digital State
5	PortC Configuration	Input/Output Mapping
6	PortD Data	Digital State
7	PortD Configuration	Input/Output Mapping
8	Keypad Register	Read Keypad Data
9	LCD Data	Read/Write LCD data bus
10	LCD Control	Set LCD control lines
11	SD Data	Read Extended SD lines

Descriptions

Port Data Registers

The bits of these ports are mapped to the data lines of the physical ports. Writing to these bits latches a Vcc or GND value (1 or zero respectively) to the appropriate pin. Pins are mapped according to their respective positions on the header, i.e. PB4 has its value latched by the 4th bit of the PortB configuration register.
Latching a bit will result in a voltage change at the pin if the pin is configured to be an output with the corresponding configuration register bit.
Reading from this address will return the current state (1 or zero for Vcc or GND) of the pin.

Port Configuration Registers

This port is bitwise mapped to the configuration of the ports. Setting a bit to 1 sets the corresponding pin to an output, Setting a bit to 0, sets it as an input, ex. Setting the PorB configuration register to 0x10 would set PB4 to be an output and place its current latched state (see the Data Register description) on the pin.

Keypad Register

Reading this register returns the last value latched from the keypad. The high nibble is the row; the low nibble is the column. The keypad sets its interrupt line when a button is pressed and releases it when data is read from this register.

LCD Data Register

This is used to latch data to the LCD data bus. This latched data is always present except during a read cycle. Which must be manually implemented from software (EMAC provides software for this) through the control lines.

LCD Control Register

This register latches the state of the control lines.
Bit 0 – RS control – 1 sets RS, high 0 sets RS low
Bit 1 – RW control – 1 sets RW, high 0 sets RW low
Bit 2 – Backlight control – 1 for on, 2 for off, when in software control mode.

SD Data Register

Reading this register returns the state of the optional SD card pins.
Bit 0 – SD IRQ state.
Bit 1 – SD CS state.
Bit 2 – SD WP state.

2.5.4. Other CPLD Functions

The CPLD also provides the 4MHz clock for the optional Analog Channels.
This is obtained by dividing its input 8MHz clock by 2.

The CPLD also controls the Modem Reset line, which is currently tied to the modules reset_out line.

2.6. Analog Channels

The SoM-100ES optionally provides a 12-bit, 8 channel A/D. In addition to the A/D, the SoM-100ES optionally provides 4 D/A channels with 12-bit resolution. These optional converters communicate with the processor through the on-board SPI. The A/D input channel accepts 0 – 5 Volt inputs. The D/A channels provide 0 – 5 Volt outputs with a drive capability of 5 mA. In order to access the optional 12-bit A/D (LTC1290) and D/A (TLV5614) communication must take place using the SoM's SPI port. The A/D uses SPI select 0 and the D/A uses SPI select 1.

Table 5:Analog I/O (HDR2)

Pin	Signal	Pin	Signal
1	GND	2	GND
3	ANI00	4	ANI01
5	ANI02	6	ANI03
7	ANI04	8	ANI05
9	ANI06	10	ANI07
11	GND	12	GND
13	ANO00	14	ANO01
15	ANO02	16	ANO03
17	ANI07	18	GND
19	VCC +5VDC	20	Vref +2.5VDC

2.7. Serial Ports

2.7.1. RS 232 SERIAL 0 UART

The SoM-100ES provides one dedicated RS232 UART Serial 0 which has software configurable baud rates. No handshake Lines are available for use on this port. The DTR line of the port is connected to modules reset_in line, when jumper JP5 is enabled. (default position ON). This Reset connection is used by Javakit in conjunction with the SoM-400EM module.

Table 6: Serial Port 0 (CN1)

Pin	DB9 Description
1	NC
2	TxD
3	RxD
4	reset_in (Jumperable)
5	GND
6	NC
7	NC
8	NC
9	NC

2.7.2. RS 232/422/485 SERIAL 1 UART

The SoM-100ES provides one jumper (JP4 selectable RS 232/422/485 Serial Port which has software configurable baud rates. This jumper determines which interface Serial 1 (COM 2) Port utilizes. Place the jumper in the 485 position for use as an RS/485 port and place the jumper in the 422 position for use as a RS 422 interface. Remove the jumper (default) for RS/232. RS232 Handshake Lines are implemented by the use of SODIMM pins 78 and 82. When using this serial port in the RS485 mode, the Handshake Line implemented through the use of SODIMM pin 82 controls the transmitter enable line of the RS485 driver.

Table 7: Serial Port 1 (CN2)

Pin	DB9 Description
1	RS422/485 TX-
2	RS232 RXD or 422/485 TX+
3	RS232 TXD or 422/485 RX+
4	RS422/485 RX-
5	GND
6	NC
7	RTS (82)
8	CTS (78)
9	NC

2.7.3. RS 232/Modem SERIAL 2 UART

The SoM-100ES provides one jumper selectable RS 232/Modem Serial Port which has software configurable baud rates. This jumper JP2, is used to select how COM3 (Serial 2) gets utilized. Set the jumper to position H for RS232 access through HDR10. A serial cable is provided to allow standard DB9 terminations. Setting JP2 to position G routes this serial port to the socket modem socket. Tables 8 and 9 outline these connections.

Table 8: Serial Port 2 (HDR10)

Pin	Signal	DB9 Description
1	NC	-
2	NC	RxD (103)
3	RxD (103)	TxD (102)
4	RTS (39)	-
5	TxD (102)	GND
6	CTS (79)	-
7	NC	RTS (39)
8	RI (76)	CTS (79)
9	GND	RI (76)
10	NC	-

The Socket Modem socket (MOD1) is designed to accept the standard Multitech SocketModem, as well as the new Multitech SocketModem GSM/GPRS for wireless capability.

Table 9: Socket Modem Socket (Mod 1) Implemented Pins

Pin	Signal	Description
1	Tip	phone signal(JK2)
2	Ring	phone ring (JK2)
24	Reset	modem reset(CPLD)
26	GND	GND
29	DCDIND	DCD LED control(LD11)
30	RXIND	RX LED control(LD12)
31	DTRIND	DTR LED control(LD13)
32	TXIND	TX LED control(LD14)
33	RTS	RS232 RTS(39)
34	RXD	RS232 RXD(103)
35	TXD	RS232 TXD(102)
36	RI	RS232 RI(76)
37	DSR	RS232 DSR(107)
38	CTS	RS232 CTS(79)
39	DCD	RS232 DCD(30)
40	DTR	RS232 DTR(106)
41	GND	GND
61	VCC	5V
63	GND	GND

2.8. CAN I/O

The SoM-100ES provides a single CAN bus channel. Jumpering JP6 to ON, enables the terminating resistor for end of network termination.

Table 10: CAN (HDR1)

Pin	Signal	DB9 Description
1	NC	-
2	NC	CANL
3	CANL	GND
4	CANH	-
5	GND	-
6	NC	-
7	NC	CANH
8	NC	-
9	NC	-
10	NC	

2.9. LCD

The LCD interface currently supports 2 and 4 line character LCDs and some graphic LCDs.
The LCD is connected to the SoM-100ES's on-board CPLD. EMAC provides software for controlling the LCD in its development packages. For low-level information on how to interface with the CPLD default program see:
Section 2.5 CPLD Based General Purpose Digital I/O.

Table 11: LCD Interface (HD4)

Pin	Signal	Pin	Signal
1	VCC	2	GND
3	RS	4	CNTR
5	E	6	R/W*
7	D1	8	D0
9	D3	10	D2
11	D5	12	D4
13	D7	14	D6
15	K (JP1 Pin3)	16	A (JP1 Pin4)

2.10. Keypad

This header provides an interface for a 4x4, 4x5, or 4x6 matrix Keypad. These row and column scan lines are directly connected to the SoM-100ES's on-board CPLD When scanning the keypad Columns are connected to output lines and the rows are connected to input lines.

Table 12: KEYPAD (HDR7)

Pin	Signal
1	COL6
2	COL5
3	COL4
4	COL3
5	COL2
6	COL1
7	ROW1
8	ROW2
9	ROW 3
10	ROW 4
11	ESD SHIELD

2.11. Multi-Media/Secure Digital Card Socket

The SoM-100ES provides standard 5638 type socket, which accepts SD, MMC, and SDIO cards. This Socket is connected to the processor's SPI bus and uses the SPI mode provided by both SD and MMC standards. Pins 8-11 provide the expanded optional connections added by the Secure Digital standard, they are connected to the CPLD for flexibility.

Table 13: MMC Socket (SOK2)

Pin	Signal
1	Slave Select 2
2	MOSI
3	GND
4	3.3V
5	SCK
6	GND
7	MISI
8	IRQ–>CPLD
9	NC
10	Carrier Detect->PLD
11	Write Protect–>CPLD
12	GND

3. Software

The SoM-100ESR2 is programmable via a selection of free software tools and open source EMAC software.

3.1. Eclipse SoM-100ES-SDK

EMAC provides its codebase as a project within the free Eclipse IDE. Eclipse is a powerful open-source Java based IDE. It has plug-ins for Java and C, development and debugging, as well as several other languages.
http://www.eclipse.org/

EMAC offers a free download of Eclipse 3.0, complete with JDK 1.4.2 and the pre-integrated Tini distribution up to 1.14 for the Win32 environment.
We also offer the project standalone, for easy integration with Eclipse for Linux and Mac users.
ftp://SoM:sompublic@ftp.emacinc.com/index.html

This project currently contains Java classes and native libraries for controlling all the IO of the SoM-100ES using a SoM-100EM module.
It will also contain C code and drivers for the new SoM-5282EM, which will run in a real time uCLinux environment.

3.2. Quartus II Web Edition

Altera offers powerful free tools for programming the Max II plus PLD of the SoM-100ESR2.
These tools include free and flexible modules for implementing uarts, I2C, counters, RAM, Flash, etc….
https://www.altera.com/support/software/download/altera_design/quartus_we/dnl-quartus_we.jsp