PROGRAMMABLE 32 LINE PARALLEL I/O BOARD MANUAL

Manual Revision 3.1

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INTRODUCTION

The programmable 32 Line Parallel I/O Board adds four 8-bit I/O ports to an EPAC, MicroPac, or Training System. One of the 8 bit ports is dedicated as as output port while the other three ports can be configured as input or output ports and one of these three ports can be split further as 4 input lines and 4 output lines. The board is a plug-on accessory utilizing the 8255 Programmable Peripheral Interface I.C. (PPI), with outside world terminations via two 50 pin, OPTO I/O rack compatible, male header connectors. Connection to the system is through a 50 pin ribbon cable (included). The board's terminations are all direct (unbuffered) TTL logic levels. The dimensions are 5 1/4" by 3 5/8".

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Introduction:

EMAC's Programmable 32 Line Parallel I/O Board (abbreviated from here on as 32IO) is a peripheral expansion utility board used to provide more direct TTL level digital I/O capability for the EPAC line of single-board computer (SBC) products.

The following descriptions apply to the revision 3 artwork board only. Past and future revisions may operate differently. The board may be identified by the PCB markings at the top end, left side of the PCB as one holds it, so the text printing is right side up. The EMAC assembly is P/N E-030-8, and the PCB part number is 01-0125 REV 3.

The board utilizes a multi-purpose PCB, that may serve other applications, depending on the component population, so it may appear that some of the components are missing. The board has been populated and tested for the 32IO function.

Dimensions:

The 32IO card measures approximately 3 and 5/8 inches wide by 5 and 3/8 inches long, and 1/2 inches thick, accounting for the tallest components on the board. It may be bolted, with plastic standoff hardware, directly onto any of the EPAC SBCs, since they all provide a similar mounting footprint to connect to the card.

When mounting the card on a chassis, the mounting hole spacing is a square cornered rectangle, with centers of 3.30 inches, by 5.00 inches. Allow at least a 1/2 inch center to center spacing between mounting hole centers when mounting several boards adjacent to each other. Details of the board layout and dimensions may be found in the illustrations.

Power consumption:

The 32IO is all CMOS in construction, except for the power supply regulator. The majority of power supply current will be due to the quiescent current of the regulator itself, not the circuitry! With no external loads connected to the board, it will consume approximately 10 mA. of current. The board draws unregulated raw power from the expansion bus.

Interfacing:

DIGITAL I/O

The 32IO provides four 8 bit digital I/O ports. The inputs and outputs are all TTL level compatible with each output capable of driving 2 standard TTL loads. The four ports are split into two 50 pin ribbon headers, CN2 and CN3, which have identical pin footprints. Each connector is wired to directly connect to 16 position OPTO-22 [tm] digital I/O module racks.

In the OPTO-22 connector format used, all even numbered pins (2-50) are ground, pins 1 and 49 are 5 volts Vcc, and the 16 TTL I/O signals are on the odd numbered pins from 17 to 47. The odd numbered pins from 3 to 15 are not connected.

If you are connecting to an OPTO-22 board, care should be taken to select the jumper option on the board, so that Vcc on the rack is isolated from Vcc on the 32IO card. The 32IO card should not be expected to supply power to the OPTO-22, nor should the OPTO-22 power the 32IO card. The regulator on the EMAC card is not sized to deliver operational power to other units, and power back fed from other sources will disrupt power supply and reset sequencing on the EMAC products. The 32IO's Vcc pins are only for use in special applications where low power CMOS sub peripherals are to be powered locally by parallel board power.

Header connector CN2 is connected to port B and C of the 82C55 CMOS PPI chip. These ports may be set to input or output, and port C may be split as well, providing several combinations of input and outputs. Header connector CN3 is connected to port

A of the 82C55 and to a separate octal latch. Although port A can be set for either input or output, the latch port, called port D, is output only. Refer to the I/O port pinouts and/or schematics for more details.

EPAC BUS INTERFACE

Header connector CN1, which is also a 50 pin ribbon header, connects to the EPAC digital I/O bus. There are several types of EPAC SBCs, and some have differing bus types. The 32IO card accepts all types of EMAC SBCs made to date. These include the EPAC 3000, 3000G2. and the UNIVERSAL TRAINER and PRIMER training systems It may be used with the MICROPAC series also, but it will not allow them to function as super low power units anymore, as the regulator on the parallel card cannot be turned on and off.

The 32IO card has an address comparator, and when the DIP switch selected addresses, qualified by EXTIO*, match those present on the expansion bus, I/O transactions between the SBC and the I/O ports on the Parallel board occur.

Software control:

Next to the DIP switch are silkscreen markings for A4,A5,A6,A7. When using the 32IO with the EPAC/MicroPac products, this should typically be set to A4 OFF, and A5,A6,A7 ON which will set the board address to E0h On the MicroPac 180, EPAC 3000 and 3000 G2 the 32IO may be accessed by I/O addresses 1E0 through 1E7 hex. On the other boards, including the PRIMER and UNIVERSAL TRAINER, the I/O addresses are E0 to E7. In the descriptions that follow, the latter I/O addresses will be used, so for the MicroPac 180, EPAC 3000 and 3000 G2 merely add 100 hex to these to get the correct I/O. Other base addresses can be defined by using different DIP switch settings, but they might conflict with I/O addresses on EMAC products.

The 82C55 PPI chip is mapped in at I/O address E0 through E3 hex. The four I/O addresses correspond to digital ports A, B, C, and an internal 82C55 configuration port, respectively. These ports are all write/readable but I/O address E4 (referred to as port D) is write only. Addresses E5 through E7 are reserved, and unused at this time, but data written to them will appear in the D port as if it were written to address E4.

The 82C55 PPI must be initialized in most applications. Upon power on or hardware reset, all three ports within the PPI will be set to read data only. An I/O read from addresses E0 hex will retrieve the bit pattern input to the A port of the PPI. Likewise, I/O reads from E1 or E2 will retrieve the bits at ports B and C. When it is desired to make one or all the ports an output port, configuration code must be written to the PPI control register at I/O address E3 hex.

The INTEL(R) data books go into more detail about the codes written to the PPI control register to set the port directions. In most applications, simple, MODE 0 I/O transactions are supported, the more advanced configurations are not directly supportable. As a simple example, writing an 80 hex to the control register (address E3) will set PPI ports A, B, and C all to outputs. Data written to those port addresses will latch into the port pins, and the output will appear on the header connector pins. Also you may examine the data that was last written to an output port by reading the port.

Port D of the board is a simple octal output latch. This latch is write only, and requires no initialization. It cannot be read back, or used as an input port. Upon power up or hardware reset, all outputs are low (0). They can not be tri-stated, either. If you need to read back the data in the D port, it is suggested that you create a D port driver in software, that keeps a copy of the D port data in a memory variable, whenever data is written to port D. When you need to read what was last written to the D port, simply retrieve the variable from memory. Be sure to always use the driver so that all writes will leave a current copy of the D port data in memory.

Below is an example 8085 assembly language program which configures the PPI so that port A is an input port and ports B and C are output ports. The program reads the data that is input to port A and outputs it to ports B, C and D.

```
porta   equ     0e0h
portb   equ     0e1h
portc   equ     0e2h
pcntl   equ     0e3h    ;control word address
portd   equ     0e4h    ;data latch
start   equ     8000h   ;This is the starting address  of the program (it can be anything)

        org     start
        mvi     a,90h   ;configure PPI for mode 0 with port A as input and B & C as output
        out     pcntl   ;write the control word
loop:   in      porta   ;get data from port A...
        out     portb   ;...and write it to ports B, C and D
        out     portc
        out     portd
        jmp     loop    ;read port A again
```

When using the 8255 in basic I/O mode, the bits written to PCNTL should be as follows

bit 7 1
bit 6 0
bit 5 0
bit 4 direction of port A
bit 3 direction of pc4-pc7 (upper half of port C)
bit 2 0
bit 1 direction of port B
bit 0 direction of pc0-pc3 (lower half of port C)

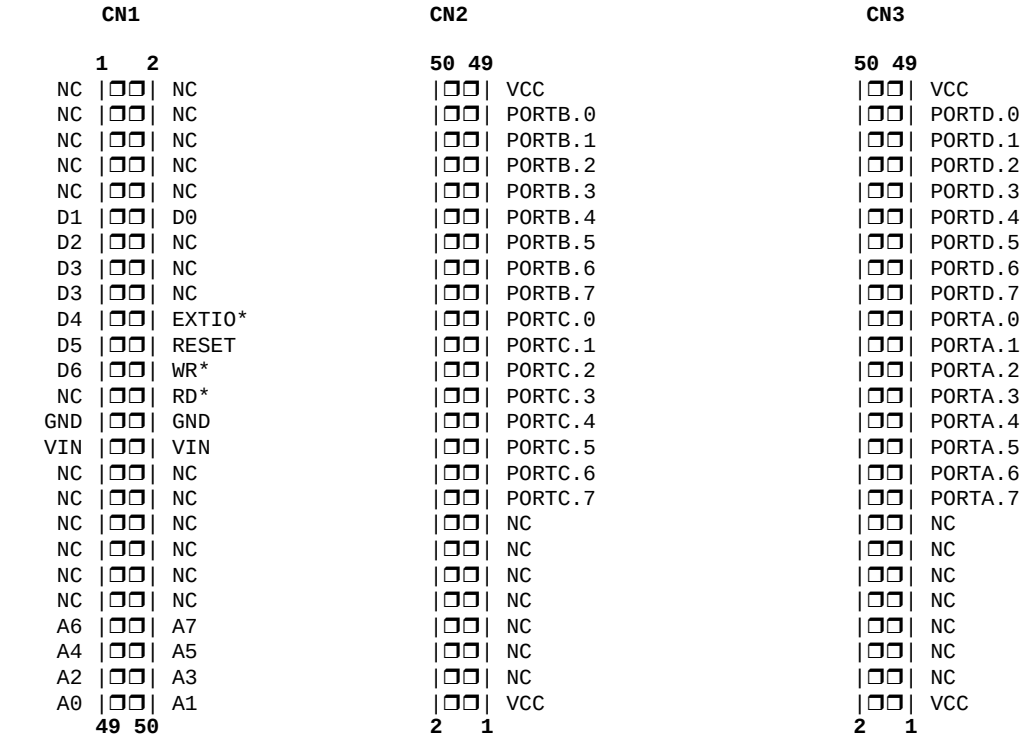
For bits controlling direction, a 1 makes it an input and 0 makes it an output.

Notes:

1. Remember that the PPI must be initialized if port A, B, or C need to be output ports.

2. 82C55 PPI has a bug in it which is not clearly alluded to in the INTEL(R) data books. Whenever ANY port is configured to output, the other ports within that PPI (including the port being configured) that are already configured as outputs, will be reset to zero! So, for example, if port B is already set to output, with a C3 hex sitting there, and you decide to change port A from input to output the data at port B will be wiped out to 00 hex at the same time that port A is reconfigured. Port B will need to be re-written to restore its previous data. Load control relays connected to such a port will chatter when or if this should happen, so plan carefully what port drives what loads, or group them to ports that will not require configuration during normal operation.

CONNECTOR DESCRIPTIONS



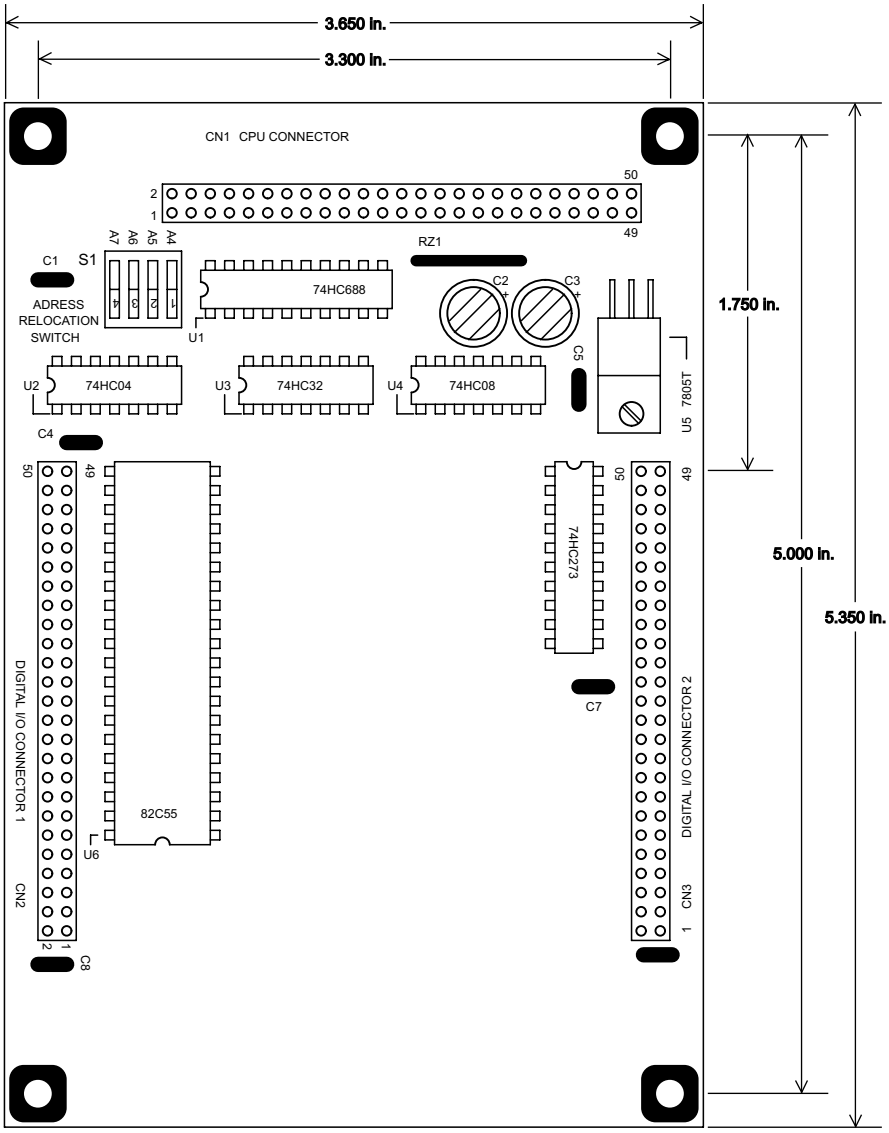
Label definitions:

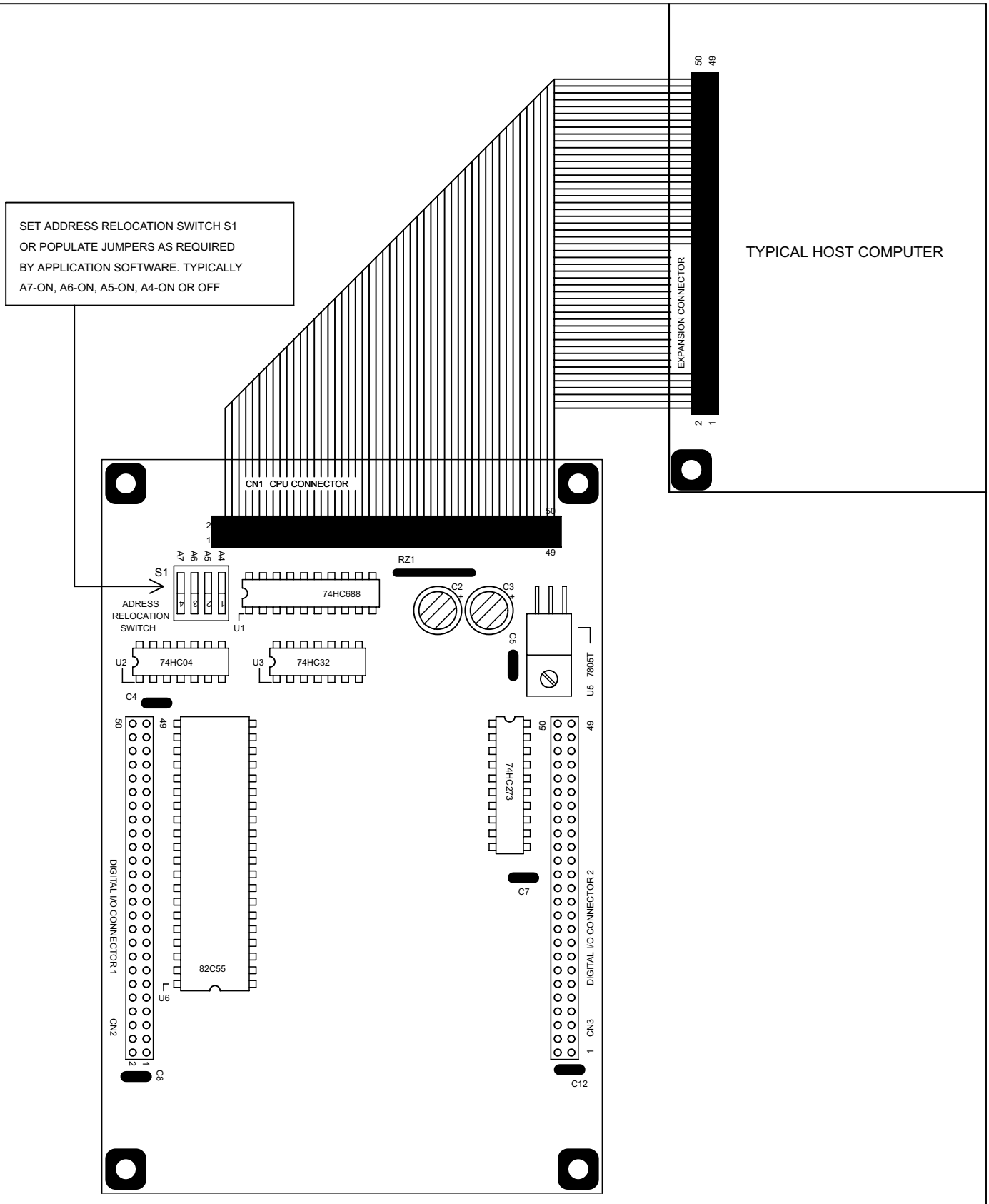
NC - no connect
D0-D7 - data bus lines from host SBC
EXTIO* - active low chip select from host SBC (single board computer)
RESET - active high reset signal from host SBC
WR* - active low write signal from host SBC
RD* - active low read signal from host SBC
GND - ground
Vin - unregulated positive DC supply from host SBC
A0-A7 - address lines from host SBC
PORTA.
PORTB,
PORTC - user definable I/O lines
PORTD - output only lines

NOTE: All even numbered pins on CN2 and CN3 are ground.

APPENDIX A
MECHANICAL DRAWINGS

PARALLEL EXPANSION PORT CARD
LAYOUT AND MOUNTING DIMENSIONS

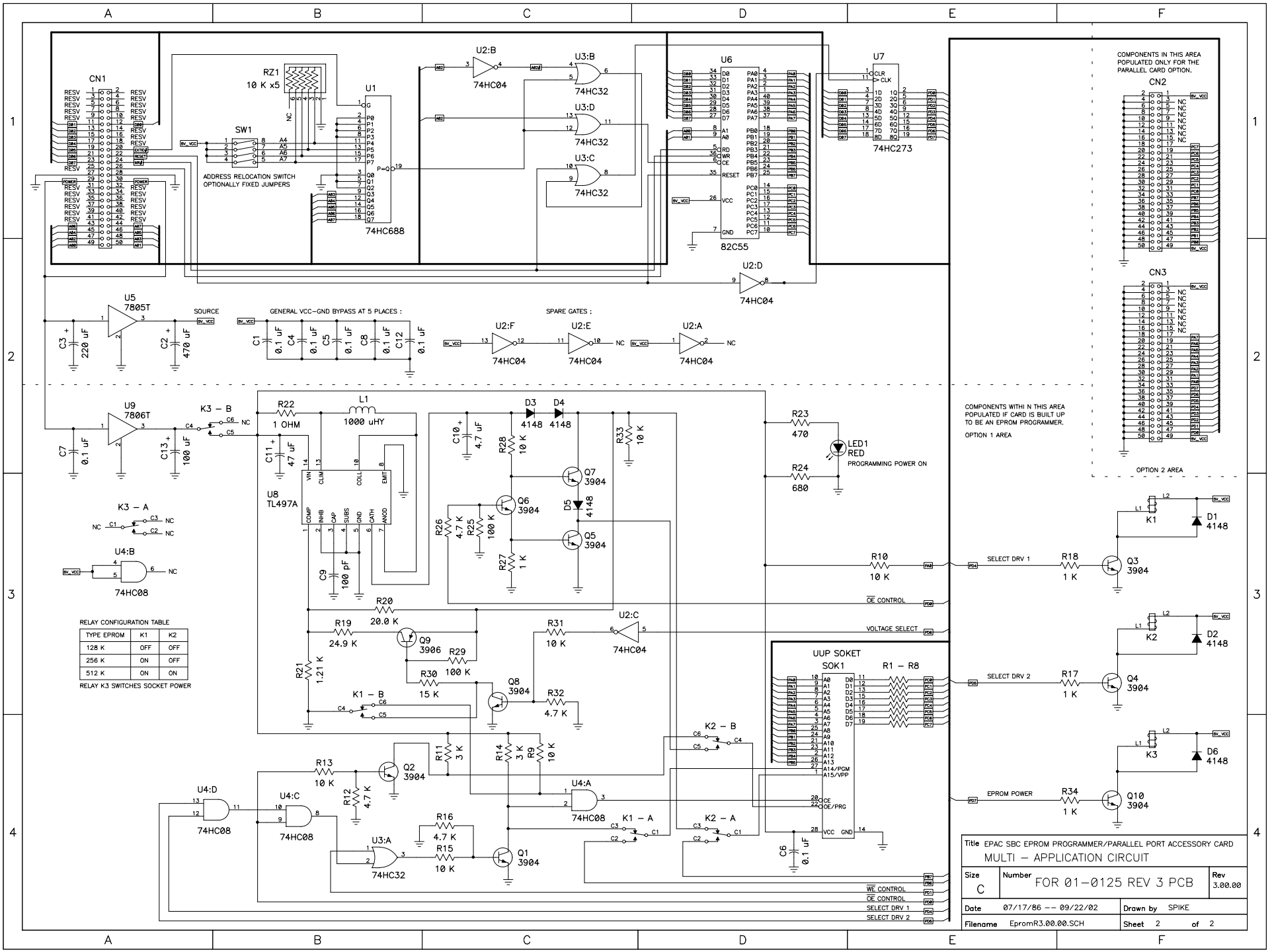




FILE : PAR3ILL.PCN
ATTR : ROTOFF
SCALE : 1 : 1

APPENDIX B

SCHEMATICS


CN1
RZ1
10 K x5
SW1
ADDRESS RELOCATION SWITCH
OPTIONALLY FIXED JUMPERS
U1
74HC688
U2:B
74HC04
U3:B
74HC32
U3:D
74HC32
U3:C
74HC32
U6
82C55
U7
74HC273
U2:D
74HC04
U5
7805T
SOURCE
GENERAL VCC-GND BYPASS AT 5 PLACES :
SPARE GATES :
U2:F
74HC04
U2:E
74HC04
U2:A
74HC04
U9
7806T
K3 - B
R22
1 OHM
L1
1000 uHY
D3
4148
D4
4148
U8
TL497A
R23
470
LED1
RED
PROGRAMMING POWER ON
R24
680
Q7
3904
Q6
3904
Q5
3904
D5
4148
R28
10 K
R33
10 K
R26
4.7 K
R25
100 K
R27
1 K
R10
10 K
OE CONTROL
VOLTAGE SELECT
R20
20.0 K
R19
24.9 K
Q9
3906
R29
100 K
R30
15 K
R31
10 K
U2:C
74HC04
R21
1.21 K
Q8
3904
R32
4.7 K
K1 - B
K2 - B
K1 - A
K2 - A
UUP SOKET
SOK1
R1 - R8
R13
10 K
Q2
3904
R11
3 K
R14
3 K
R9
10 K
R12
4.7 K
U4:D
74HC08
U4:C
74HC08
U4:A
74HC08
R16
4.7 K
U3:A
74HC32
R15
10 K
Q1
3904
C6
0.1 uF
WE CONTROL
OE CONTROL
SELECT DRV 1
SELECT DRV 2
COMPONENTS IN THIS AREA POPULATED ONLY FOR THE PARALLEL CARD OPTION.
CN2
CN3
OPTION 2 AREA
COMPONENTS WITHI N THIS AREA POPULATED IF CARD IS BUILT UP TO BE AN EPROM PROGRAMMER.
OPTION 1 AREA
SELECT DRV 1
R18
1 K
Q3
3904
K1
D1
4148
SELECT DRV 2
R17
1 K
Q4
3904
K2
D2
4148
EPROM POWER
R34
1 K
Q10
3904
K3
D6
4148
RELAY CONFIGURATION TABLE
TYPE EPROM | K1 | K2
128 K | OFF | OFF
256 K | ON | OFF
512 K | ON | ON
RELAY K3 SWITCHES SOCKET POWER
Title EPAC SBC EPROM PROGRAMMER/PARALLEL PORT ACCESSORY CARD
MULTI - APPLICATION CIRCUIT
Size C
Number FOR 01-0125 REV 3 PCB
Rev 3.00.00
Date 07/17/86 -- 09/22/02
Drawn by SPIKE
Filename EpromR3.00.00.SCH
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