FAIRCHILD SEMICONDUCTOR™

April 1998

MM74HC08
Quad 2-Input AND Gate

General Description

These AND gates utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. The HC08 has buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 7 ns (t_{PHL}), 12 ns (t_{PLH})
- Fanout of 10 LS-TTL loads
- Quiescent power consumption: 2 µA maximum at room temperature
- Low input current: 1 µA maximum

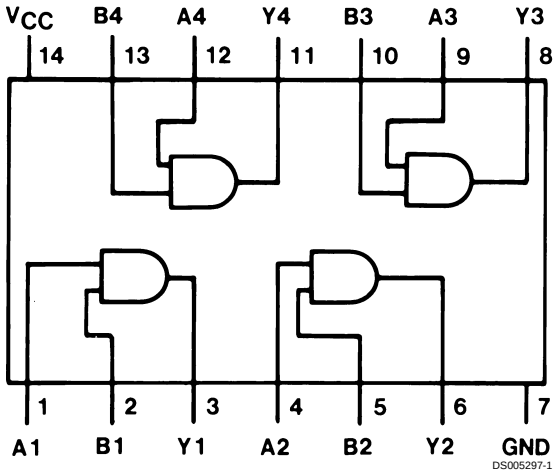
Ordering Code

Commercial	Package Number	Package Description
MM74HC08N	N14A	14-Lead Molded Dual-In-Line (0.300″ Wide)
MM74HC08M (Note 1)	M14A	14-Lead Molded Small Outline (0.150″ Wide), JEDEC
MM74HC08MTC (Note 1)	MTC14	14-Lead Molded Thin Shrink Small Outline Package, JEDEC
MM74HC08SJ (Note 1)	M14D	14-Lead Molded Small Outline, EIAJ

Note 1: Devices also available in 13″ Tape and Reel, Use suffix MX, SJX, and MTCX

Connection Diagram

Pin Assignment for DIP, SOIC and TSSOP



Top View
Order Number MM74HC08

Absolute Maximum Ratings (Notes 3, 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65˚C to +150˚C
Power Dissipation (P_D)	
(Note 4)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L)	
(Soldering 10 seconds)	260˚C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)	−40	+85	˚C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	V_{CC}	T_A=25˚C	T_A=−40 to 85˚C	T_A=−40 to 125˚C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage (Note 6)		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} $\|I_{OUT}\|$≤20 µA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} $\|I_{OUT}\|$≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 µA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 µA	6.0V		2.0	20	40	µA

Note 2: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 3: Unless otherwise specified all voltages are referenced to ground.

Note 4: Power Dissipation temperature derating — plastic "N" package: −12 mW/˚C from 65˚C to 85˚C.

Note 5: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

Note 6: V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics

V_{CC}=5V, T_A=25˚C, C_L=15 pF, t_r=t_f=6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}	Maximum Propagation Delay, Output High to Low		12	20	ns
t_{PLH}	Maximum Propagation Delay, Output Low to High		7	15	ns

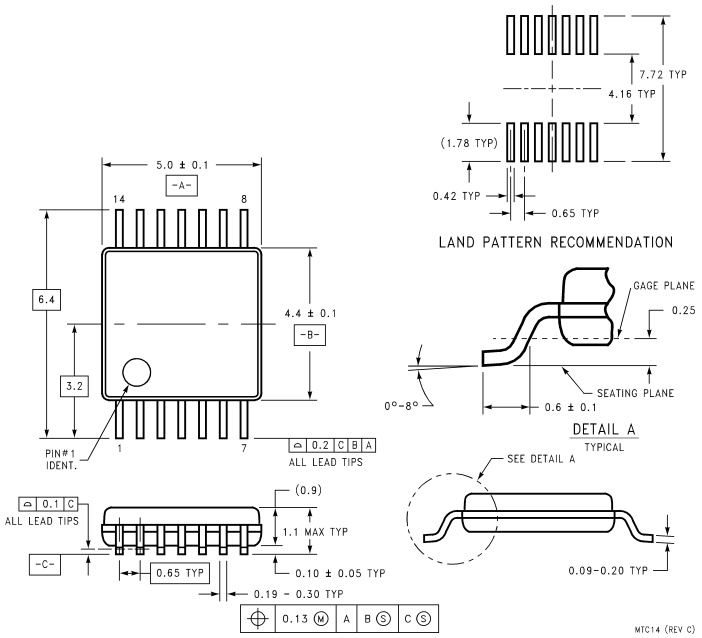
AC Electrical Characteristics

V_{CC}=2.0V to 6.0V, C_L=50 pF, t_r=t_f=6 ns (unless otherwise specified)

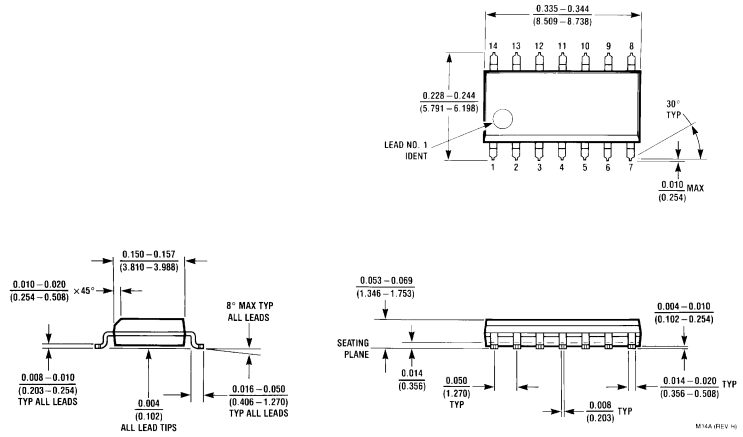
Symbol	Parameter	Conditions	V_{CC}	T_A=25˚C		T_A=−40 to 125˚C	Units
				Typ	Guaranteed Limits		
t_{PHL}	Maximum Propagation Delay, Output High to Low		2.0V	77	121	175	ns
			4.5V	15	24	35	ns
			6.0V	13	20	30	ns
t_{PLH}	Maximum Propagation Delay, Output Low to High		2.0V	30	90	134	ns
			4.5V	10	18	27	ns
			6.0V	8	15	23	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	110	ns
			4.5V	8	15	22	ns
			6.0V	7	13	19	ns
C_{PD}	Power Dissipation Capacitance (Note 7)	(per gate)		38			pF
C_{IN}	Maximum Input Capacitance			4	10	10	pF

Note 7: C_{PD} determines the no load dynamic power consumption, P_D=C_{PD} V_{CC}^2 f+I_{CC} V_{CC}, and the no load dynamic current consumption, I_S=C_{PD} V_{CC} f+I_{CC}.

Physical Dimensions inches (millimeters) unless otherwise noted

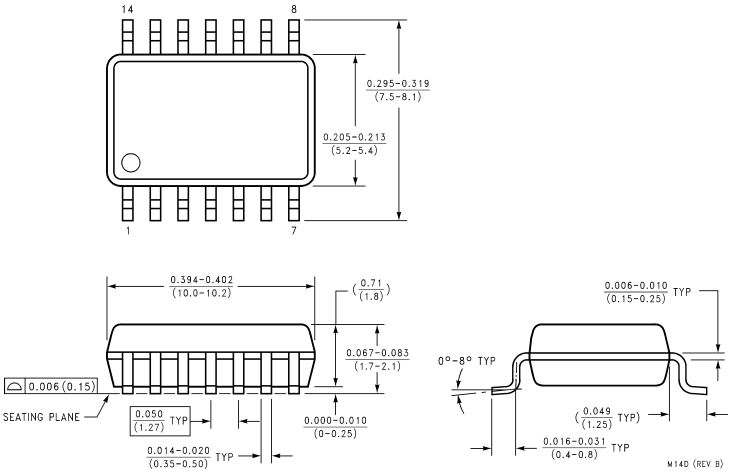


14-Lead Molded Thin Shrink Small Outline Package, JEDEC
Order Number MM74HC08MTC
Package MTC14

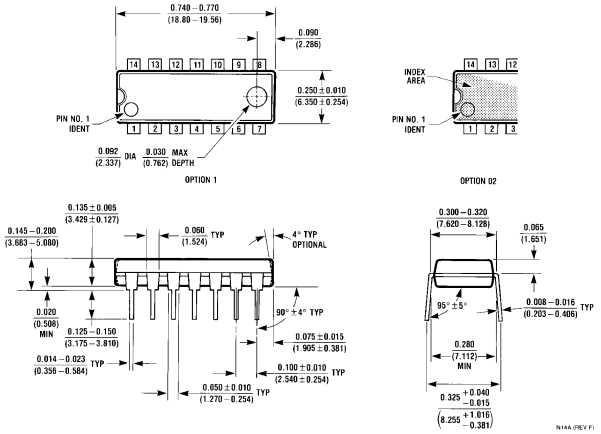


14-Lead Molded Small Outline (0.150” Wide) JEDEC
Order Number MM74HC08M
Package M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Molded Small Outline, EIAJ
Order Number MM74HC08SJ
Package M14D



14-Lead Molded Dual-In-Line (0.300" Wide)
Order Number MM74HC08N
Package N14A

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