

### FEATURES

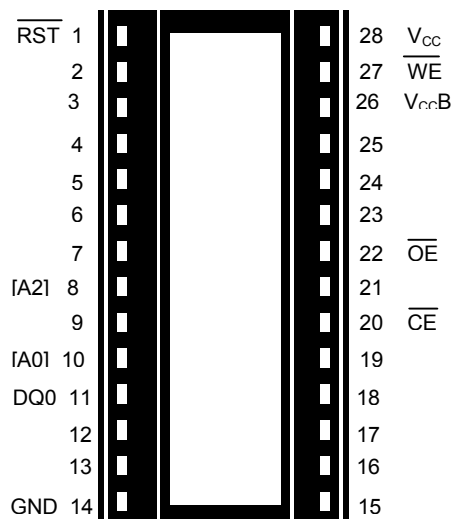
- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Converts standard 2k x 8 up to 512k x 8 CMOS static RAMs into nonvolatile memory
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month; leap-year compensation valid up to 2100
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Proven gas-tight socket contacts
- Full  $\pm 10\%$  operating range
- Operating temperature range:  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$
- Accuracy is better than  $\pm 1$  minute/month @  $+25^{\circ}\text{C}$

### ORDERING INFORMATION

DS1216B, DS1216C, DS1216D, DS1216E, DS1216F, DS1216H (See Figure 2 for letter suffix marking identification.)

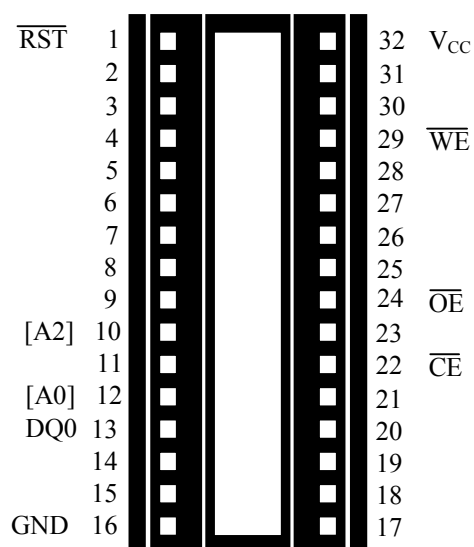
### PIN DESCRIPTION

- $\overline{\text{RST}}$  - RESET
- DQ0 - Data Input/Output 0 [RAM]
- A2 - Address Bit 2 (Read/Write [ROM])
- A0 - Address Bit 0 (Data Input [ROM])
- GND - Ground
- $\overline{\text{CE}}$  - Conditioned Chip Enable
- $\overline{\text{OE}}$  - Output Enable
- $\overline{\text{WE}}$  - Write Enable
- $V_{\text{CC}}$  - Switched  $V_{\text{CC}}$  for 28-/32-Pin RAM
- $V_{\text{CCB}}$  - Switched  $V_{\text{CC}}$  for 24-Pin RAM
- $V_{\text{CCD}}$  - Switched  $V_{\text{CC}}$  for 28-Ppin RAM



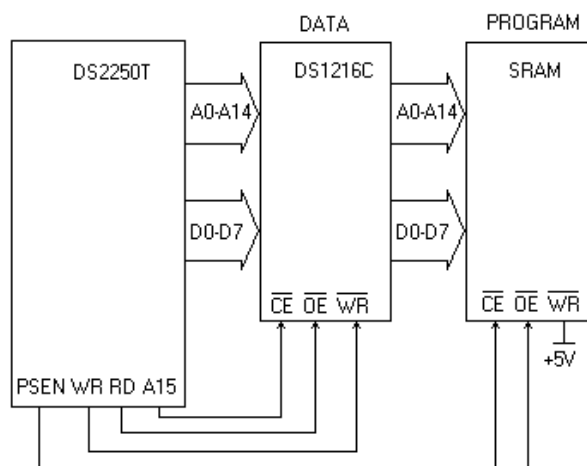
DS1216B/C/D/E  
28-Pin Intelligent Socket

PART	RAM/ROM	RAM DENSITY	PCB MODIFICATION REQUIRED FOR DENSITY UPGRADE?
DS1216B	RAM	16k/64k	No/Yes
DS1216C	RAM	64k/256k	No
DS1216D	RAM	256k/1M	No/Yes
DS1216E	ROM	64k/256k	No
DS1216F	ROM	64k/256k/1M	No
DS1216H	RAM	1M/4M	No



DS1216D/E/F/H  
32-Pin Intelligent Socket

## TYPICAL OPERATING CIRCUIT



## DESCRIPTION

The DS1216 SmartWatch RAM and SmartWatch ROM Sockets are 600mil-wide DIP sockets with a built-in CMOS watch function, an NV RAM controller circuit, and an embedded lithium energy source. The sockets provide an NV RAM solution for memory sized from 2k x 8 to 512k x 8 with package sizes from 26 pins to 32 pins. When a socket is mated with a CMOS SRAM, it provides a complete solution to problems associated with memory volatility and uses a common energy source to maintain time and date. The SmartWatch ROM sockets use the embedded lithium source to maintain the time and date only. A key feature of the SmartWatch is that the watch function remains transparent to the RAM. The SmartWatch monitors  $V_{CC}$  for an out-of-tolerance condition. When such a condition occurs, an internal lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent loss of watch and RAM data.

Using the SmartWatch saves PC board space since the combination of SmartWatch and the mated RAM take up no more area than the memory alone. The SmartWatch uses the  $V_{CC}$ , data I/O 0,  $\overline{CE}$ ,  $\overline{OE}$ , and  $\overline{WE}$  for RAM and watch control. All other pins are passed straight through to the socket receptacle.

The SmartWatch provides timekeeping information including hundredths of seconds, seconds, minutes, hours, days, date, months, and years. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including correction for leap years. The SmartWatch operates in either 24-hour or 12-hour format with an AM/PM indicator.

## OPERATION

Communication with the SmartWatch RAM is established by pattern recognition on a serial bit stream of 64 bits that must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. On the SmartWatch ROM, communication with the clock is established using A2 and A0, and either OE or CE. All accesses that occur prior to recognition of the 64-bit pattern are directed to memory.

After the pattern match, the next 64 reads and/or writes are directed to the clock, and the RAM is disabled. Once the pattern is established, the next 64 read/write cycles will be directed to the RTC registers. When power is cycled, 64 reads should be executed prior to any writes to ensure that the RTC registers are not written. A pattern match is ignored if the RST bit is zero and the RST pin goes low during the match sequence. A pattern match is also terminated if a read occurs during the 64-bit match sequence.

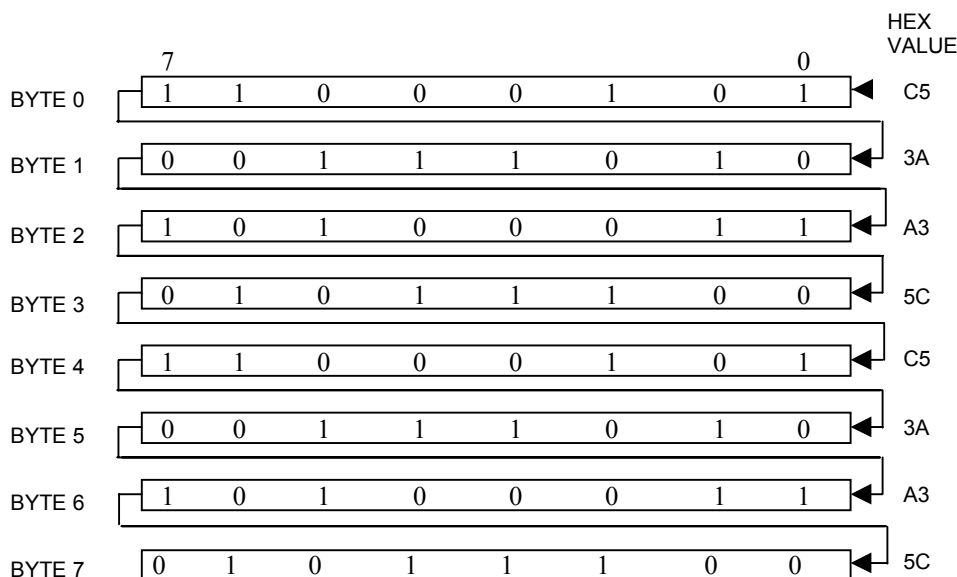
## **PATTERN MATCH—RAM**

Data transfer to and from the timekeeping registers is accomplished with a serial bit stream under control of chip enable ( $\overline{CE}$ ), output enable ( $\overline{OE}$ ), and write enable ( $\overline{WE}$ ). Initially, a read cycle to any memory location using the  $\overline{CE}$  and  $\overline{OE}$  control of the SmartWatch starts the pattern recognition sequence by moving a pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive write cycles are executed using the  $\overline{CE}$  and  $\overline{WE}$  control of the SmartWatch. These 64 write cycles are used only to gain access to the SmartWatch. Therefore, any address to the memory in the socket is acceptable. However, the write cycles generated to gain access to the SmartWatch are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a SmartWatch scratch pad. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for 64 write cycles as described above until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the SmartWatch is enabled and data transfer to or from the timekeeping registers can proceed. The next 64 cycles will cause the SmartWatch to either receive or transmit data on DQ0, depending on the level of the  $\overline{OE}$  pin or the  $\overline{WE}$  pin. Cycles to other locations outside the memory block can be interleaved with  $\overline{CE}$  cycles without interrupting the pattern recognition sequence or data transfer sequence to the SmartWatch.

## **PATTERN MATCH—ROM**

Communication with the SmartWatch is established by pattern recognition of a serial bit stream of 64 bits that must be matched by executing 64 consecutive write cycles, placing address bit A2 low with the proper data on address bit A0. The 64 write cycles are used only to gain access to the SmartWatch. Prior to executing the first of 64 write cycles, a read cycle should be executed by holding A2 high. The read cycle will reset the comparison register pointer within the SmartWatch, ensuring the pattern recognition starts with the first bit of the sequence. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above, until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the SmartWatch is enabled and data transfer to or from the timekeeping registers can proceed. The next 64 cycles will cause the SmartWatch to either receive data on data in (A0) or transmit data on data out (DQ0), depending on the level of /WRITE READ (A2).

## SMARTWATCH COMPARISON REGISTER DEFINITION Figure 1



**Note:** The pattern recognition in Hex is C5, 3A, 5C, C5, 3A, A3, 5C. The odds of this pattern accidentally duplicating and causing inadvertent entry to the SmartWatch are less than 1 in  $10^{19}$ . This pattern is sent to the SmartWatch LSB to MSB.

After power-up, the controller could be in the 64-bit clock register read/write sequence (from an incomplete access prior to power-down). Therefore, it is recommended that a 64-bit read be performed upon power-up to prevent accidental writes to the clock, and to prevent reading clock data when access to the RAM would otherwise be expected.

## NONVOLATILE CONTROLLER OPERATION

The DS1216 SmartWatch performs circuit functions required to make a CMOS RAM nonvolatile. First, a switch is provided to direct power from the battery or  $V_{CC}$  supply, depending on which voltage is greater. This switch has a voltage drop of less than 0.2V. The second function that the SmartWatch provides is power-fail detection, which occurs at  $V_{TP}$ . The DS1216 constantly monitors the  $V_{CC}$  supply. When  $V_{CC}$  goes out of tolerance, a comparator outputs a power-fail signal to the chip-enable logic. The third function accomplishes write protection by holding the chip-enable signal to the memory within 0.2V of  $V_{CC}$  or battery. During nominal power-supply conditions, the memory chip-enable signal will track the chip-enable signal sent to the socket with a maximum propagation delay of 7ns for the 5V and 12ns for the 3.3V version.

## FRESHNESS SEAL

Each DS1216 is shipped from Dallas Semiconductor with its lithium energy source disconnected, ensuring full energy capacity. When  $V_{CC}$  is first applied at a level greater than the lithium energy source is enabled for battery-backup operation.

## SMARTWATCH REGISTER INFORMATION

The SmartWatch information is contained in eight registers of 8 bits, each of which is sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the SmartWatch registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 3.

Data contained in the SmartWatch registers is in binary-coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all eight registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

### AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12-hour or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20–23 hours).

### OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the  $\overline{\text{RESET}}$  and oscillator functions. Bit 4 controls the  $\overline{\text{RESET}}$  (pin 1). When the  $\overline{\text{RESET}}$  bit is set to logic 1, the  $\overline{\text{RESET}}$  input pin is ignored. When the  $\overline{\text{RESET}}$  bit is set to logic 0, a low input on the  $\overline{\text{RESET}}$  pin will cause the SmartWatch to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. When set to logic 1, the oscillator is off. When set to logic 0, the oscillator turns on and the watch becomes operational. These bits are shipped from the factory set to logic 1.

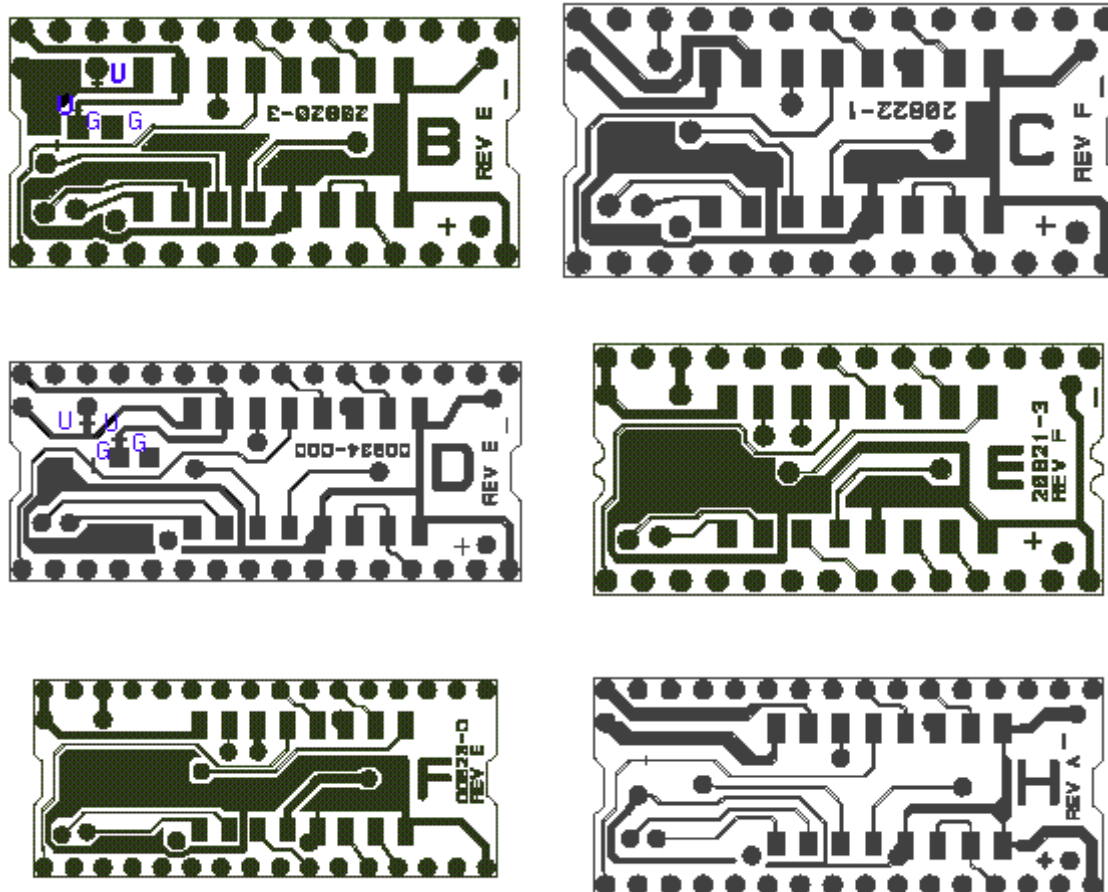
### ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits that will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

### ADDITIONAL INFORMATION

Refer to Application Note 52 for information about using regarding optional modifications and the phantom clock contained within the SmartWatch.

## RESET AND MEMORY DENSITY OPTIONS Figure 2

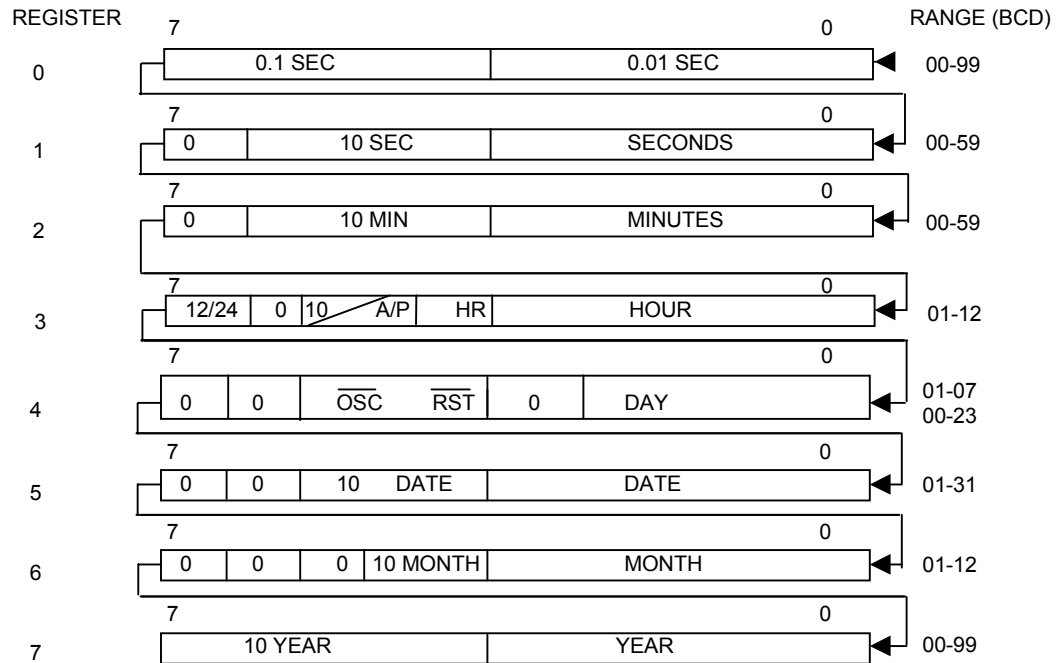


The letter suffix of the SmartWatch is located on the PCB as shown above.

The RESET pin on the controller has an internal pullup resistor. To disable the RESET function, the trace between pin 1 on the socket and pin 13 on the controller can be cut. In this case, the socket will ignore the RESET input, preventing address transitions from resetting the pattern match, even if the RST bit is enabled.

On the DS1216B and DS1216D, the two  $V_{CC}$  pins are connected together on the PCB. The switched  $V_{CC}$  from the controller is connected to the two  $V_{CC}$  pins that connect to the inserted RAM. No modifications are required if the lower density RAM is used. To use the higher density RAM, the trace by the lower density RAM  $V_{CC}$  pin, identified by a hash mark labeled “U,” must be cut. The two square-metal pads, labeled “G,” must be shorted together. This disconnects switched  $V_{CC}$  from the pin going to the inserted RAM, and connects it to the corresponding address input pin for the higher density RAM.

## SMARTWATCH REGISTER DEFINITION Figure 3



**ABSOLUTE MAXIMUM RATINGS\***

Voltage Range on any Pin Relative to Ground	-0.3V to +7.0V for 5V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-40°C to +70°C
Soldering Temperature Range	See J-STD-020A Specification (Note 6)

\* This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS** (0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V <sub>CC</sub> Pin 5V Supply	V <sub>CC</sub>	4.5	5.0	5.5	V	1
Logic 1	V <sub>IH</sub>	2.2		V <sub>CC</sub> + 0.3	V	8
Logic 0	V <sub>IL</sub>	-0.3		+0.8	V	8

**DC ELECTRICAL CHARACTERISTICS** (0°C to +70°C; V<sub>CC</sub> = 5.0 ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V <sub>CC</sub> Supply	I <sub>CC1</sub>			5	mA	1, 2,3
V <sub>CC</sub> Supply Voltage (I <sub>CC0</sub> = 80mA)	V <sub>CC01(U)</sub>	V <sub>CC</sub> - 0.2			V	1, 6
Input Leakage	I <sub>IL</sub>	-1.0		+1.0	μA	2,8,13
Output Logic 1 Voltage (I <sub>OUT</sub> = -1.0mA)	V <sub>OH</sub>	2.4			V	
Output Logic 1 Voltage (I <sub>OUT</sub> = -1.0mA)	V <sub>OL</sub>			0.4	V	
Write Protection Voltage	V <sub>TP</sub>	4.25		4.5	V	

**BACKUP POWER CHARACTERISTICS** (0°C to +70°C; V<sub>CC</sub> < V<sub>TP</sub>)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{\text{CE}}$ Output	V <sub>OH(L)</sub>	V <sub>BAT</sub> - 0.2			V	1
V <sub>CC</sub> Supply Voltage (I <sub>CC0</sub> = 10μA)	V <sub>CC02(U)</sub>	V <sub>BAT</sub> - 0.2			V	1, 6,14
RAM V <sub>CC</sub> (Battery) Voltage	V <sub>BAT</sub>	2	3	3.6	V	1,15
Recovery at Power-Up	t <sub>REC</sub>			2	ms	
V <sub>CC</sub> Slew Rate fall	t <sub>F</sub>	0			μs	
$\overline{\text{CE}}$ Pulse Width	t <sub>CE</sub>			1.5	μs	5



**CAPACITANCE**(T<sub>A</sub> = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>			5	pF	
Output Capacitance	C <sub>OUT</sub>			7	pF	

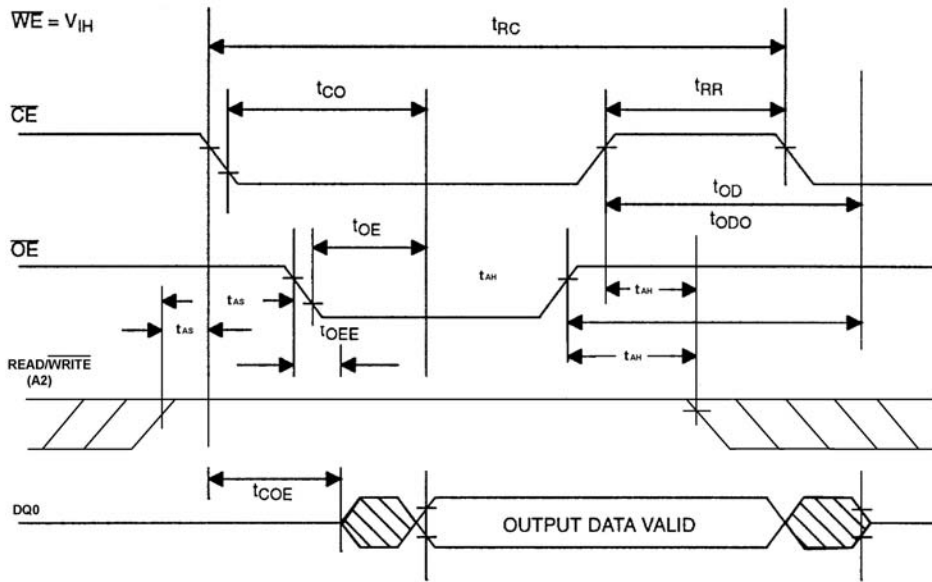
(T<sub>A</sub> = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention	t <sub>DR</sub>			10	Years	14

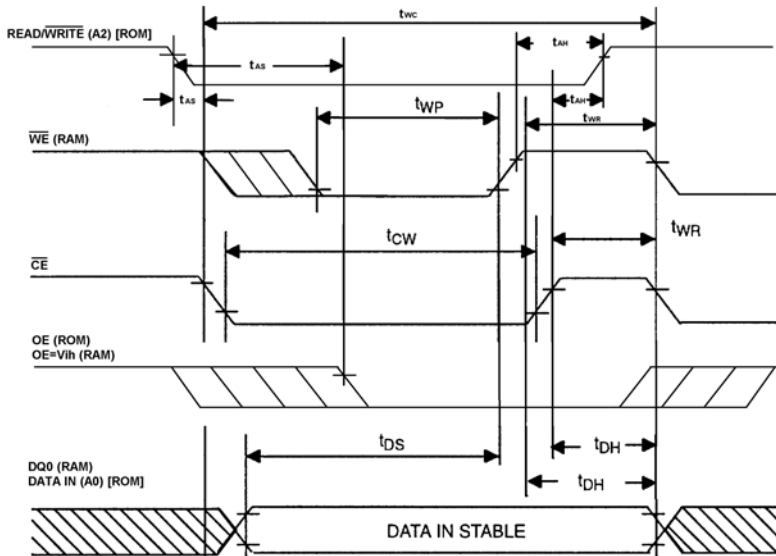
**AC ELECTRICAL CHARACTERISTICS**(0°C to 70°C; V<sub>CC</sub> = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYPE	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	75			ns	
$\overline{\text{CE}}$ Access Time	t <sub>CO</sub>			65	ns	
$\overline{\text{OE}}$ Access Time	t <sub>OE</sub>			65	ns	
$\overline{\text{CE}}$ to Output Low-Z	t <sub>COE</sub>	6			ns	
$\overline{\text{OE}}$ to Output Low-Z	t <sub>OEE</sub>	6			ns	
$\overline{\text{CE}}$ to Output High-Z	t <sub>OD</sub>			30	ns	
$\overline{\text{OE}}$ to Output High-Z	t <sub>ODO</sub>			30	ns	
Address Setup Time (ROM)	t <sub>AS</sub>	20				11
Address Hold Time (ROM)	t <sub>AH</sub>			10		12
Read Recovery	t <sub>RR</sub>	15			ns	
Write Cycle Time	t <sub>WC</sub>	75			ns	
Write Pulse Width	t <sub>WP</sub>	75			ns	
Write Recovery	t <sub>WR</sub>	15			ns	9
Data Setup Time	t <sub>DS</sub>	35			ns	10
Data Hold Time	t <sub>DH</sub>	0			ns	10
$\overline{\text{CE}}$ Pulse Width	t <sub>CW</sub>	65			ns	
$\overline{\text{RESET}}$ Pulse Width	t <sub>RST</sub>	75			ns	
$\overline{\text{CE}}$ Propagation Delay	t <sub>PD</sub>			6	ns	7
$\overline{\text{CE}}$ High to Power-Fail	t <sub>PF</sub>			0	ns	

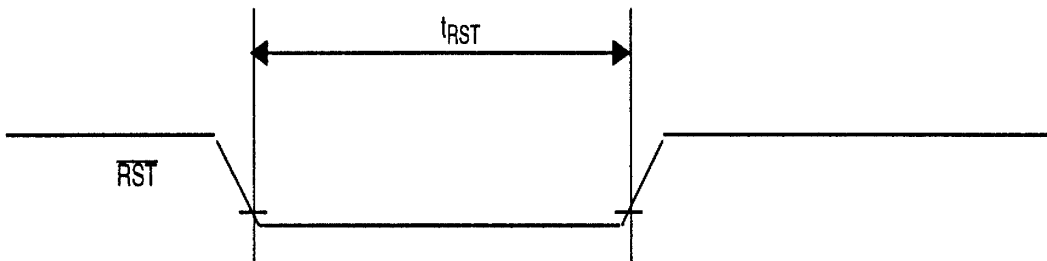
### TIMING DIAGRAM: READ CYCLE TO SMARTWATCH



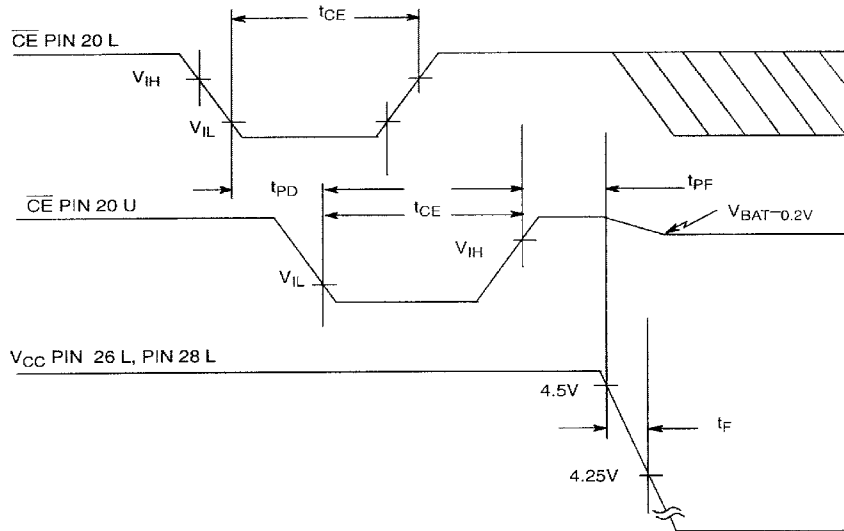
### TIMING DIAGRAM: WRITE CYCLE TO SMARTWATCH



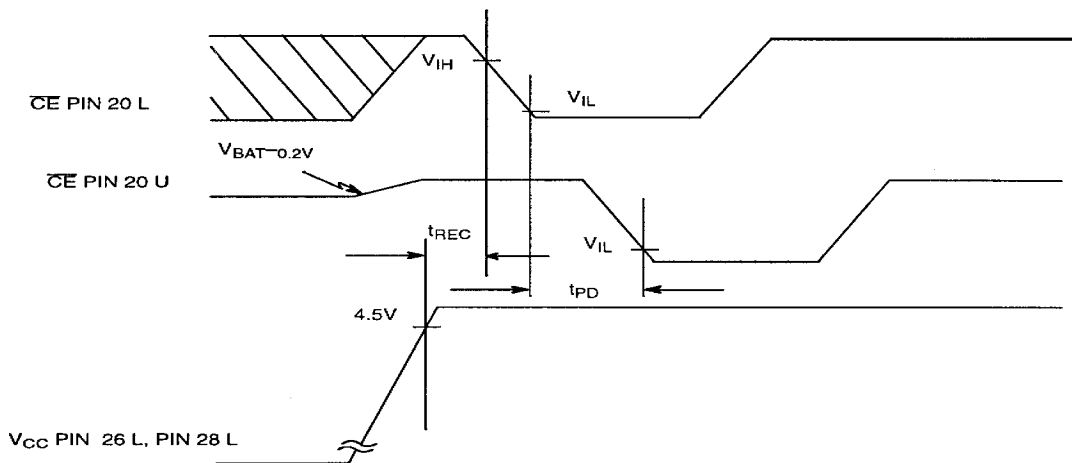
### TIMING DIAGRAM: RESET FOR SMARTWATCH



## TIMING DIAGRAM: POWER-DOWN



## TIMING DIAGRAM: POWER-UP



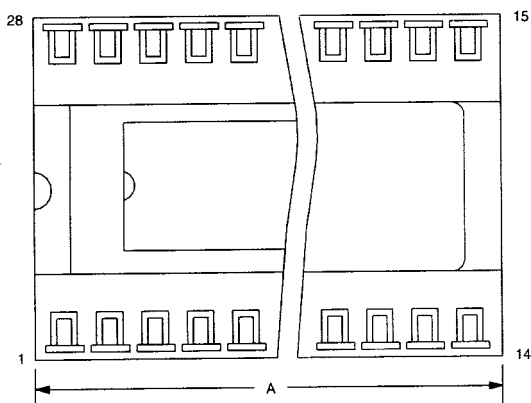
**Warning:** Under no circumstances should negative undershoots of any amplitude be allowed when the device is in battery-backup mode. Water washing for flux removal will discharge internal lithium source because exposed voltage pins are present.

**NOTES:**

- 1) Pin locations are designated “U” when a parameter definition refers to the socket receptacle and “L” when a parameter definition refers to the socket pin.
- 2) No memory inserted in the socket.
- 3) Pin 26L can be connected to  $V_{CC}$  or left disconnected at the PC board.
- 4) SmartWatch sockets can be successfully processed through some conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. However, post-solder cleaning with water washing techniques is not permissible. Discharge to the lithium energy source can result, even if deionized water is utilized. It is equally imperative that ultrasonic vibration is not used in order to avert damage to the quartz crystal resonator employed by the oscillator circuit.
- 5)  $t_{CE\ max}$  must be met to ensure data integrity on power loss.
- 6)  $V_{CCO1}$  is the maximum voltage drop from  $V_{CC}(L)$  to  $V_{CC}(U)$  while power is being supplied by  $V_{CC}(L)$ .  $V_{CCO2}$  is the maximum voltage drop from  $V_{BAT}$  to  $V_{CC}(U)$  while the part is in battery backup.
- 7) Input pulse rise and fall times equal 10ns.
- 8) Applies to pins  $\overline{RST}$  L,  $A2$  L,  $A0$  L,  $CE$  L,  $OE$  L, and  $\overline{WE}$  L.
- 9)  $t_{WR}$  is a functions of the latter occurring edge of  $\overline{WE}$  or  $\overline{CE}$ .
- 10)  $t_{DH}$  and  $t_{DS}$  are a function of the first occurring edge of  $\overline{WE}$  or  $\overline{CE}$ .
- 11)  $T_{as}$  is a function of the first occurring edge of  $OE$  or  $CE$ .
- 12)  $T_{ah}$  is a function of the latter occurring edge of  $OE$  or  $CE$ .
- 13)  $\overline{RST}$  (Pin 1) has an internal pullup resistor.
- 14) Expected data retention is based on using an external SRAM with a data retention current of less than 0.5 $\mu$ A at +25°C. Expected data retention time (time while on battery) for a given RAM battery current can be calculated using the following formula:  

$$0.045 / (\text{current in amps}) = \text{data retention time in hours}$$
- 15) The DS1216 products are shipped with the battery-backup power off. First power-up switches backup battery on to clock and RAM  $V_{CC}$  pin upon power down.

**DS1216 28 SMARTWATCH**



PKG	28-PIN		32-PIN	
DIM	MIN	MAX	MIN	MAX
A IN.	1.390	1.420	1.580	1.620
MM	35.31	36.07	40.13	41.14
B IN.	0.690	0.720	0.690	0.720
MM	17.53	18.29	17.53	18.29
C IN.	0.420	0.470	0.400	0.470
MM	10.67	11.94	10.16	11.94
D IN.	0.035	0.065	0.035	0.065
MM	0.89	1.65	0.89	1.65
E IN.	0.055	0.075	0.055	0.075
MM	1.39	1.90	1.39	1.90
F IN.	0.120	0.160	0.120	0.160
MM	3.04	4.06	3.04	4.06
G IN.	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79
H IN.	0.590	0.630	0.590	0.630
MM	14.99	16.00	14.99	16.00
J IN.	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30
K IN.	0.015	0.021	0.015	0.021
MM	0.38	0.53	0.38	0.53
L IN.	0.380	0.420	0.380	0.420
MM	9.65	10.67	9.65	10.67

