E-PAC 3000 G2

HARDWARE REFERENCE MANUAL

FOR BOARD REVISION 3

MANUAL REVISION 2.0

DISCLAIMER

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FCC COMPLIANCE

EMAC's E-PAC series of computers and accessories are classified as sub-assemblies per FCC CST bulletin, No. 62, May 1984. The bulletin states that sub-assemblies are not themselves subject to the FCC rules. Only the end product is directly subject to the rules.

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THE E-PAC 3000 G2

INTRODUCTION

We at EMAC hope that you will find the E-PAC 3000 G2 to be as powerful and useful as we do. Please carefully read this User's Guide before and during operation of your new single board computer (SBC).

The E-PAC 3000 G2 board was designed to maximize the amount of control and monitor features available on a single printed circuit board. This industrial strength computer is packed with features you might expect to find on a multi-board system. The E-PAC 3000 G2 comes equipped with 16 analog to digital channels with sample and hold, 8 optically coupled digital inputs, 8 buffered digital outputs, 16 programmable I/O lines, 4 serial ports, watchdog timer and more.

STANDARD FEATURES

CENTRAL PROCESSING UNIT
Hitachi's HD64180 or Zilog's Z180 CMOS microprocessor running at 6.144 Mhz.

INPUTS/OUTPUTS
8 optically coupled digital inputs, 8 buffered digital outputs (high current drive), 16 programmable I/O lines, 16 12-bit (or optional 16 bit) analog inputs, 40 pin header I/O connector and 50 pin I/O rack compatible connector.

MEMORY
Memory space is available for up to 512K of EPROM or Flash and up to 512K of static RAM. A 1K bit EEPROM is also included.

POWER SUPPLY
Single voltage supply +8 to +15 Vdc. with on board regulation.

TIMERS
Watchdog timer (a hardware reset will occur if software does not periodically access the timer), two programmable 16 bit timers, and four 8 bit counter/timers. All programmable timers and counters have interrupt support.

COMMUNICATIONS
Four RS232 ports come standard, one optional, and one port can be optionally configured as a full duplex RS422/485 port.

CHARACTER AND GRAPHIC LCD INTERFACES
A dual row 16 pin header is provided which interfaces to OPTREX (c) DMC series character displays or compatibles. This header has connections for optional LED backlit displays to allow software control of the backlight. Another header interfaces to LCD displays capable of combined graphics and text, such as the DENSITRON LM4229.

DIP SWITCH
7 switches for program options and selections.

SOCKETS
High reliability machined sockets for Memory IC's.

EXPANSIBILITY
50 pin header connector for use with expansion boards.

DIMENSIONS
The 3000 G2 with all of its I/O is only 8" by 5.25" and 0.75" high.

OPTIONAL ON-BOARD HARDWARE FEATURES

HIGH SPEED OPTION
The standard 6.144 MHz clock speed can be upgraded to 12.288 MHz.

ANALOG SPIKE PROTECTION
The E-PAC 3000 G2 analog multiplexer may be upgraded to have overvoltage protection in addition to several hundred volts of transient spike protection. This IC is installed at the factory if requested.

REAL TIME CLOCK CALENDAR
The E-PAC can be equipped with a real time clock/calendar (RTC). The RTC contains a lithium energy cell which maintains clock information and RAM memory data. The clock keeps time in hundredths of seconds, seconds, minutes, hours, day of week, date of month, month and year. The month and year determine the number of days in each month. If you have the real time clock option refer to the specification sheet included in your RTC Supplement for technical and programming specifications. This option can be installed at any time by the user or at the factory before shipping.

32K X 8, 128K X 8 OR 512K X 8 NONVOLATILE RAM (RAMDISK)
EMAC has a 32K and a 128K RAMDISK available for source code or data storage. The RAMDISK has a built-in lithium energy cell which maintains data in RAM memory. Source code or data can be written into and stored for later use in the RAMDISK. The RAMDISK may be removed from the E-PAC and replaced at a later time without loss of memory which allows the RAMDISKS(s) to be removed/inserted much like floppy disks. The E-FORTH and MTBASIC operating system fully supports the operation of the RAMDISK.

SERIAL PORT, KEYPAD, SERIAL KEYBOARD INTERFACE
An optional on-boad coprocessor gives an additional RS-232 serial port and the capability to scan a matrix of 8x7 keys, or to interface to a serial keyboard. It is also factory programmable for custom functions as well.

OTHER OPTIONS FOR E-PAC SYSTEMS

TERMINAL BOARD: A perfect board for terminating all those I/O connections.
SIGNAL CONDITIONING CARDS: A low cost method of implementing Analog I/O.
EPROM PROGRAMMER BOARD: A simple solution to burning application programs.
PROGRAMMABLE 32 LINE PARALLEL BOARD: For 32 additional lines of programmable digital I/O.
DISPLAY BOARD: An economical method of interactive communication.
PARALLEL PRINTER BOARD: For printing data or whenever a hard copy is needed.
SUPPORT SOFTWARE: When your E-PAC needs to communicate to your PC.

FOR MORE INFORMATION ON THE ABOVE ITEMS JUST GIVE US A CALL.

EMAC's E-PAC 3000 G2 has most everything you need to start programming your monitor and control application. Following is additional information helpful in setting up your E-PAC 3000 G2.

64180/Z180 MPU DESCRIPTION64180/Z180 MPU DESCRIPTION

The MPU for the 3000 G2 is a Hitachi type HD64180 or the Zilog Z180 second source. This chip incorporates the 8080, and Z80 instruction sets, as well as several very powerful new instruction. The hardware interface is a combination of the two bus structures, but is primarily INTEL structure by nature. The HD64180/Z180 integrates a number of peripheral devices, as well as the core CPU. This additional hardware reduces the number of peripheral chips normally required to build a working MPU board.

The additional peripherals include two built in UARTS for serial communication, two 16 bit timers, a two channel DMA controller, an interrupt controller, and a memory management unit (MMU).

The HD64180/Z180 MPU has a one megabyte addressing range, and a 64K device I/O map. The MPU has some limitations, due to pin function tradeoffs, but on a whole is very powerful.

Certain pin function tradeoffs were made by Hitachi in the design of the HD64180. Internal registers set whether a pin functions as an input for the DMA system or as a CTS line for serial communication, or whether an output pin functions as a timer output or an address line. In the case of the 3000 G2, priority is given to the DMA controller for the DMA/CTS tradeoff.

As for the address line/timer output pin tradeoff EMAC opted for the timer output. Many applications require a hardware output from a timer, for use as a speaker port output, serial clock, etc. The 3000 G2 memory decoder does not take the A18/TOUT pin into consideration thus the 512k memory limit.

The speed at which the MPU operates is set by a crystal, reference designator Y1. The standard speed board uses a 12.288 Mhz crystal, which is internally divided by two inside the MPU, and the actual clock speed therefore is 6.144 Mhz. EMAC offers the slower clock speed for users who may require a lower power consumption. In the case of a speed upgraded 3000 G2, the crystal is replaced with a 18.432 MHz crystal, and a higher speed grade MPU is used allowing more software throughput.

The MPU works hand in hand with Zilog KIO chip. Interrupts are daisy chained from the KIO to INT0 of the HD64180/Z180 processor (see section on interrupts). In order for KIO interrupts to function properly the MPU must be put in a special Z mode. This is accomplished by setting bits 5 and 7 to logic 1, of the operation mode control register (I/O address 3EH). This is the default configuration for the Z180 and the special Z mask version of the HD64180ZCP.

EXTERNAL HARDWARE RESET

A screw connection for an external reset is provided on the E-PAC 3000 G2. To generate an external reset, connect ground to the external reset input, pin 2 of screw terminal connector ST1, using a switch, relay, or logic device. If a logic device is used, it must be able to safely sink 13 ma. of current. See Appendix A "External Reset Drawing"

POWER REQUIREMENTS

ON-BOARD VOLTAGE REGULATION AND GENERATION

A single +8 to +15 Vdc. power supply is all that is required because a negative supply is produced on board by a DC to DC converter. The DC to DC converter automatically produces a negative voltage which tracks the positive voltage used to power the board (i.e. if 8 volts DC is fed to the 3000 G2, the negative supply will mirror it with a -8 volts). The typical current draw of the E-PAC 3000 G2 is 150 mA. in the standard configuration.

Connect the + volts lead of the power supply to pin 1 and the ground lead to pin 2 of the screw terminal connector ST2, refer to Appendix C "Component Layout".

The power supply delivers the appropriate power supply voltages to the various circuits in the 3000 G2. The power supply that feeds the board may come from screw terminal ST2 (pin 1 Vin and pin 2 system ground) or from the terminal board/external source, via header connector HDR4. A diode will short out the supply input should the power supply be connected backwards, to protect the 3000 G2 from supply reversal, however, it will not protect against overvoltage.

The digital system will operate down to 7 volts or even lower without regulation, but to permit correct analog system performance, at least 12 volts must be used to operate correctly at the +-10 volt ranges (see the Analog to Digital section). 15 volts DC is the absolute maximum safe input voltage.

The DC power supply input to the 3000 G2 need not be regulated, but it should be well filtered. Although tight regulation is not essential to the proper operation of the 3000 G2, care should be taken to see to it the input voltage, power supply ripple peaks included, do not fall below the minimum voltage requirements for the analog configuration in use, and also that power plus ripple never totals more than 15 volts.

Should the supply voltage ripple fall beneath the supply overhead requirement, this ripple will impress itself onto the signal(s) fed to the A/D, causing erratic readings of the input codes, which will adversely affect the accuracy of A/D readings by the 3000 G2. This same ripple may also appear on the analog outputs of 3000 G2 boards with the D/A option. Also, should the voltage positive ripple peak too high, the inverting power supply and RS-232 chips will be at risk of destruction, as they are rated at 15 volts maximum. (The ratings of these parts are what set the

maximum limit). As long as the power supply input voltage stays between the minimum overhead and maximum breakdown levels, the power supply voltage will have no adverse effect on the unit's analog accuracy.

When applications with large power supply input voltage fluctuations are possible, it is suggested that pre-regulation be employed ahead of the 3000 G2, to help avoid problems.

USING EXTERNAL VOLTAGE SOURCES

The 3000 G2 has the option of bypassing the on-board 5V regulator and/or DC to DC converter, allowing for use of external 5V regulated and ±V supplies.

Putting jumpers in positions A-B and C-D of JP15 enables use of the on-board 5V regulator. A jumper in position D-E only, enables the external 5V regulated input on ST2 pin 5.

ST2

5	+5V in (regulated)
4	-Vin
3	Graphic LCD backlight +Vin
2	GND
1	+Vin

Putting jumpers in positions A-B and C-D of JP14 enables use of the on-board negative voltage charge pump. A jumper in position D-E only, enables the external -V input on ST2 pin 4. This option requires a +Vin input on ST2 pin 1 to supply the positive voltage for the RS-232 chips.

The external supplies must be in same range as specified in the previous section and the 5V supply must be regulated.

MEMORY CONFIGURATION

The E-PAC 3000 G2 can be configured to address up to 1 megabyte of memory devices.

SOCKET U19

This socket accepts EPROM or Flash devices of various sizes by configuring a few jumpers.

EPROM JUMPER SETTINGS

	JP5	JP6	JP7	JP8,9,10
64K/128K EPROM (AT27C512R/C010R)	A	A	A	A
256K EPROM (AT27C020R EPROM)	A	A	B	B
	See notes for JP10 below regarding this configuration.			
512K EPROM (AT27C040R EPROM)	A	B	B	B
	See notes for JP10 below regarding this configuration.			

FLASH JUMPER SETTINGS

(Removing the jumper completely from JP6 will write protect the flash)

	JP5	JP6	JP7	JP8,9,10
64K/128K FLASH (AT29C512/C010 PEROM)	B	A	B	A
256K/512K FLASH (AT29C020/C040 PEROM)	B	A	B	B
	See notes for JP10 below regarding this configuration.			

SOCKET U20
This accepts RAM devices only.

RAM MEMORY JUMPER	JP11	
32K/128K RAM	A	
512K RAM	B	(this requires JP8-JP10 to be in position B)

SOCKET U21 AND U22
These accept 32K/128K RAM devices only. If JP8-JP10 are in position B and a memory device is in socket U20, devices should not be put in sockets U21 or U22 since they share the same memory space.

MEMORY MAP OPTIONS

JP8-JP10 in position A

SOCKET	START	END	SIZE	DEVICE TYPE
U19	0:0000	1:FFFF	64K to 128K	EPROM/Flash
U20	2:0000	3:FFFF	32K to 128K	RAM
U21	8:0000	9:FFFF	32K to 128K	RAM
U22	A:0000	B:FFFF	32K to 128K	RAM

JP8-JP10 in position B

SOCKET	START	END	SIZE	DEVICE TYPE
U19	0:0000	7:FFFF	64K to 512K	EPROM/Flash
U20	8:0000	F:FFFF	32K to 512K	RAM
(if a memory device is in socket U20, devices should not be put in sockets U21 or U22 since they share the same map)				
U21	8:0000	9:FFFF	32K to 128K	RAM
U22	A:0000	B:FFFF	32K to 128K	RAM

For more information on the function of the jumpers, see JUMPER DESCRIPTIONS in the appendices.

SEEPROM

The Serial EEPROM (93C46) is 1K bit in size providing 64, 16 bit words of serially accessed nonvolatile memory. To utilize the SEEPROM, control and data signals must be provided. Setting Port C bit 4 (I/O address 102H) high selects the SEEPROM and allows SEEPROM data to be read through the most significant bit (bit 7) of the dipswitch port (I/O address 40H). Port C bit 1 is used to write data to the SEEPROM. When writing or reading data from the SEEPROM each bit must clocked in or out. Port C bit 0 is used to drive the clock input of the SEEPROM. See appendix E for further information on the 93C46.

The 3000 G2's SEEPROM unit contains 16 bit words which can be written and read from. The SEEPROM is intended for semi-permanent non volatile storage of special operating parameters, such as storage of baud rates, network or password IDs, etc. It should not be used as true read/write memory as it has a limited amount of write cycles (10,000). Access is though a serial data format, created by software. The SEEPROM chip has only 4 active pins, serial data in, serial data out, serial clock, and chip enable. The chip is a type 93C46. PPI port C, bit 4 should be set high to enable this chip. Serial data clock and serial data in share port lines with the analog system's multiplexer bits PPI Port C bit 0 and bit 1. Therefore, mixing analog channel reads with SEEPROM accesses will inadvertently cause the multiplexer to change channels. When this happens, the 3 microsecond settling time is required prior to the next analog conversion (see Analog to Digital Conversion section). The data or status of the SEEPROM is read at a spare input bit on the DIP switch port, input Bit 7.

E-PAC 3000 G2 I/O

The HD64180/Z180 MPU can access up to 64K of I/O device addresses. It has a variety of 8080 and Z80 type I/O addressing modes, plus some special internal device addressing modes. Some of the 3000 G2 I/O devices are the ones built into the MPU, the rest are separate devices spread about the board. The MPU reserves 40 hex of I/O addresses for itself. When these addresses are used by the software, the bus cycles also appear on the 3000 G2 bus. The MPU ignores external bus activity while internal I/O transactions take place. To avoid contention, and to allow the 3000 G2 and expansion accessories to properly function with the MPU, the I/O decoder ignores those addresses reserved by the HD64180/Z180.

The I/O decoder for the 3000 G2 decodes address lines A6 through A10. The decoder is a 1 of 8 decoder, type 74HC138, reference designator U17. because it does not decode the lower address lines A0 through A5, the decoded chip selects will not change for 40 hex consecutive addresses. The reserved addresses of the MPU, addresses 00 hex through 3F hex, will all fall into chip select CS0. As there are no devices selected by the Y0 output of the decoder, no 3000 G2 I/O devices will be selected for those addresses. MPU I/O transactions at theses addresses will therefore go to the internal devices only.

The various devices selected by the I/O decoder will proceed linearly at 40 hex boundaries until I/O address 200 hex. Decoder U18B, the other half of a 74HC139 1 of 4 decoder, monitors address lines A9 and A10, and will negate an enabling line for the I/O decoder. This allows external I/O mapped peripheral cards made for the 3000 G2 to use I/O addresses from 200 to 7FF hex with no contention with older EMAC peripherals. The external I/O cards must have an I/O decoder operating in parallel with the 3000 G2,s decoder.

All I/O transactions are qualified with MPU signal IOE*. Signal IOE* is inverted to IOE, which passes on to the expansion bus connector. On the 3000 G2, this signal takes the place of the former IO/M* signal used on the E-PAC 1000, 2000 series boards. As no external memory is possible, the IOE line indicates only that an I/O map transaction is in progress.

The I/O decoder selects ranges of I/O device addresses much larger than actually consumed by the I/O devices used on the 3000 G2. This is because 40 hex addresses are reserved for MPU internal I/O addressing, so the 3000 G2 I/O decoder bridges address lines higher than A0 through A5. The eight I/O groups selected span 40 hex addresses each. The highest I/O address selected by the 3000 G2 I/O decoder is I/O address 1FF hex. The decoder is disabled by U19 for addresses 200 hex through 7FF hex, but reenables at 800 hex. The access repeats over and over throughout the 64K address range.

I/O addresses from 00 hex to 3F hex are to be used only by the MPU, addresses 40 hex through 1FF hex are reserved for 3000 G2 and EMAC expansion card functions, and the remaining addresses 200 hex through 7FF hex are available to the application user for expansion cards of his own design. See appendix D for a complete I/O address listing.

KIO DESCRIPTION

The 3000 G2 makes use of the Zilog KIO (84C90) chip to pack a lot of functionality onto the board. Its reference designator is U15.
The KIO contains three parallel TTL level I/O ports, two serial ports, and four timer/counters. All units within it function exactly as their separate chip counterparts, the PIO, the SIO, and the CTC Zilog peripherals. Of course, some pin functions must trade off as the 84 pin J lead package cannot support every pin function for all devices simultaneously. However, Zilog seems to have made better pin function tradeoff choices on the KIO than most other chip makers have on some of their multifunction chips. See appendix E for exact programming details.

The KIO's PIO unit, (Parallel I/O) has two 8 bit wide parallel TTL/MOS level compatible digital I/O ports. These ports are directly wired to the 3000 G2's TTL I/O port, 50 pin connector header HDR2. Both ports may be set to various input or output modes. In MODE3, individual bits may be set independently as input or output, providing total application flexibility. The 3000 G2 does not, however, provide the handshaking lines used in the strobed I/O mode 2 of the KIO. Modes 1 and/or 3 are recommended for the parallel ports.

These parallel ports have interrupt control masks that can be programmed to generate an interrupt for a given set of input/output conditions, so that any one input or combination of inputs can trigger an interrupt for fast servicing of priority or emergency conditions.

The KIO's serial unit, SIO (Serial I/O), consists of two independent serial communication units, that support asynchronous or synchronous serial data transmission or reception. The 3000 G2 provides RS-232 level interface chips and 10 pin ribbon cable headers CN2 and CN3, for both channels. As with the PIO, the SIO unit has a host of interrupt sources within it.

The KIO's CTC unit, (Counter Timer Circuit) has four, 8 bit counters. The four Counter Timer Circuits as the name implies can be used for counters as well as timers. Each counter/timer has a selection of input, output, and control input selections. The KIO's CTC provides the 3000 G2 with four additional timers. However, their function is quite tricky. Each timer/counter can be set and used independently. Each one has an eight bit counter that counts down from its loaded count to zero. When it reaches zero, it outputs a pulse equal to one half the clock period. They can not be set to produce a square wave output. (That is why the A18/TOUT pin of the MPU was set to TOUT, even though it cheats us out of an address line, and 512 K of memory).

If a channel is used as a timer, it counts only the system clock, through a selectable prescaler of 16 or 256. As the system clock is 6.144 or 12.288 MHz, these timers don't take long to time out. Each counter/timer can be set to start with an external gate pulse, and the gate polarity can be set to rising or falling edge trigger, otherwise the timer can be set to reload and retrigger automatically. Each timer/counter can be set to count input pulses, once again the polarity of the count trigger is selectable. Each timer/counter has two hardware access pins. These pins go to a header connector, HDR3. HDR3 is for hardware access to the four timer/counters in the KIO, and the TOUT of the HD64180/Z180.

The KIO control section is specific to the KIO only. Register KIO command register, at I/O address 8EH, is used to set the Daisy chain interrupt priority order, to reset individually any of the PIO, SIO, or CTC units, and to switch the third digital I/O port's functions. The pin function tradeoff mentioned previously is selected here. The port can be set to access the SIO handshake lines directly, or can be switched into a direct parallel I/O port. If set to the port mode, the bit direction is set via PIA PORT C Command register at I/O address 8DH. Data I/O for that port is found at I/O address 8CH.

The KIO has a spare oscillator circuit built into it, normally used by Zilog systems for generation of the system clock, but since the 3000 G2 already has a system clock, this oscillator is used to generate a unique clock source for the A/D system, which requires a different clock frequency than the MPU for its own internal processes.

SERIAL COMMUNICATIONS PORTS

Four RS232 asynchronous communication ports are provided as part of your E-PAC 3000 G2. RS232 negative supply voltage is generated by the DC to DC converter on the E-PAC 3000 G2 (or optionally, -V input from outside the board). Connection to the COM0 (Asynchronous Serial Communications Interface 1, ASCI1) RS232 port is provided via the screw terminal connector (ST1), and connection to the COM1 (ASCI0) RS232 port is provided via a 10 pin head connector (CN1) (see the "Component Layout" drawing). E-FORTH and MTBASIC use COM1 for standard default communications.

The COM0 and COM1 ports are both implemented in the HD64180/Z180 microprocessor. These asynchronous serial ports provide full duplex serial communication at software selectable Baud Rates of 300 to 76800 Baud (76800 requires 24.576 crystal). To set the baud rate, the correct prescale value (divide by 10 or 30) and the correct divide ratio must be selected. These values are chosen depending on the baud rate desired and the clock frequency of the processor. The Asynchronous Serial Communications Interface (ASCI) Control Register B is used to set the baud rate. In addition to setting the baud rate, the number of bits, the type of parity, and the number of stop bits must be selected. These parameters are set by ASCI Control Register A. See appendix E for more information on the ASCI.

The ASCI serial port 0 is the E-PAC 3000 G2 port COM 1 and ASCI serial port 1 is the E-PAC 3000 G2 COM 0 for downward compatibility. Both of these serial ports have the provision to be used in a interrupt mode or a polled mode. To use the ASCI in the interrupt mode, first enable the interrupts using the ASCI Status Register and "EI" instruction and provide the software interrupt handlers at the software selectable vector. In the polled mode of operation for reception, check bit 7 (RDRF) of the ASCI Status Register. If this bit is high then there is a byte available for reading. This byte can be read from the ASCI Receive Data Register. For transmission, check bit 1 (TDRE) of the ASCI Status Register. If this bit is high then the transmit buffer is empty a byte may be written to the ASCI Transmit Data Register.

An optional RS422/485 replacement of the COM0 RS232 port is available. The RS422/485 port can be used as a full or half duplex port. It is accessible via screw terminal ST1, which is a seven position screw terminal. RS-232 interface IC U2 has a dual socket position. Placement of the chip at station " A " connects it for straight RS-232 communication from the UART in the MPU to the screw terminations. Placement of the chip to position " B ", and installing the two RS-422/485 chips, convert this port to RS-422/485.

The RS-422/485 option permits use of a full duplex RS-422 current loop communication port, (4 wire) or by tying the output and input pins together, a half duplex, RS-485 NETWORKING port can be had. Up to 32 similar ports may share the same communication lines. To prevent contention especially when used as a half duplex port, care must be taken to assure that only one port transmits at a time. The system

automatically powers up in the receive mode. To transmit, set KIO port C line 0 high (I/O address 8CH), to receive set the same line low. To force the transmit output low, set KIO port C line 1 high, for normal operation this line is low. The RS422/485 option is necessary when using E-PAC SDOS NET.

The HD64180/Z180 ASCI ports also provide the ability for a nine bit network. This innovative function when enabled, will interrupt the processor if the ninth bit of a data byte is set. Using this feature in conjunction with the multi-drop RS485 option and software drivers provide all the components of a simple yet powerful nine bit network.

SERIAL CONNECTORS

COM0 (ASCI1)

(RS-232)

7 ☐ TA
6 ☐ TB
5 ☐ **RX**/RA
4 ☐ **TX**/RB
3 ☐ **GND**
2 ☐ RST*
1 ☐ NMI

(RS422/485 OPTION)

7 ☐ **TA**
6 ☐ **TB**
5 ☐ RX/**RA**
4 ☐ TX/**RB**
3 ☐ **GND**
2 ☐ RST*
1 ☐ NMI

COM1 (ASCI0)

```
    1   2
nc  . . nc
TX  . . RTS0
RX  . . CTS0
nc  . . nc
GND . . nc
    9   10
```

RTS0 = CNTLA0 BIT 4
CTS0 = CNTLB0 BIT 5

COM2 (SIO A)

```
    1   2
nc  . . nc
TX  . . DTR
RX  . . DCD
RTS . . CTS
GND . . nc
    9   10
```

DTR = KIO PORT C BIT 5
DCD = SIOA RD REG 0 BIT 3
CTS = SIOA RD REG 0 BIT 5
RTS = KIO PORT C BIT 4
nc = No connect

COM3 (SIO B)

```
    1   2
nc  . . nc
TX  . . nc
RX  . . nc
RTS . . CTS
GND . . nc
    9   10
```

RTS=KIO PORT C BIT 3
CTS=KIO PORT C BIT 2

COM4 (OPTIONAL)

```
      1   2
   nc . .  nc
TX232 . .  CP1.7
RX232 . .  nc
TXTTL . .  nc
  GND . .  Vcc
      9   10
```

CP1.7 = COPROCESSOR P1.7
TXTTL = TTL/MOS TX OUTPUT

COM0 (ACSI1) does not offer any handshaking lines when used in either the RS232 mode or RS485 mode.

COM1-COM4 are all 10 pin header connectors which are compatible with DB9 crimp on ribbon connectors. You may purchase a pre-made DB9 to 10 pin header adapter from EMAC (part # E010-06).

COM1 (ASCI0) is RS-232 only. It has a 10 pin dual row connector (CN1) for connection to a terminal or PC. This port is the normal default communication port for the 3000 G2. All EMAC operating system software communicates through this port for programming the 3000 G2. Two handshaking lines are available for this port CTS pin 8 and RTS pin 7. CTS has a pullup resistor to render it inactive when not connected, permitting communication. TXD is available on pin 2, RXD on pin 3, and ground on pin 5.

COM2 (SIOA) and COM3 (SIOB) are also RS-232 only. They are driven by the two serial communication systems in the KIO chip. Although the KIO supports synchronous and asynchronous operation, these serial ports are configured for asynchronous operation only, due to the unavailability of a serial clock pin assignment on the headers.

To set the baud rate of COM2 and COM3, HDR3 pins 11 and 12, and pins 13 and 14 should be jumpered (which connects *CRYSTAL FREQUENCY*/4 to CTC2 and CTC3 respectively). CTC2 and CTC3 must be configured to be counters and programmed with the appropriate scaler value (see section on TIMERs). COM2 uses CTC2 and COM3 uses CTC3 to determine associated baud rates. The corresponding counter prescales its CLK input and is further divided by programming the SIO for X16, X32, or X64 clock mode (the X1 mode shouldn't be used due to limitations of the SIO). Using the X16 or the X32 clock mode furnishes all of the standard baud rates for either crystal frequency (crystal frequency/4 / CTC time constant / clock mode = baud rate). In addition to programming the baud rate the number of data bits, number of stop bits, parity, async or sync operation, and handshaking if any must also be programmed.

The SIO section of the KIO offers a number of interesting and powerful features involving CRC generation/checking, status error conditions, and interrupts. There are eight interrupt vectors set aside for COM2 and COM3 within the KIO. In addition to receive/transmit for both channels, there are several interrupts for error status conditions as well as handshaking lines. Interrupts can be generated on each character received or on the first character received. To use interrupts the base vector address must be programmed through "WRITE REGISTER 2" of SIOB, in

addition to programming the processor for INT mode 2 and initializing interrupt vector register I. Register I provides the upper 8 bits of the vector and SIO supplies the lower 8 bits (see section on interrupts). Interrupts must also be enabled both at the SIO and at the HD64180/Z180, before COM2 and COM3 interrupts will be acknowledged.

If interrupt driven communication is not necessary for COM2 and COM3, the simpler and easier method of polling can be used. To poll for receiver ready, check "READ REGISTER 0", bit 0 for a high. To poll for transmitter empty check "READ REGISTER 0", bit 2 for a high.

CHARACTER LCD INTERFACECHARACTER LCD INTERFACE

A dual row 16 pin header is provided which interfaces to OPTREX (c) DMC series character displays or compatibles. These displays are available in a variety of formats, such as 16x1 (16 characters by 1 line), 20x2 or 40x4). The data register is at I/O address 141 hex and the command register is at 140 hex (see your LCD display's data manual for programming instructions). Currently the LCD interface is write only. This header has connections for optional LED backlit displays to allow software control of the backlight. The backlight is turned on by configuring bit 7 of KIO port C to be an output and setting it high (setting it low turns off the backlight).

LCD PANEL HDR5

```
     1    2
   VCC .  . GND
RS (A0) .  . CONTRAST
     E .  . R/W*
    D1 .  . DO
    D3 .  . D2
    D5 .  . D4
    D7 .  . D6
BACKLIGHT K .  . BACKLIGHT A
     15    16
```

Setting KIO port C bit 7 high will turn on the backlight.

GRAPHIC LCD INTERFACE

This allows interfacing to LCD displays capable of combined graphics and text, such as the DENSITRON LM4229. It provides all the necessary control lines and brings external voltage from ST2 pin 3 to supply the backlight, if necessary. JP13 selects the font size for an LM4229 display according to the following table:

	MD2	**FS1**
6X8 Font LO	HI	
8X8 Font HI	LO	

The command/status register is 200h and the data register is 201h but currently the interface is write only. Refer to the data manual of the desired graphic LCD device for programming details.

GRAPHIC LCD HDR6

```
2   1
 . . GROUND
 . . Vcc
 . . (no connect)
 . . C/D*
 . . RD*
 . . WR*
 . . XD0
 . . XD1
 . . XD2
 . . XD3
 . . XD4
 . . XD5
 . . XD6
 . . XD7
 . . CE*
 . . RESET*
 . . (no connect)
 . . MD2
 . . FC1
 . . + BACKLIGHT VOLTAGE
40  39
```

All even numbered pins are digital ground.

COPROCESSOR

The optional coprocessor adds the following features to the 3000G2: an additional serial port with a character buffer for inputs and outputs, a 8 by 7 keypad decoder and a 16 bit counter. All communication to it is through the Z180's Clocked Serial I/O interface (CSIO) with the INT2* interrupt used as an attention signal to the Z180. Due to the complexity of the interface it is described in the assembly language drivers software.

```
        4X4 SCAN MODE
            1   2
     SCAN 1  . . XSCAN 8
     SCAN 2  . . XSCAN 7
     SCAN 3  . . XSCAN 6
     SCAN 4  . . XSCAN 5
       IN 1  . . XSCAN 4
       IN 2  . . XSCAN 3
       IN 3  . . XSCAN 2
       IN 4  . . XSCAN 1
        GND  . . IN6
        GND  . . IN5
           19   20
Italicized pins are not used
in scanning keys.
```

```
              8X7 SCAN MODE
      (requires custom coprocessor)
                  1   2
           SCAN 1  . . XSCAN 8
           SCAN 2  . . XSCAN 7
           SCAN 3  . . XSCAN 6
             IN 0  . . XSCAN 5
             IN 1  . . XSCAN 4
             IN 2  . . XSCAN 3
             IN 3  . . XSCAN 2
             IN 4  . . XSCAN 1
              GND  . . IN6
              GND  . . IN5
                 19   20
```

When special custom features are needed on the 3000G2 board, many of these can be implemented on the coprocessor. EMAC can custom program the coprocessor's firmware for almost unlimited applications (please call for a cost estimate for your requirements). Some hardware features available for a custom programmed coprocessor are: two 16 bit counter/timers, a serial port which can be used in synchronous or asynchronous mode, up to 12 I/O lines, and an analog comparator.

E-PAC 3000 G2 DIGITAL I/O

DIP SWITCH

The DIP switch has 7 switches which may be used for applications such as the selection of program options. The DIP switch is connected to the system data bus through a 74HC541 input buffer and is accessed through I/O, address 40H. The high order bit is used to read the SEEPROM data out line and should be ANDed off.

BUFFERED DIGITAL I/O

The buffered digital I/O lines, common to most E-PAC SBCs (E-PAC 1000, 2000, and 3000) boards share an EMAC standardized footprint. Header connector HDR4, carries eight optically coupled "open collector" high current digital outputs, and eight optically coupled digital inputs. The connector also carries +Vin and ground (which may be used as outputs to supply power to peripherals or as an input to supply power to the board), sixteen analog signal inputs, and analog system return ground. These analog and power connections will be described in more detail later. The connector can be plugged onto the E-PAC TERMINAL BOARD, or to a ribbon cable connector of the user's design.

HDR4

TERMINAL BOARD HEADER

1	2
+VIN	**+VIN**
GROUND	**GROUND**
INPUT 0 (PB.0)	**(PB.7) INPUT 7**
INPUT 1 (PB.1)	**(PB.6) INPUT 6**
INPUT 2 (PB.2)	**(PB.5) INPUT 5**
INPUT 3 (PB.3)	**(PB.4) INPUT 4**
OUTPUT 7 (PA.7)	**(PA.6) OUTPUT 6**
OUTPUT 5 (PA.5)	**(PA.4) OUTPUT 4**
OUTPUT 3 (PA.3)	**(PA.2) OUTPUT 2**
OUTPUT 1 (PA.1)	**(PA.0) OUTPUT 0**
ANALOG IN 15	ANALOG IN 14
ANALOG IN 13	ANALOG IN 12
ANALOG IN 11	ANALOG IN 10
ANALOG IN 9	ANALOG IN 8
ANALOG IN 7	ANALOG IN 6
ANALOG IN 5	ANALOG IN 4
ANALOG IN 3	ANALOG IN 2
ANALOG IN 1	ANALOG IN 0
ANALOG GROUND	ANALOG GROUND
(RESERVED)	(RESERVED)
39	40

BUFFERED DIGITAL OUTPUTSBUFFERED DIGITAL OUTPUTS

The E-PAC 3000 G2 has 8 buffered outputs; each output can be independently programmed to an on or off state. The "on" state is defined by the output being pulled to ground through the driver transistor (see Appendix B). The driver can sink up to 500 ma. in the on state. The "off" state is defined by the driver transistor being off and the pullup voltage selected by JP17 being present on the outputs.

JP17 **Buffered Digital Output Power and Ground Option Jumper.**

Positions A,B and C select the source for the buffered digital output pull-ups.

A +Vin from ST2 pin 1
B Isolated +V from HDR4A
C Vcc

Positions D and E select the Ground options
D Isolated ground from HDR4A
E Digital ground

The E-PAC 3000 G2 uses the ULN2803 Darlington driver chip as the output driver device. On a power-up reset, the ULN2803 outputs will go to an off state.

The ULN2803 is driven from the 8255 PPI. In the standard configuration, the A port is the output port, the B port is the input port and the C port is used as control for various I/O devices. Therefore the PPI should always be software configured for port A output, port B input and port C output. See appendix E for information on the 8255 PPI.

The eight digital outputs come from the "A" port of an 82C55 PPI peripheral chip (I/O address 100H) on the G2. The byte wide output goes into optocouplers which then drive an octal darlington driver IC. This darlington driver has eight darlington pair transistor drivers built into it, with built in thermal and current limiting. The base of each darlington is driven by the optocouplers, and the collectors go to the eight digital output pins on the digital I/O connector.

Through software, the PPI lines when set high (logic one) turn on the corresponding optocoupler which then turns on the driver, grounding the associated I/O connector output pin. Negative logic is used on the I/O header. A GROUND is the "ON" or logic one condition here. Note this connector output is NOT directly TTL compatible. The saturation voltage of the driver outputs is typically 0.9 volts, and as the TTL low level threshold is 0.8 volts, TTL logic cannot be guaranteed to work in all cases at this output port. This eight bit port is primarily intended to drive mechanical relays, LED's, small incandescent lights, SSR's etc. The PPI allows the user to read the output status of this port (any port configured for output) by inputting from it.

The main features of this output port are its high voltage, and high current drive capabilities. The outputs can stand off 50 volts DC, (off state) and can sink 500 mA. each (on state). However, there are some limitations due to the total package dissipation (2.25 watts) if all outputs are expected to operate simultaneously at high power.

Each of the eight outputs has a 10K resistor pullup. The common of this 10K resistor network is connected to positions A,B and C of JP17 (described earlier). The 10K resistors pull the digital output lines up to the selected voltage when they are OFF. The user may drive this OFF STATE voltage higher if desired by removing the jumper and connecting the external voltage source to the common of the resister network. There will be no ill effect caused by the pullup resistor being sourced to a lower voltage, as long as the driven device has a low impedance, as would be the case when a solenoid, relay coil, or incandescent lamp is involved.

The darlington driver IC has flyback diodes built into each output, but these are not connected in the 3000 G2, as clamping voltage conflicts may arise when multi-level outputs are driven by the 3000 G2. It is recommended that the user apply his own flyback diodes as required when driving inductive loads, such as solenoids or mechanical relays.

BUFFERED DIGITAL INPUTSBUFFERED DIGITAL INPUTS

The E-PAC 3000 G2 has 8 optically coupled inputs. When ground is present on any of the inputs, an internal LED is forward biased and turns on the optocoupler's output transistor. This will cause ground potential to be present at the input on the 8255 PPI B port (I/O address 101H). If the buffered input is left open or a high is present at the input, the LED remains off and the transistor is subsequently off. The input of the 8255 B port will then be pulled up to 5 Vdc. The inputs should not go below ground or above the input voltage. For more information on using the 8255 see Appendix E.

The phototransistor, when illuminated, places a ground at the associated input pin on PPI input port B. The phototransistor is illuminated by a corresponding LED, which is lit by the current (if any) flowing through the digital input pin(s). Current is supplied to each LED from a 1K ohm resistor, bussed to a common voltage select jumper on the board, JP16. If option B is selected the isolated +V must be in the 5 to 15 volt range.

JP16 Buffered Digital Input Pullup Voltage Option Jumper.

This selects the source for the buffered input pullups.

A	+Vin from ST2 pin 1
B	Isolated +V from HDR4A (must be 5 to 15 volts)
C	Vcc

The digital inputs are also logically similar to the outputs, in that a GROUND is the active state, and an OPEN or HIGH is the inactive state. These inputs are primarily intended for switch, pushbutton, or relay contact, etc. input. The loop current, therefore is normally supplied by the E-PAC, although many other configurations are possible.

Software that uses the buffered digital I/O port can read, modify, and rewrite the bit patterns on the digital outputs. It can only READ the digital inputs. Inputs on this port must be tightly polled in applications that must respond quickly to changes in inputs, no interrupt support is present on the PPI chip as used on the 3000 G2. Interrupt support is possible, however on the TTL I/O port described later.

TOTAL ELECTRICAL ISOLATION

In extremely electrically noisy environments, external inputs can introduce noise to the EPAC 3000G2 and possibly causing it to reset. To solve this problem, the computer needs to be electrically isolated from the noise of the outside world. HDR4A allows digital I/O with complete electrical isolation. It uses the same digital lines as HDR4 but external power and ground inputs are available (Isolated + and Isolated ground) instead of the normal power and ground connections. To isolate this header electrically, put jumpers in positions B and D (only) of JP17 and in position B (only) of JP16.

HDR4A

```
BUFFERED DIGITAL I/O HEADER
                1  2
    ISOLATED +  . .  ISOLATED GND
INPUT 0 (PB.0)  . . (PB.1) INPUT 1
INPUT 2 (PB.2)  . . (PB.3) INPUT 3
INPUT 4 (PB.4)  . . (PB.5) INPUT 5
INPUT 6 (PB.6)  . . (PB.7) INPUT 7
    ISOLATED +  . .  ISOLATED GND
OUTPUT 0 (PA.0)  . . (PA.1) OUTPUT 1
OUTPUT 2 (PA.2)  . . (PA.3) OUTPUT 3
OUTPUT 4 (PA.4)  . . (PA.5) OUTPUT 5
OUTPUT 6 (PA.6)  . . (PA.7) OUTPUT 7
               19   20
```

HDR4A is useful in that a 20 pin female header connector and ribbon cable can be plugged into it, and the other end of the ribbon can be split into two 10 pin cables. Two 10 pin female headers can be crimped on to these, resulting in a 10 pin connector with all the input lines and another with all the output lines and each having an isolated+ and isolated ground connection.

If complete isolation is not necessary and there is a need to supply power to the outside world through HDR4A, put jumpers in JP17 positions B, D, E. Also put a jumper in position A to supply +Vin, or C to supply Vcc. Never put jumpers in A and C at the same time, and never put jumpers in A or C when external voltage is being applied to Isolated +. This could damage your board and void the warranty.

PROGRAMMABLE DIGITAL I/O

The E-PAC 3000 G2 is equipped with 20 unbuffered TTL level programmable I/O lines. Each of these 20 lines can be individually programmed as inputs or outputs. These 20 lines are routed to a 50 pin header connecter (HDR2) that is standard I/O rack compatible. The Programmable Digital I/O is implemented using the KIO PIO ports A and B, and PIA port C (I/O addresses 80h, 82h, 8Ch respectively).

Note that port C bits 3, 4 and 7 also drive COM3 RTS, COM2 RTS and the optional LCD backlight control respectively. Since they are outputs normally they can be programmed as inputs without problems with contention. Remember, though, that the COM3 RTS, COM2 RTS and backlight will be controlled by the levels being input to these bits

The connector footprint of HDR2 is compatible with standard connection to I/O rack modules. The optional 3000 G2 D/A section output pins also reside in this header connector, at pin stations not normally used by the I/O rack modules. It has 20 TTL I/O line connections, 25 digital ground return lines, and two +5 volt DC pin connections. (It is advisable to provide separate supplies for external devices on this port, and not use 3000 G2 board power, unless they draw 100 Ma or less). This connector header also accepts the EMAC parallel printer adaptor board (E020-10). This small board allows the 3000 G2 to output to any standard parallel printer using a standard PC printer cable.

By virtue of the massive functional programmability of the KIO, the PIOA and PIOB pins can be programmed to produce an interrupt to the MPU upon the transition of a pin level or combination of pin levels, so tight polling of inputs is not required. Both the PIOA and PIOB ports can set to OR, AND, and don't care conditions on the port's input lines, allowing the generation of interrupts on hundreds of digital input combinations. See appendix E for further details.

HDR2

DIGITAL I/O HEADER

		1 2
	VCC	. .
	D/A CHANNEL A 2	. .
	D/A CHANNEL B 1	. .
	ANALOG GROUND	. .
(B.L. CTRL)	PORT C.7	. .
(COM2 RTS)	PORT C.4	. .
(COM3 RTS)	PORT C.3	. .
	PORT C.2	. .
	PORT B.7	. .
	PORT B.6	. .
	PORT B.5	. .
	PORT B.4	. .
	PORT B.3	. .
	PORT B.2	. .
	PORT B.1	. .
	PORT B.0	. .
	PORT A.7	. .
	PORT A.6	. .
	PORT A.5	. .
	PORT A.4	. .
	PORT A.3	. .
	PORT A.2	. .
	PORT A.1	. .
	PORT A.0	. .
	VCC	. .
		49 50

All even numbered pins are ground and Ports A,B and C are from the KIO.

ANALOG TO DIGITAL CONVERTER

The E-PAC 3000 G2 provides 16 analog input channels. The analog to digital conversion has 12 bit resolution (16 bit resolution is optional), and the conversion time to read a selected channel is 13 microseconds (3 microseconds for the supporting analog circuitry and 10 microseconds for the converter). The 3000 G2 I/O connectors HDR4 and HDR4B have the 16 input pins for the analog input system (note that HDR4B has some of the same pin descriptions as HDR4) . The HDR4 connector footprint is standard throughout the 1000-3000 E-PAC SBC cards. It is not mandatory to use the analog ground return that is available on these connectors, but it is recommended in order to achieve the best analog accuracy.

HDR4

	1 . . 2	
	+VIN . . +VIN	
	GROUND . . GROUND	
INPUT 0 (PB.0)	. .	(PB.7) INPUT 7
INPUT 1 (PB.1)	. .	(PB.6) INPUT 6
INPUT 2 (PB.2)	. .	(PB.5) INPUT 5
INPUT 3 (PB.3)	. .	(PB.4) INPUT 4
OUTPUT 7 (PA.7)	. .	(PA.6) OUTPUT 6
OUTPUT 5 (PA.5)	. .	(PA.4) OUTPUT 4
OUTPUT 3 (PA.3)	. .	(PA.2) OUTPUT 2
OUTPUT 1 (PA.1)	. .	(PA.0) OUTPUT 0
ANALOG IN 15	. .	**ANALOG IN 14**
ANALOG IN 13	. .	**ANALOG IN 12**
ANALOG IN 11	. .	**ANALOG IN 10**
ANALOG IN 9	. .	**ANALOG IN 8**
ANALOG IN 7	. .	**ANALOG IN 6**
ANALOG IN 5	. .	**ANALOG IN 4**
ANALOG IN 3	. .	**ANALOG IN 2**
ANALOG IN 1	. .	**ANALOG IN 0**
ANALOG GROUND	. .	**ANALOG GROUND**
(RESERVED)	. .	(RESERVED)
	39 40	

HDR4 B

1	2
o o	**ANALOG IN 0**
o o	**ANALOG IN 1**
o o	**ANALOG IN 2**
o o	**ANALOG IN 3**
o o	**ANALOG IN 4**
o o	**ANALOG IN 5**
o o	**ANALOG IN 6**
o o	**ANALOG IN 7**
o o	**ANALOG IN 8**
o o	**ANALOG IN 9**
o o	**ANALOG IN 10**
o o	**ANALOG IN 11**
o o	**ANALOG IN 12**
o o	**ANALOG IN 13**
o o	**ANALOG IN 14**
o o	**ANALOG IN 15**
o o	(RESERVED)
o o	(RESERVED)
o o	(RESERVED)
o o	**ANALOG GROUND**
39	40

All odd numbered pins are digital ground.

Analog Inputs can be configured to accept +2.5 to -2.5, +5 to -5 Vdc, and +10 to -10 Vdc (of course standard ranges such as 1 to 6 volts can also be measured in the +10 to -10 Vdc). To prevent damage, none of the analog inputs should exceed the supply rails. For example if the E-PAC 3000 G2 is powered by +12 Vdc (Vin = +12 Vdc) then the analog input voltage should not exceed +12 Vdc or fall below -12 Vdc. If there is a possibility that the analog inputs will exceed the recommended range or there is a chance of voltage spikes then the optional transient spike protection option (E010-02) should be used. The analog circuitry always provides the A/D convertor chip with signals in the ±10 volt range, no matter what range it is configured for, requiring it to have at least 2 volts of overhead voltage on the power supply (at least 12V). Without this, overhead full-scale voltage inputs will not be converted to full scale readings by the A/D convertor.

If the transient spike protection option (E010-02) was not ordered with the E-PAC 3000 G2, you may see a limitation with the standard Harris 506 multiplexers in that they do not always work correctly for supply voltages less than 10 volts DC (this problem is different from the lack of full-scale readings when powering the board at under 12V). In the Harris data sheets it does not specify a minimum supply voltage (but it does suggest that 8 volts DC is adequate). If your Vin supply voltage to the E-PAC 3000 G2 is less than 10 volts and strange analog readings are present, you have a couple of options. First you can set up your application software to access channel 15 several times a second (this seems to alleviate the problem) or you can replace the Harris 506 with the Harris 506A (the high voltage spike protected version) or the Intersal cross (IH6116/IH5116). If using a Terminal Board with the E-PAC 3000 G2, jumper out the 8 volt regulator that supplies the 3000 G2 with power. This will require that you provide a regulated and somewhat accurate supply to the Terminal Board.

ANALOG OPERATIONANALOG OPERATION

The analog input system's inputs first pass through an analog multiplexer chip, U48. This chip acts as a rotary switch. It picks out which of the sixteen inputs will be sent to the A/D converter. The multiplexer is controlled by address inputs sent to it from U41, the PPI chip, from Port C lines 0 to 3. The selected input is passed over to U46, which amplifies and scales the input voltage to a ±10 volt full scale input to the A/D converter chip, U44. The A/D chip is a BURR-BROWN ADS7804 (or an optional 16 bit ADS7805).

Software written for the A/D input system should select which input is to be measured, by setting the analog multiplexer via PPI Port C, waiting 4 microseconds for the input to settle, and then initiating a conversion by writing a dummy value to one of the A/D registers (addresses 180H or 181H). The conversion will be completed and ready to read in 10 microseconds. If only one analog channel is to be read without interruption,

the 4 microsecond settling time is not required which will allow for faster readings. Note that since the SEEPROM uses some of the same port lines as the analog multiplexer, mixing analog channel reads with SEEPROM accesses will inadvertently cause the multiplexer to change channels. When this happens, the 3 microsecond settling time is required prior to the next conversion.

Upon completion of a conversion, the DAV line on the A/D goes low and can be polled by checking bit 6 of KIO PIA Port C (I/O address 8CH). When DAV goes low, read the low and high bytes of the A/D (address 180H for the low byte or 181H for the high byte). Reading the high byte of the conversion will cause the DAV line to go high again. The following values will be returned based on the conversion voltage and the resolution of the A/D (full scale is normally 5 volts).

	12 bit A/D		**16 bit A/D**	
	high	**low**	**high**	**low**
+ full scale	7F	F0	7F	FF
	7F	E0	7F	FE
	:	:	:	:
	00	10	00	01
base voltage (0V)	00	00	00	00
	FF	F0	FF	FF
	:	:	:	:
	80	10	80	01
- full scale	80	00	80	00

Note that with the 16 bit A/D the values returned are in 2's complement form so that a negative voltage gives a negative number. On a 12 bit A/D it is the same, however the value is returned in steps of 16 for each count. To convert the value to 1 step per count, the value must be shifted as a 16 bit word, 4 places to the right. To retain the 2's complement form, the sign must be extended (after shifting, the upper 4 bits should be made same as the MSB of the original 16 bit word).

ANALOG CALIBRATION

The A/D range is factory calibrated to the +10V to -10V DC range. This range allows the conversion of any voltage between +10 V and -10 V. For example, if the desired voltage range is 0 to 2.5 Vdc, no jumper or calibration changes would be required since this is within the factory set range, though the full resolution of the A/D would not be used.

In some applications the full resolution must be used, so in these situations the analog voltage ranges can be changed in order to achieve maximum resolution. EMAC can factory adjust the E-PAC 3000 G2 to any range for a small charge, or by following the instructions below it can be changed by the customer.

When changing the analog input voltage range, jumper JP18 must be configured to the desired range as shown below:

JP18

5V span:	Shunt only pins 1 and 2 together
10V span:	Shunt only pins 2 and 3 together
2.5V span:	Shunt only pins 3 and 4 together

After changing the jumper setting, the calibration will be slightly off, so the analog circuitry should be recalibrated to achieve accurate readings. Analog channels cannot be independently configured, so all 16 analog channels will be configured to the same input voltage range. If different voltage ranges and scales are required, use the EMAC Multi-Voltage Board (E022-05). Each board allows you to individually control the voltage ranges and scales of 4 channels.

The calibration procedure involves the setting of the two multi-turn potentiometers. The first pot (VR1) controls the shift and the second pot (VR2) controls the span. They do not change the shift or span very much, and should not be relied upon to change the basic ranges of the A/D system. Two analog input voltages are required in order to calibrate the analog circuitry. The first is the base voltage which is the lowest positive voltage supported by the chosen range (analog ground). The second is the full scale voltage, which is the largest voltage supported by the chosen range (+2.5 Vdc, +5 Vdc, or +10 Vdc). The accuracy of these two voltage will have a direct effect on the accuracy of the A/D readings. For best results provide stable voltages with accuracy better than the accuracy you wish to achieve.

To calibrate, connect the base voltage to analog channel #0 and the full scale voltage to analog channel #1. Software should be written to read both channels and display their outputs repetitively in hexadecimal. While viewing the outputs adjust the shift pot until channel #0 returns the

base value. Now adjust the gain pot until channel #1 reads the full scale value. Repeat these adjustments until both the base and full scale voltages read correctly. Depending on the accuracy and stability of the calibration voltages, some digital count flutter may be seen. If flutter exists, calibrate to an average of the counts seen. When fully calibrated, it is suggested that some type of sealer be put on the pots to prevent them from going out of adjustment.

DIGITAL TO ANALOG CONVERTER

The 3000 G2 has an optional 2 channel, 12 bit resolution D/A programmable output system. The D/A chip U34, is an ANALOG DEVICES part, AD7549. It accepts digital codes from the MPU buss, and produces a current output, which is converted to a voltage by an op-amp then scaled to a -5 to +5 volts DC output. The D/A system has tweaking pots, similar in function to those in the A/D section, to trim the zero code and full scale code analog output voltages. There are two trim pots for each of the two channels.

For applications that need a bipolar output, jumpers JP9A and JP9B provide a bipolar shift by installing a jumper at that position. The bipolar shift causes the 0-10 volt unipolar output to become a -5 to +5 volt bipolar output.

The jumper option is field alterable by merely placing or removing a header jumper at the station(s) required. The stations are labeled "A" and "B". Without a jumper in place, channel A or B will have a unipolar, 0 to 10 volt output, 12 bits of resolution. With a jumper in place at A or/and B, that channel will have a bi-polar, -5 to +5 volt output. The SPAN is always 10 volts, the jumper merely slides the output down 5 volts, and the bit resolution remains the same.

The two D/A output channels may be set for unipolar or bipolar operation independently, and the tweaking pots for each channel are also independent. Like the A/D system, factory calibration and pot sealing are performed at 0 - 10 volts DC. The other setting is checked for tolerance, but should field application require a different setting, field re-calibration may be necessary.

Unlike the A/D system, no multiplexing takes place. Both outputs are continuous as per the output code sent to them, and one can be changed without affecting the output of the other. The D/A outputs are present at connector header HDR2, at pin stations not used by the digital I/O rack standard.

When the D/A is set to the unipolar 0-10 volt range, the D/A requires the same voltage overhead as the A/D system requires. At least 12 volts DC should be used as a minimum power supply input for the D/A output to reach the full 10 volts at the output.

The D/A chip is accessed through the I/O map, by writing three four bit nibbles to data addresses in the chip (I/O addresses C0H - C2H for channel A, and C4H - C7H for channel B). Upon writing the most significant nibble, the 12 bit code is broadside loaded into the D/A output register for that channel, to produce a low glitch output.

The D/A is reset to zero code whenever a hardware reset occurs. This means the output will default to 0 if the channel is optioned for unipolar, or the output will be at -5 volts by default if that channel is set to bi-polar.

TIMERS AND COUNTERS

The E-PAC 3000 G2 comes equipped with two 16 bit timers and four 8 bit timer/counters. The two 16 bit timers are resident in the HD64180/Z180 microprocessor. By loading a user programmable termination count, time intervals from microseconds to tenths of seconds are available. When the termination count is reached, an interrupt can then be issued to the MPU. The timer can also be set up to reload itself or to stop counting upon reaching the termination count. In either case, an interrupt can be issued. The timer interrupts are internally connected and controlled. The timer status can also be checked in a polled mode by reading the Timer Control Register.

These timers (TIMER0/PRT0, TIMER1/PRT1) are 16 bit down counters that count the timer input pulses and issues a HD64180/Z180 timer interrupt when the terminal pulse is reached. The user can reprogram the length of the count before the termination pulse is reached if so desired. The user can also determine the timer interval by programming the counter register from values 2H to FFFFH. The source of timer input pulses is the system clock divided by 20 (307.2KHz for a clock frequency of 6.144 MHz and 614.4KHz for a clock frequency of 12.288 MHz).

These timers are ideal as an external program interval timers. If you wish to perform a software operation at a specific time interval, then the

timer/counter can be programmed to that interval. Upon the resulting timer interrupt your program can execute the desired software.

TIMER1/PRT1 is equipped with an added timer out pin. Actually this pin perform double duty as a trade off pin with address line A18. EMAC went to special effort to free this line for use as a timer output. This line can be programmed high, low, or toggled at each reload of the timer. The timer output line when toggled produces a 50% duty cycle square wave and can drive one of the other counter/timers if so desired. This line when used in the high/low mode can also trigger or gate (with external circuitry) one of the timer/counters. The output is available at pin 2 of the HDR3 connector.

The KIO's CTC unit, (Counter Timer Circuit) has four, 8 bit counters/timers. These counter/timers may be used as counters as well as timers as their name implies. Each counter/timer has a unique I/O address for input, output, and control input. The four independently programmable channels of the CTC satisfy common control system requirements for event counting, interrupt and interval timing, and general clock rate generation. CTC2 and CTC3 (TIMER5 and TIMER6) are used to generate baud rates for SIOA and SIOB. If these communications ports are not in use then their associated counter/timers are free to be used for other timing functions.

Register KIO command, at I/O address 08E hex, is used to set the Daisy chain interrupt priority order, to reset individually any of the PIO, SIO, or CTC units, and to control the PIA.

The KIO's CTC provides the 3000 G2 with four additional timers. However, their function is quite tricky. Each timer/counter can be set and used independently. Each one has an eight bit counter that counts down to zero from the initial loaded count. When they reach zero, they output a pulse equal to one half the clock period. They can not be set to produce a square wave output. The A18/TOUT pin of the MPU can do this but it cheats us out of an address line, and 512 K of memory.

If a CTC channel is used as a timer, it counts only the system clock signal, through a programmable prescale of 16 or 256. As the system clock is 6.144 or 12.288 mhz, these timers don't take long to time out. To use the timer/counter in this mode, select the timer function with auto trigger.

Each counter/timer can be set to start with an external gate pulse, and the gate polarity can be set to rising or falling edge trigger, otherwise the timer can be set to reload and retrigger automatically. Each timer/counter can be set to merely count input pulses, once again the polarity of the count trigger is selectable. Each timer/counter has two hardware access pins. These pins all go to a header connector, HDR3. HDR3 is for hardware access to the four timer/counters in the KIO, and the TOUT of the MPU. CTC0 and CTC1 each have an input function pin available on HDR3, called CLK/TRIG. The function of this input will be the CLOCK pin if that timer/counter is set for the counter function, or as the trigger pin if the timer/counter is set to the timer function. Both CTC2 and CTC3 have special positions on HDR3 to allow jumpering of their CLK/TRIG inputs to a signal that is 1/4 the crystal frequency. This is necessary when they are used as baud rate clocks for the SIO.

When a timer/counter is used as a counter, the counter will decrement from the value loaded into it, until it is clocked down to zero. The clock edge polarity can be set by writing the appropriate code to it's control register. When the counter is decremented to zero, it stops counting, and the output pin for that counter, ZC/TO pin (Zero Count) goes high. At the same time an interrupt for that counter will occur, if its interrupt was enabled.

When a timer/counter is used as a timer, the system clock (from the MPU) is used as the clocking source by default. The CLK/TRIG input pin now functions as a gate start for the timer, if so enabled. This gate may be used to start timing at a specific externally synchronized event. The timer's clock input from the MPU can be set in software to be prescaled by either 16 or 256, before it gets to the timer. As in the counter mode, when the timer decrements to zero, the ZC/TO output goes high, and will produce an interrupt if so enabled. However, the timer can be set in software to automatically reload and restart, unlike the counter mode, which simply stops at zero. In that case, the output at the ZC/TO pin will be a brief pulse as the counter reloads.

Whether in the timer or counter modes, the number of counts must be loaded into the timer's, Time Constant register for that timer/counter. When interrupts are used, an interrupt vector must be loaded into timer/counter 0 (CTC0) interrupt vector register. This vector will be the base vector address and all timer/counter channels will be offset from it, generating a unique vector for each timer/counter.

The actual count within the timer/counter can be read at any time by inputting from the timer Control Word register. The timer/counters will only output however, when they have decremented to zero.

To have longer time periods, the timer/counters may be cascaded in hardware. To do this, jumper one timer/counter's ZC/TO pin to the next one's CLK/TRG pin, then by software set up the first timer/counter to the timer mode, with auto reload enabled, and set the next one, and any after that (to cascade more than 2 timer/counters), to the counter mode. Because a timer/counter is always clocked by prescaled system clock when it is in the timer mode, all cascaded stages must be set to counter mode in order to work properly. Also, since counters do not

automatically reload, the counters must have re-load interrupt handlers installed and enabled in order for that counter to cascade to others.

Counter/timer outputs TC2 and TC3 are wired directly to the SIO units Channel A and Channel B data clocks, respectively. These timer/counters are dedicated to providing the serial data clocks required by COM2 and COM3 (SIOA and SIOB). As long as these serial ports are not in use at the time, TC2 and TC3 may be used for other timer functions. If serial data communication is desired, however, only TC0 and TC1 are totally free. See appendix E for further details on programming the Programmable Reload Timers.

E-PAC 3000 G2 INTERRUPTS

The 3000 G2 MPU system supports many interrupts, most of them internal to the HD64180/Z180 and the Z84C90 KIO, plus three external hardware interrupts. The HD64180/Z180 MPU supports 12 interrupt groups, 4 of which are external. Out of the four MPU external interrupts, one of them (INT0) is fed directly by the KIO chip, which has it's own interrupt controller, and a large number of interrupt sources. Finally, the three remaining MPU external interrupts go directly to terminations on the board to provide hardware access to them.

The interrupts of the MPU are arranged in a fixed priority. They will be described in the same order as their priority.

1. TRAP

The TRAP interrupt is an internally define interrupt. It occurs when an undefined opcode is fetched. Software can use this interrupt for purposes of error detection or software debugging. This interrupt in non-maskable.

2. NMI

The NMI* interrupt is a non-maskable hardware interrupt. It is activated when the pin input edge is active low. The input must remain low for the MPU to acknowledge this interrupt. NMI* cannot de disabled through software. To maintain compatibility with existing EMAC SBC boards, which use an active high hardware input for NMI, an inventer (U12F) is placed ahead of the NMI* pin on the MPU, making the NMI input connection to the 3000 G2 a positive true input. An RC filter comprised of C7 and R6 help prevent noise spikes produced outside the 3000 G2 from false triggering of the NMI input. The NMI interrupt input is accessible via screw terminal ST1, terminal 1. It is TTL/MOS level compatible.

3. INT0

The MPU's INT0 interrupt input is wired directly to the KIO chip on the 3000 G2. This interrupt can be programmed for 3 unique interrupt modes, however it must be programmed in software to interrupt mode 2, for use by the KIO chip. The KIO uses the Zilog "daisy chain" method of interrupt expansion. No other access is given to INT0, as the KIO monopolizes this interrupt itself.

For Mode 2 interrupt handling, a interrupt vector table contains the address of the interrupt handler(s) that each interrupt will vector to. The handler addresses are pointed to by the addition of the interrupt vector high byte, and an interrupt low byte supplied by the interrupting device, in this case the KIO chip. The interrupt vector high byte is determined by the content of MPU register I. The I register must be set in software via the LD A,I Z80 type instruction. This register content then locates the table along 256 byte blocks within the address space.

The interrupting device will assert MPU signal INT0 low, and when the MPU gets around to servicing this interrupt, it will assert IOEN* and LIR* (LIR* is roughly equivalent to signal M1 in Z80 jargon) together, indicating an interrupt acknowledge. This interrupt acknowledge causes the device (KIO) to pass a vector onto the data bus, which the MPU uses as the low order vector table address. The interrupt acknowledge is then de-asserted, and the MPU pushes the program counter onto the stack, and jumps to the interrupt handler,s address found in the table.

The KIO provides a unique interrupt vector for each interrupt source, 14 in all.

Upon completion of each interrupt handler, the RETI (RETurn from Interrupt) instruction causes the MPU to return from that interrupt, restore the program counter from the stack, and inform the interrupting device that service is complete.

Zilog interrupt structure uses a daisy chain system, that allows their MPU's only one interrupt hardware pin. All peripheral chips have an INT* output pin, an IEI (interrupt input), and an IEO (interrupt output) pin. All INT* pins connect in parallel, and when any device requests interrupt service, this one line is asserted low. At the same time, it's IEO pin, normally high, also drops low. The interrupt priority of Zilog peripherals is set in hardware by connection of the IEI's and IEO's one to another in series. The peripheral of highest priority has it's IEI line connected to Vcc,

and the next priority device has it's IEI line driven by the first devices' IEO line, and so on, down to the lowest priority device.

The peripheral who is interrupted first, gets first interrupt opportunity. That device, when acknowledged, drops it's IEO line, which will prohibit lower priority peripherals from interrupting this interrupt. However, those peripherals of higher priority can interrupt (preempt) the current interrupt.

The RETI Z80 type instruction is a specialized type of RETURN. The standard return merely restores the stack and program counter. The RETI instruction does the same, but also informs the Zilog type peripheral that its interrupt is over with. The Zilog type peripherals are "smart", in that they decode the MPU instruction flow in parallel with the MPU, looking for the RETI instruction. They do this with the assistance of MPU signal M1. Machine cycle 1, is the opcode fetch cycle of Zilog MPUs. Signal M1 tells all peripherals, "the opcode is being fetched now, so all you peripherals listen carefully". The HD64180/Z180 MPU does not use M1, but provides an equivalent signal, called LIR*, (Load Instruction Register) which is used by Zilog type devices for the same purpose as M1.

The interrupting peripheral that currently has control of the service will read the RETI opcode, and know that it is time to raise it's IEO line, permitting lower priority devices to ask for interrupt service. This action is separate from the interrupt acknowledge, which already has occurred by the LIR* and IOE* signal acknowledgement. This RETI sequence is specific to the act of restoring the interrupt daisy chain alignment.

When a higher priority interrupt finishes after preempting a lower priority interrupt, the lower priority interrupt is given the opportunity to continue. When the lower priority interrupt is complete, he can pull the daisy chain, and flush the interrupts down, so other lower priority interrupts can be acknowledged.

The KIO is a super integration VLSI chip that contains the Zilog PIO (Parallel Input Output), SIO (Serial Input Output), CTC (Counter Timer Circuit), and KIO specific units. The KIO has a control register in it used to set the interrupt priorities among the various peripherals. The internal daisy chain then goes out one interrupt pin to the MPU's INT0 interrupt input.

INT0 may be masked by software, using the internal mask register in the MPU. The INT0* pin is active low. It must be held low until acknowledged, then it must be immediately released high or another interrupt will occur. As this pin is directly connected to only the KIO chip, this hardware requirement is automatically met.

4. INT1

5. INT2

INT1 and INT2 (referred to as INT0 and INT1, respectively, in the HDR1 I/O Expansion Connector description) also use the same vector table lookup method used by INT0, but the input pin function cannot be changed. They are always used in a mode similar to interrupt mode 2. Their pin inputs to the MPU are also active low, but inverters are placed ahead of them on the 3000 G2 to provide hardware compatibility with existing EMAC SBCs. These interrupt lines both go to the Expansion Connector header HDR1, for use by EMAC expansion peripherals or user defined add on boards. If the optional coprocessor is installed, it will use INT2 to interrupt the main processor. In this configuration do not connect external interrupt sources to the HDR1 INT2 pin (referred to as INT1) .

Their interrupt vectors come from the IL register in the MPU, accessible via software (I/O address 33H). The IL register takes the place of the hardware that otherwise places the low vector onto the data bus. The IL vector joins up with the I register to point to the required interrupt handler code. All interrupt vectors for INT1, INT2 and KIO interrupt handlers should be neatly arranged in this table. Both INT1 and INT2 are software maskable.

6. Timer 0
7. Timer 1
8. DMA channel 0
9. DMA channel 1
10. Clocked Serial I/O port
11. Asynchronous SCI channel 0
12. Asynchronous SCI channel 1

These remaining interrupts are all internal to the MPU. The MPU contains two timers, to asynchronous serial communication ports, two DMA channels, and one synchronous serial port. All these devices, when enabled, produce a unique interrupt vector response into the vector table, which must contain the associated interrupt handler address. All hardware interface is taken care of internally. All these interrupts may be enabled/disabled through software via configuration registers.

APPENDIX A

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APPENDIX B

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APPENDIX C

E-PAC 3000 G2 Rev. 3 JUMPER DESCRIPTIONS

The E-PAC 3000 G2 has configuration jumpers to permit selection of certain hardware parameters for the board.

JP1 and JP2 RS422/485 Terminating Resistor Jumpers.

Jumpers inserted in JP1 and JP2 enable terminating resistors for the receiver and transmitter, respectively.

JP3 Optional Coprocessor UART Redirection Jumper.

This selects the source of data for the optional coprocessor's UART receive line. In position 1-2 the receiver gets data from the RS-232 converter chip. In position 2-3, the data comes from CN4 pin 5.

JP4 Watchdog Timer Jumper.

The watchdog timer is normally enabled for use with EMAC operating system software. The watchdog timer will automatically hardware reset the 3000 G2 if it is not periodically triggered by software. Should some form of interference cause the software to crash, it is unlikely the watchdog will be properly retriggered, and it will time out, causing a reset. After this reset, the system can reinitialize.

When the jumper is in position A, the watchdog is pulsed by bringing bit 6 of port C (I/O address 102h) low and then high. When in position B it is pulsed by simply writing a dummy value to I/O address 240h.

In some cases, such as when a microprocessor emulator unit is used, or custom software is written that does not have the proper drivers built in, the watchdog timer function can become an annoyance. Removing the jumper will disable the watchdog timer, and the board will only reset on power up, or an external pushbutton reset input.

JP5-JP7 U19 Configuration jumpers.

JP5 controls pin 1 of memory socket U19. Position A selects 5V for EPROM Vpp and Position B selects A18 for flash.

JP6 controls pin 31 of memory socket U19. Position A selects WE* for flash and Position B selects A18 for a 512K EPROM.

JP7 controls pin 30 of memory socket U19. Position A selects 5V for Vcc on the 27C512 EPROM and Position B selects A17 for flash.

JP8-JP10 Memory Map Configuration Jumpers.

JP8 determines whether A18 will be included in the memory mapping. Position A leaves it out of the map and allows A18 to be used in the TOUT function, limiting the memory map to 512k total. Position B includes A18 in the memory map allowing up to 1 meg.

JP9 selects how much memory will be used by socket U19. Position A limits U19 to a maximum of 128k. Position B allows greater that 128k (up to 512k). To avoid contention and ensure proper operation do not put a device in socket U20 if JP10 is in position A and JP9 is in position B since in this jumper configuration U20 shares

the same memory space as U19.

JP10 selects how much memory will be used by socket U20. Position A limits U19 to a maximum of 128k. Position B allows greater that 128k (up to 512k). To avoid contention and ensure proper operation do not put devices in sockets U21 or U22 at the same time a device is in U20 if JP10 is in position B since in this jumper configuration U20 shares the same memory space as U21 and U22.

JP11 U20 Configuration Jumper.

This controls pin 30 of memory socket U20. Position A selects 5V for Vcc on a 32K RAM and Position B selects A17 for 512k RAMs

JP12 External status input Jumper.

This is normally a wire jumper soldered into position A. It is used in custom boards without A/D as a external status input.

JP13 Graphic LCD Interface Font Size Selector Jumper.

The table below shows the jumper settings for different font sizes.

	MD2	**FS1**
6X8 Font	LO	HI
8X8 Font	HI	LO

JP14 Negative Voltage Source Jumper.

Putting jumpers in positions A-B and C-D enables use of the on-board negative voltage charge pump. A jumper in position D-E only, enables the external -V input on ST2 pin 4.

JP15 5V Source Jumper.

Putting jumpers in positions A-B and C-D enables use of the on-board 5V regulator. A jumper in position D-E only, enables the external 5V input on ST2 pin 5.

JP16 Buffered Digital Input Pullup Voltage Option Jumper.

This selects the source for the buffered input pullups.

A	+Vin from ST2 pin 1
B	Isolated +V from HDR4A
C	Vcc

JP17 Buffered Digital Output Power and Ground Option Jumper.

Positions A,B and C select the source for the buffered digital output pullups.

A	+Vin from ST2 pin 1
B	Isolated +V from HDR4A
C	Vcc

Positions D and E select the Ground options

D	Isolated ground from HDR4A
E	Digital ground

JP18 Analog Input Voltage Range Jumper.

Jumper 1-2 for 5V span, 2-3 for 10V and 3-4 for 2.5V.

JP19 Digital to Analog Output Voltage Range Jumper.

The presence or absence of a jumper in position A enables a -5 to +5 volt span or 0 to 10V span, respectively, for D/A channel A. Similarly, the presence or absence of a jumper in position B enables a -5 to +5 volt span or 0 to 10V span, respectively, for D/A channel B.

APPENDIX D

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E-PAC 3000 G2 I/O MAPPING

The E-PAC 3000 G2 I/O Decoder Selects from 640 unique I/O addresses, from the 64K available on the 64180/Z180, and provides chip selects to various I/O devices external to the 64180/Z180 MPU. The 64180/Z180 reserves 40 HEX I/O addresses internally (64 decimal) for use in its own extensive internal I/O architecture. The internal I/O map can be relocated by software but upon reset defaults to 00 HEX to 3F HEX. The E-PAC 3000 G2 I/O decoder also decodes these I/O addresses, but no devices are connected as these addresses are reserved by the 64180/Z180. The E-PAC 3000 G2 I/O Decoder, decodes nine evenly spaced I/O chip selects, at 40 HEX increments. They are as follows:

MPU INTERNAL I/O

ADDRESS	FUNCTION
00 hex	ASCI Control Register A Ch 0
01 hex	ASCI Control Register A Ch 1
02 hex	ASCI Control Register B Ch 0
03 hex	ASCI Control Register B Ch 1
04 hex	ASCI Status Register Ch 0
05 hex	ASCI Status Register Ch 1
06 hex	ASCI Transmit Data Register Ch 0
07 hex	ASCI Transmit Data Register Ch 1
08 hex	ASCI Receive Data Register Ch 0
09 hex	ASCI Receive Data Register Ch 1
0C hex	Timer Data Register Ch 0 low byte
0D hex	Timer Data Register Ch 0 High byte
0E hex	Reload Register Ch 0 Low byte
0F hex	Reload Register Ch 1 High byte
10 hex	Timer Control Register
0A hex	CSI/O Control Register
0B hex	CSI/O Transmit/Receive Data Register
14 hex	Timer Data Register Ch 1 low byte
15 hex	Timer Data Register Ch 1 high byte
16 hex	Reload Register Ch 1 low byte
17 hex	Reload Register Ch 1 high byte
18 hex	Free Running Counter
20 hex	DMA Source Address Register Ch 0 low byte
21 hex	DMA Source Address Register Ch 0 high byte
22 hex	DMA Source Address Register Ch 0 bank byte
23 hex	DMA Destination Address Register Ch 0 low byte
24 hex	DMA Destination Address Register Ch 0 high byte
25 hex	DMA Destination Address Register Ch 0 bank byte
26 hex	DMA Byte Count Register Ch 0 low byte
27 hex	DMA Byte Count Register Ch 0 high byte
28 hex	DMA Memory Address Register Ch 1 low byte
29 hex	DMA Memory Address Register Ch 1 high byte
2A hex	DMA Memory Address Register Ch 1 bank byte
2B hex	DMA I/O Address Register Ch 1 low byte
2C hex	DMA I/O Address Register Ch 1 high byte
2E hex	DMA Byte Count Register Ch 1 low byte
2F hex	DMA Byte Count Register Ch 1 high byte
30 hex	DMA Status Register

31 hex	DMA Mode Register
32 hex	DMA/WAIT Control Register
33 hex	IL Register (Interrupt Vector Low)
34 hex	INT/TRAP Control Register
36 hex	Refresh control Register
38 hex	MMU Common Base Register
39 hex	MMU Bank Base Register
3A hex	MMU Common/Bank Area Register
3E hex	Operation Mode Control Register
3F hex	I/O Control Register

E-PAC 3000 G2 I/O Hardware Addresses

ADDRESS	**FUNCTION**
40 hex	Dipswitch port (read only)
80 hex	KIO PIO Port A Data
81 hex	KIO PIO Port A Command
82 hex	KIO PIO Port B Data
83 hex	KIO PIO Port B Command
84 hex	KIO CTC Channel 0
85 hex	KIO CTC Channel 1
86 hex	KIO CTC Channel 2
87 hex	KIO CTC Channel 3
88 hex	KIO SIO Channel A Data
89 hex	KIO SIO Channel A Command/Status
8A hex	KIO SIO Channel B Data
8B hex	KIO SIO Channel B Command/Status
8C hex	KIO PIA Port C Data
8D hex	KIO PIA Port C Command
8E hex	KIO Internal Command
C0 hex	DAC A Channel low nibble
C1 hex	DAC A Channel middle nibble
C2 hex	DAC A Channel high nibble
C3 hex	DAC A Channel load command
C4 hex	DAC B Channel low nibble
C5 hex	DAC B Channel middle nibble
C6 hex	DAC B Channel high nibble
C7 hex	DAC B Channel load command
100 hex	PPI Port A Data
101 hex	PPI Port B Data
102 hex	PPI Port C Data
103 hex	PPI Control Register
140 hex	LCD port command register
141 hex	LCD port data register
180 hex	ADC Data/Control low byte
181 hex	ADC Data/Control high byte
182 hex	ADC Control Mode low byte

183 hex ADC Control Mode high byte

1C0 through 1FF
E-PAC 1000, 2000, 3000 and G2 expansion boards

200 hex Graphic LCD data register
201 hex Graphic LCD command/status register

240 through 27F
Writing to any of these addresses will pulse the watchdog if JP4 is in position B.

Consider all unspecified I/O device addresses in this range as reserved addresses.

The bit mapping of the E-PAC ports are found in the following table, the bitmaps of the 64180/Z180 MPU, 84C90 KIO, and ML2230 are found in Appendix E.

PPI PORT A: Standard General Purpose Buffered Output Port.

PPI PORT B: Standard General Purpose Optically Coupled Input Port.

PPI PORT C: Used to control E-PAC internal functions as follows:

Bit 0 Wired to A/D systems's multiplexer bit 0 and to SEEPROM Serial Clock pin. As the SEEPROM and the A/D are not likely to be used simultaneously, this is a multi-function bit.

Bit 1 Wired to A/D system's multiplexer bit 1 and to SEEPROM Data IN pin. Also a multi-function bit.

Bit 2 Wired to A/D system's multiplexer bit 2 only.

Bit 3 Wired to A/D system's multiplexer bit 3 only.

Bit 4 Wired to SEEPROM Chip Select.

Bit 5 Attention output to the optional coprocessor

Bit 6 Watchdog timer pulse bit, PWDTN.

Bit 7 Output to reset optional coprocessor

KIO PORT A: General purpose Port all 8 bits available.

KIO PORT B: General purpose Port all 8 bits available.

KIO PORT C: Used to provide control lines for the RS422/485 port and handshaking lines for SIOA and SIOB. Bit 6 reads the A/D DAV line.

Bit 0 Network TXEN bit. When set, enables the optional RS-422/485 network driver to transmit mode.

Bit 1 Network ATTEN bit. When set high (with network output enabled) drives the EMAC net option to activate the "attention" state.

Bit 2 SIO B, Data Terminal Ready line (DTR).

Bit 3 SIO B, Request To Send line (RTS).

Bit 4 SIO A, Request To Send line (RTS).

Bit 5 SIO A, Data Terminal Ready line (DTR).

BIT 6 Active low A/D Data AVailable line (DAV*).

Bit 7 LCD backlight enable.

APPENDIX E

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APPENDIX F

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