EPAC 3000

BOARD REVISION 2

HARDWARE REFERENCE MANUAL

MANUAL
REVISION 1.0

DISCLAIMER

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INTRODUCTION

We at EMAC hope that you will find the EPAC 3000 to be as powerful and useful as we do. Please carefully read this manual before and during operation of your new single board computer.

The EPAC 3000 board was designed to maximize the amount of control and monitor features available on a single printed circuit board. This industrial strength computer is packed with features you might expect to find on a multi-board system. The EPAC 3000 comes equipped with 16 analog to digital channels, 8 optically coupled digital inputs, 8 buffered digital outputs, 20 programmable I/O lines, watchdog timer and more.

STANDARD FEATURES

CENTRAL PROCESSING UNIT
Hitachi's HD64180 CMOS microprocessor running at 6.144 MHz.

INPUTS/OUTPUTS
8 optically coupled digital inputs, 8 buffered digital outputs (high current drive) and 16 channels of 8 bit A/D all available on a 40 pin header I/O. Twenty programmable TTL level I/O lines on a standard I/O rack compatible connector. Also, there is a single TTL level input and TTL level output available.

MEMORY
Memory space for 64K to 128K of EPROM and for 32K to 384K of static RAM. Total combined EPROM and RAM memory space is 512k. A 1K bit EEPROM is also included.

POWER SUPPLY
Single voltage supply +8 to +15 Vdc. with on board regulation.

TIMERS
Watchdog timer (a hardware reset will occur if software does not periodically access the timer), and two programmable 16 bit timers with interrupt support. One timer has a programmable TTL level output

COMMUNICATIONS
Two RS-232 ports come standard, one of which can be optionally replaced by a full duplex RS-422/485 port.

SOCKETS
High reliability machined sockets for Memory IC's.

EXPANSIBILITY
50 pin header connector for use with expansion boards.

SETTING UP YOUR EPAC 3000

EMAC's EPAC 3000 has most everything you need to start programming your monitor and control application. Listed below is additional information helpful in setting up your EPAC 3000.

POWER REQUIREMENTS

A single +8 to +15 Vdc. power supply is required, a negative supply is produced on board by a DC to DC converter. The DC to DC converter automatically produces a negative voltage which tracks the positive voltage used to power the board. The maximum current draw of the EPAC 3000 is 150 ma. in its standard configuration.

Connect the + volts lead of the power supply to pin 1 and the ground lead to pin 2 of the screw terminal connector ST2, refer to Appendix C "Component Layout".

NOTE: +15 Volts DC is the maximum input voltage allowed. An input voltage of +12 Vdc. is recommended whenever possible.

EXTERNAL HARDWARE RESET

A screw connection for an external reset is provided on the EPAC 3000. To generate an external reset, connect ground to the external reset input, pin 2 of screw terminal connector ST1, using a switch, relay, or logic device. If a logic device is used, it must be able to safely sink 13 ma. of current. See Appendix B "External Reset Drawing" and the "Component Layout" drawing in Appendix C. for connection points.

SERIAL COMMUNICATIONS PORTS

Two RS-232 communication ports are provided as part of your EPAC 3000. RS-232 negative supply voltage is generated by the DC to DC converter on the EPAC 3000. Connection to the COM0 RS-232 port is provided via the screw terminal connector (ST1), and connection to the COM1 RS-232 port is provided via the DB-9 connector, see the "Component Layout" drawing, in appendix C. E-FORTH and MTBASIC use COM1 for standard default communications.

The COM0 and COM1 ports are both implemented in the HD64180 microprocessor. These asynchronous serial ports provide full duplex serial communication at software selectable Baud Rates of 300 to 38400 Baud. To set the baud rate the correct prescale value (divide by 10 or 30) and the correct divide ratio must be selected. These values are chosen depending on the baud rate desired and the clock frequency the processor is operating at. The Asynchronous Serial Communications Interface (ASCI) Control Register B is used to set the baud rate. In addition to setting the baud rate, the number of bits, the type of parity, and the number of stop bits must be selected. These parameters are set by ASCI Control Register A. See appendix E for more information on the ASCI.

The ASCI serial port 0 is the EPAC 3000 port COM 1 and ASCI serial port 1 is the EPAC 3000 COM 0. Both of these serial ports have the provision to be used in an interrupt mode or a polled mode. To use the ASCI in the interrupt mode, first enable the interrupts using the ASCI Status Register and "EI" instruction and provide the software interrupt handlers at the software selectable vector. In the polled mode of operation for reception, check bit 7 (RDRF) of the ASCI Status Register. If this bit is high then there is a byte available for reading. This byte can be read from the ASCI Receive Data Register. For transmission, check bit 1 (TDRE) of the ASCI Status Register. If this bit is high then the transmit buffer is empty a byte may be written to the ASCI Transmit Data Register.

An optional RS-422/485 replacement of the COM0 RS-232 port is available. The RS-422/485 port can be used as a full or half duplex port. Up to 32 similar ports may share the same communication lines. To prevent contention especially when used as a half duplex port, care must be taken to assure that only one port transmits at a time. The system automatically powers up in the receive mode. To transmit, set PPI #1 port A line 5 high. To receive, set the same line low. The RS-422/485 option is necessary when using ENET. Communication cables are available as an accessory from EMAC.

COM1 has the handshake lines CTS and RTS available. To read the CTS line (pin 8 of COM1) examine bit 4 of PPI #0 port C. To control the RTS line (pin 7 of COM1) , set or reset bit 6 of PPI #1 port A. Note that the RS-232 converter chip inverts the signals read from CTS and written to RTS.

PROGRAMMING THE EPAC 3000

EMAC offers optional resident E-FORTH or MTBASIC (Multi-Tasking control BASIC) compiler/operating systems which can greatly increase software productivity. These operating systems provide all the features of a high level operating system but are oriented for monitor/control applications. If the user has E-FORTH or MTBASIC, all interaction between the operating system and the user is through a dumb terminal or PC terminal emulator. EMAC has terminal emulator software that runs on IBM PCs and compatibles. This software includes a menu driven terminal program with file download and upload capability as well as Intel Hex file creation for EPROM programming.

The EPAC 3000 can also run programs written in Assembly language or any other language producing 8080/Z80 or 64180 executable code. Third party cross assemblers and cross compilers are available for the EPAC 3000. These Tools allow the development of code to take place on the IBM PC using languages such as "C". Contact EMAC for a list of third party vendors.

STANDARD I/O OF THE EPAC 3000

DIGITAL OUTPUTS

The EPAC 3000 has 8 buffered outputs; each output can be independently programmed to an on or off state. The "on" state is defined by the output being pulled to ground through the driver transistor (see Appendix B). The driver can sink up to 300 ma. in the on state. The "off" state is defined by the driver transistor being off, allowing the output to go to the level selected by JP3. Position B of JP3 allows the level to go up to VIN (the voltage applied at the power connector ST2), position A allows +5V, or if the jumper is removed the output will be open.

JP3	OUTPUT AT OFF STATE
A	+ 5V
B	+ VIN
(no jumper)	open

Jumper JPX enables diodes in the driver chip, to protect it from the flyback current of inductive loads, such as relays.

The EPAC 3000 uses the ULN2803 Darlington driver chip as the output driver device. In the power up state, the ULN2803 outputs will go to an off state (5V., the input voltage, or open, jumper selectable).

The ULN2803 is driven from the 8255 PPI #0. In the standard configuration, the A port is the output port, the B port is the input port and the upper half of the C port is used as an input for various I/O devices. Therefore PPI #0 should always be software configured for port A as output, port B as input and upper half of port C as input. The lower half of port C is user definable and accessible

through HDR2. See appendix E for information on the 8255 PPI.

There is a TTL level digital output on pin 4 of HDR3 which is controlled by changing bit 7 of PPI #1 port A (this port must be configured to output).

DIGITAL INPUTS

The EPAC 3000 has 8 optically coupled inputs (see Appendix B). When ground is present on any of the inputs, an internal LED is forward biased and turns on the optocoupler's output transistor. This will cause ground potential to be present at the input on the 8255 PPI #0's B port. If the input is left open or a high is present at the input, the LED remains off and the transistor is subsequently off. The input of the 8255 B port will then be pulled up to 5V. NOTE: If the input voltage pull-up option is used, then approximately 14 ma. of sink current is required. If the 5 volt pull-up option is used, then 7 ma. of sink current is required. The inputs should not go below ground or above the input voltage. For more information on using the 8255 see Appendix E.

JP2	INPUT PULL-UP VOLTAGE	REQUIRED SINK CURRENT
A	+5V	7ma
B	+VIN	14ma

There is a TTL level digital input on pin 5 of HDR3 which is examined by reading bit 7 of PPI #0 port C (the upper half of this port must be configured as input).

PROGRAMMABLE DIGITAL I/O

The EPAC 3000 is equipped with 20 unbuffered TTL level programmable I/O lines. These lines can be programmed as all inputs, all outputs, or virtually any combination of input/output. These 20 lines are routed to a 50 pin header connecter (HDR2) that is standard I/O rack compatible. The programmable digital I/O is implemented using PPI #1, Ports B and C and the lower half of port C on PPI #0. When configuring ports 1B and 1C care should be taken to assure that PPI Port 1A is always configured as a output port. When configuring the lower half of port C on PPI #0, as described earlier, PPI #0 should always be configured for port A as output, port B as input and upper half of port C as input. See Appendix A "Auxiliary I/O Connector Pin Out" for a detailed description.

ANALOG INPUTS

The EPAC 3000 provides 16 multiplexed analog input channels. For the standard 8 bit A/D, the conversion time to read a selected channel is 150uS and you may configure the inputs to accept 1 to 6V, 0 to 2.5V, 0 to 5V, and 0 to 10V. Do not apply negative voltages to the inputs when using the 8 bit A/D.

The optional 12 bit plus sign A/D convertor allows you to convert negative voltages and it has a faster conversion time. The conversion time to read a selected channel is 35uS. Analog Inputs can be configured to accept 1 to 6V, +2.5V to -2.5V, +5V to -5 V, and +10V to -10V.

To prevent damage, no analog input should exceed the supply rails. For example if the EPAC 3000 is powered by +12 Vdc (Vin = +12 Vdc) then the analog input voltage should not exceed +12 Vdc or fall below -12 Vdc. If there is a possibility that the analog inputs will exceed the recommended range or there is a chance of voltage spikes then the optional Transient Spike Protection (part # E010-02) should be used.

The Analog circuitry requires some overhead voltage, so the board should be powered by a supply that is at least 2 volts greater than the absolute value of the maximum negative input voltage, and at least 2 volts greater than the maximum positive input voltage. For example if 6 Vdc is the largest input voltage converted then at least a +8 Vdc power supply should be used, or if the maximum

negative input is -10 and the maximum positive input is 8 then the at least a 12 Vdc power supply should be used.

ANALOG VOLTAGE RANGES

The jumpers JP4 and JP5 select the voltage ranges for the A/D. All 16 analog channels will be configured to the same input voltage range. Analog channels cannot be independently configured. After configuring the jumpers, the analog circuitry must be recalibrated to achieve accurate readings (calibration is discussed later).

In the table below, only the positive voltage is given, even though the 12 bit A/D option allows negative also. For example, selecting the 10V span gives a range of -10V to 10V.

JP4 A/D VOLTAGE SPAN: Absence or presence of jumpers selects the voltage range for A/D.

PINS 1&2 MUST BE JUMPERED TOGETHER ON JP5 A & B TO ENABLE THE FOLLOWING RANGES

	JP4 A	JP4 B
2.5V	PRESENT	PRESENT
5V	ABSENT	PRESENT
10V	ABSENT	ABSENT

For 1-6 volt range select the 5V span as shown above but jumper pins 2 and 3 on JP5 A and B.

In the 1 to 6V range an analog input of 1V should produce a conversion value of 0, and an analog input of 6V should produce the maximum value for the A/D convertor (FF hex for 8 bit and FFF hex for 12 bit). This voltage range is used by EMAC's signal conditioning cards.

The +2.5V to -2.5V range gives the highest resolution of all ranges offered. With the 12 bit A/D an analog input of -2.5V will produce a conversion value of F000H. From -2.5V, each additional 0.61 mv will increase the digital count by 1 until at 0V when the count reads 0. From 0V, each additional 0.61 mv will increase the digital count by 1 until at 2.5V the count reads 0FFFH. This range achieves the highest resolution of all ranges offered.

ANALOG CALIBRATION

If the 12 bit A/D option is installed, a pre-calibration procedure is recommended to achieve accurate analog readings. This procedure involves self calibrating the A/D converter itself. This procedure should be used as part of the power up code. Self calibrating the A/D is a simple procedure, done through software. Writing a 04 to the Control Lowbyte Register (182h) causes the A/D to self calibrate. The end of calibration, is indicated by bit 5 of PPI #0 port C going low. See appendix E for more information on the ML2230 A/D converter.

The second procedure is required for both types of A/D, but only if reconfiguring the A/D input voltage range from its factory settings. This procedure involves the setting of the two multi-turn potentiometers on the EPAC 3000 board. The first pot (R48) controls the shift and the second pot (R47) controls the gain. Two voltages are required in order to calibrate the analog circuitry. The first is the base voltage which is the lowest positive voltage supported by the chosen range (analog ground or +1V). The second is the full scale voltage, which is the largest voltage supported by the chosen range (+2.5V, +5V, +6V, or +10V). The accuracy of these two voltage will have a direct effect on the accuracy of the A/D readings. For best results provide stable voltages with accuracy better then the accuracy you wish to achieve.

To calibrate connect the base voltage to analog channel #0 and the full scale voltage to analog channel #1. Software should be

written to read both channels and display their outputs repetitively. While viewing the outputs adjust the shift pot until channel #0 reads the base voltage. Now adjust the gain pot until channel #1 reads the full scale voltage. Repeat these adjustments until both the base and full scale voltages read correctly. Depending on the accuracy and stability of the calibration voltages, some digital count flutter may be seen. If flutter exists calibrate to an average of the counts seen. A thorough understanding of the analog circuitry is recommended before adjusting the calibration pots. EMAC can factory adjust the EPAC 3000 to any range prior to shipment.

ANALOG OPERATION

Each analog input is fed through an analog multiplexer and then into the analog to digital converter. PPI #1 port A bits 0-3 select the desired channel of the analog multiplexer. To allow for the settling time of the multiplexer, wait 40uS before starting the conversion.

When using the standard 8 bit A/D, the conversion may be started by writing to I/O Address 180H. With the 12 bit A/D option, sample and hold is integrated within the A/D convertor package to maintain high accuracy. Once the channel has been selected the A/D can be started which will automatically close the door on the sample and hold. An output to I/O Address 180H starts the A/D converter.

The A/D can be interrupt driven using INT2. Upon completion of the conversion, the convertor brings the INT2 line low causing an interrupt to occur, if the interrupt has been enabled. The A/D also has the provision to be used in a polled mode by examining bit 5 of PPI #0 port C. When the bit goes from high to low, the conversion is complete.

When the conversion is complete, you may read port 180h to get the result. If using the 12 bit A/D, you should also read port 181h to get the high byte of the conversion.

For added accuracy EMAC has provided a separate Analog Ground input on screw connector ST2 pin 3. While use of this input is not mandatory, EMAC does recommend its use to achieve best analog accuracy.

DIGITAL TO ANALOG OUTPUTS

This option provides 4 channels of 8 bit D/A. The presence or absence of jumpers in positions 1, 2 or 3 of JP6 configures the output voltage ranges for the D/A channels collectively.

JP6D/A OUTPUT RANGE:

	D/A OUTPUT VOLTAGE RANGE			
	0 - 5	**1 - 5**	**1 - 6**	**0 - 6**
POSITION 1	absent	absent	present	present
POSITION 2	present	absent	absent	present
POSITION 3	absent	present	present	absent

The writing a 0 to a D/A channel gives the minimum voltage of the selected range and writing FF hex gives the maximum voltage in the selected range.

8 BIT D/A CHANNEL	**PORT ADDRESS**
CHANNEL 0	C0 hex
CHANNEL 1	C1 hex
CHANNEL 2	C2 hex
CHANNEL 3	C3 hex

OTHER FEATURES OF THE EPAC 3000

MEMORY SECTION

The EPAC 3000 has four memory slots of 128K each. A total of 512K of memory space is available, excluding the 128 bytes located in the 93C46 EEPROM. The memory map is as follows:

SOCKET #	START - END	DEVICE
U6	0:0000 - 1:FFFF	EPROM
U7	2:0000 - 3:FFFF	RAM
U8	8:0000 - 9:FFFF	RAM
U9	A:0000 - B:FFFF	RAM

Note that for RAMs or EPROMs that are less that 128k the memory is mapped multiple times within the 128k space. For example memory addresses 0:0000 - 0:FFFF of a 64k EPROM in socket U6 will also be mapped to memory addresses 1:0000 - 1:FFFF. A 32k RAM in socket U7 will be mapped at 2:0000 - 2:7FFF, 2:8000 - 2:FFFF, 3:0000 - 3:7FFF and 3:8000 - 3:FFFF.

EPROM

Memory socket U6 accepts EPROMs only. EPROM devices with access times of 200 nS or lower (faster) have been found to function reliably with the EPAC 3000 with standard speed. As the EPROM industry is always producing faster and faster chips as their standard product, almost any chip you buy new will easily satisfy the speed requirements. Most EPROMs manufactured today start as low as 150 nS access time, making them suitable even for boards with the high speed option.

A 128K byte device (27C1001A) or a 64K byte device (27C512) may be used. The 27C1001A devices are 32 pin ICs that plug directly into memory socket 1. However, the 27C512 is a smaller sized 28 pin device. This chip should be placed with its notch aligned with that of the socket but leaving socket pins 1,2,31 and 32 unoccupied, and the rest filled (this is called the ground justified position).

Note:The 27C1001A EPROM is different from the 27C1000A device. The pinouts for the two devices differ for signals A16, and output enable. For this reason the 27C1000A EPROM will not work in the EPAC 3000.

RAM

Memory sockets U7, U8 and U9 accept 32k or 128k static RAMs with 120nS access times, or faster. Since the 32k devices are only 28 pins and the sockets are 32 pins, they must be inserted in the ground justified position as defined in the EPROM section. Some popular RAMs are as follow:

32k DEVICES
NEC uPD 43256A
HITACHI HM62256
MOSEL MS62256L

128 DEVICES
NEC uPD 431000
HITACHI HM62812

EMAC has available "smart sockets" which may be plugged into the MICROPAC 180 RAM socket, with the RAM chip plugged into them, to provide battery backup of the RAM. These "smart sockets" have power monitors and lithium batteries built into them, which supply standby power to the RAM device when the board is powered down. Only low power RAMs should be plugged into the "smart socket".

EEPROM

The EEPROM (93C46) is 1K bit in size providing 64, sixteen bit words of nonvolatile memory. This EEPROM is not in the memory map, but is accessed serially. To utilize the EEPROM, complex control and data signals must be provided, so use the EEPROM driver code listed in appendix F. See appendix E for further information on the 93C46.

WATCHDOG TIMER

The purpose of the watchdog timer is to provide an automatic hardware reset if the program that is currently running crashes. For example, if noise generated from a lightning strike or a power fluctuation causes the program to run erratically, in most cases the watchdog will generate a hardware reset. This can be very useful in field applications where a reset could correct a software failure. The watchdog timer line must be pulsed by the software no less than once every 0.8 seconds. The watchdog is pulsed by toggling the microprocessor's RTS0 output line. This line is controlled through internal I/O register CNTLA0 (I/O port 00) bit 4. In the E-FORTH and MTBASIC operating systems the watchdog access is handled automatically during development and in application programs. Care should be taken not to pulse the watchdog timer from within an interrupt routine, as this lessens the effectiveness of the watchdog timer.

The watchdog timer can be enabled/disabled if so desired using JP1. The disable position is marked "DS" and enable is marked "EN" (see appendix C, "Component Layout Drawing").

TIMERS

The EPAC 3000 comes equipped with two 16 bit timers which are resident in the HD64180/Z180 microprocessor. By loading a user programmable termination count, time intervals from microseconds to tenths of seconds are available. When the termination count is reached, an interrupt can then be issued to the MPU. The timer can also be set up to reload itself or to stop counting upon reaching the termination count. In either case, an interrupt can be issued. The timer interrupts are internally connected and controlled. The timer status can also be checked in a polled mode by reading the Timer Control Register.

These timers (TIMER0/PRT0 and TIMER1/PRT1) are 16 bit down counters that count the timer input pulses and issue a HD64180/Z180 timer interrupt when the terminal pulse is reached. The user can reprogram the length of the count before the termination pulse is reached if so desired. The user can also determine the timer interval by programming the counter register from values 2H to FFFFH. The source of timer input pulses is the system clock divided by 20 (307.2KHz for a clock frequency of 6.144 MHz and 460.8KHz for a clock frequency of 9.216MHz).

These timers are ideal as an external program interval timers. If you wish to perform a software operation at a specific time interval, then the timer/counter can be programmed to that interval. Upon the resulting timer interrupt your program can execute the desired software.

TIMER 1 (PRT1) has a TTL level output called TOUT available on pin 2 of HDR3. This output can be programmed by writing to bits 2 and 3 of the timer control register (TCR) at address 10h. TOUT is affected as follows:

```
ICR BITS #
3  2  TOUT FUNCTION
0  0  TOUT functions as the A18 line and becomes high when addresses 4:0000 to
             7:FFFF are accessed (there is no memory in this range).
0  1  Toggle output when timer data register 1 (TMDR1) counts down to 0
```

```
1  0  Output goes low when TMDR1 counts down to 0
1  1  Output goes high when TMDR1 counts down to 0
```

E-FORTH and MTBASIC have built-in timer program commands. See appendix E for further details on programming the Programmable Reload Timers.

EXPANSION CONNECTOR

The EPAC 3000 has a 50 pin expansion connector (HDR1) which provides additional expansion capabilities. Primarily, this connector gives access to the Data bus, Address bus and Control lines. See Appendix A "Expansion Connector Pin Out" for a detailed description.

NOTE:EMAC has modular expansion boards available for this connector.

OPTIONAL ON BOARD HARDWARE FEATURES

SOFTWARE

E-FORTH and MTBASIC are available as resident operating systems/compilers. E-FORTH has an Assembler, Editor, Overlays, and Target Compiler. MTBASIC has multitasking capabilities, floating point math and window support. E-FORTH and MTBASIC both includes high-level control, monitor, engineering, and real time features. High and low level Interrupt support is also featured.

12 BIT PLUS SIGN A/D

The analog to digital conversion has 12 bit plus sign resolution with sample/hold, and the conversion time to read a selected channel is ≈35 microseconds. Analog Inputs can be configured to accept 1 to 6V, +2.5 to -2.5, +5 to -5V, and +10 to -10V.

ANALOG SPIKE PROTECTION

The EPAC 3000 analog multiplexer may be upgraded to have several hundred volts of transient spike protection. This IC is installed at the factory if requested.

DIGITAL TO ANALOG CONVERTER

Four channels of 8 bit D/A can be configured to output 0-5, 1-5, 0-6 or 1-6 volts.

REAL TIME CLOCK CALENDAR

The EPAC can be equipped with a real time clock/calendar (RTC). The RTC contains a lithium energy cell which maintains clock information and RAM memory data. The clock keeps time in hundredths of seconds, seconds, minutes, hours, day of week, date of month, month and year. The month and year determine the number of days in each month. If you have the E-FORTH or MTBASIC operating systems, also refer to their manualsl for programming instructions. This option can be installed at any time by the user or at the factory before shipping.

NONVOLATILE RAM (RAMDISK)

EMAC has 32k and 128k RAMDISKs available for source code or data storage. The RAMDISK has a built-in lithium energy cell which maintains data in RAM memory. The RAMDISKs normally reside in memory sockets 2, 3, and 4. Source code or data can be stored in the RAMDISK for later use. The RAMDISK may be removed from the EPAC and replaced at a later time without loss of memory which allows the RAMDISK(s) to be removed/inserted much like floppy disks. The E-FORTH and MTBASIC operating system fully supports the operation of the RAMDISK.

EXTERNAL OPTIONS FOR EPAC SYSTEMS

TERMINAL BOARD: A perfect board for terminating all those I/O connections.

SIGNAL CONDITIONING CARDS: A low cost method of implementing Analog I/O.

EPROM PROGRAMMER BOARD: A simple solution to burning application programs.

PROGRAMMABLE 32 LINE PARALLEL BOARD: For 32 additional lines of programmable digital I/O. do.

LCD-KEYPAD BOARD: An economical method of interactive communication.

PARALLEL PRINTER BOARD: For printing data or whenever a hard copy is needed.

SUPPORT SOFTWARE: When your EPAC needs to communicate to your PC.

FOR MORE INFORMATION ON THE ABOVE ITEMS JUST GIVE US A CALL.

APPENDIX A

THIS APPENDIX IS NOT AVAILABLE IN PDF FORMAT

APPENDIX B

EPAC 3000 Rev. 2 JUMPER DESCRIPTIONS

JP1 **WATCHDOG TIMER:** Position EN enables, DS disables.

JP2 **OPTOISOLATOR INPUT PULL-UP VOLTAGE:** Position A for +5V, or B for +VIN.

JP3 **BUFFERED DIGITAL OUTPUT PULL-UP VOLTAGE:** Position A for +5V, or B for +VIN.

JPX **BUFFERED DIGITAL OUTPUT CLAMP DIODE ENABLE**: Jumpering this enables the internal clamp diodes to protect the output driver from the flyback current of inductive loads, such as relays.

JP4 **A/D VOLTAGE SPAN:** Absence or presence of jumpers selects the voltage range for A/D.

	JP4 A	JP4 B
2.5V	PRESENT	PRESENT
5V	ABSENT	PRESENT
10V	ABSENT	ABSENT

JP5 **A/D BASELINE SHIFT:** This jumper selects the baseline voltage for the A/D

	PINS TO JUMPER ON JP5 A & B
0V	1-2
1V	2-3 (This will only be accurate if the A/D voltage span is 5 volts)

JP6D/A OUTPUT RANGE: The presence or absence of jumpers in positions 1, 2 or 3 selects the output range for all 4 of the optional D/A channels.

	D/A OUTPUT VOLTAGE RANGE			
	0 - 5	**1 - 5**	**1 - 6**	**0 - 6**
POSITION 1	absent	absent	present	present
POSITION 2	present	absent	absent	present
POSITION 3	absent	present	present	absent

APPENDIX C

EPAC 3000 MEMORY and I/O MAPPING

MEMORY:

SOCKET #	START - END	DEVICE
U6	0:0000 - 1:FFFF	EPROM 27C512 (64K) OR 27C1001A(128K)
U7	2:0000 - 3:FFFF	RAM
U8	8:0000 - 9:FFFF	RAM
U9	A:0000 - B:FFFF	RAM

32K RAMS	128K RAMS
NEC uPD 43256A	NEC uPD 431000
HITACHI HM62256	HITACHI HM628128
MOSEL MS62256L	

Note that for RAMs or EPROMs that are less that 128k the memory is mapped multiple times within the 128k space. For example memory addresses 0:0000 - 0:FFFF of a 64k EPROM in socket U6 will also be mapped to memory addresses 1:0000 - 1:FFFF. A 32k RAM in socket U7 will be mapped at 2:0000 - 2:7FFF, 2:8000 - 2:FFFF, 3:0000 - 3:7FFF and 3:8000 - 3:FFFF.

I/O MAPPING:

I/O Decoder Selects from 512 unique I/O addresses, from the 64K available on the 64180/Z180, and provides chip selects to various I/O devices external to the 64180/Z180 MPU. The 64180/Z180 reserves 40 HEX I/O addresses internally (64 decimal) for use in it's own extensive internal I/O architecture. The internal I/O map can be relocated by software but upon reset it defaults to 00 HEX to 3F HEX.

MPU INTERNAL I/O ADDRESSES

ADDRESS	FUNCTION
00 hex	ASCI Control Register A Ch 0
01 hex	ASCI Control Register A Ch 1
02 hex	ASCI Control Register B Ch 0
03 hex	ASCI Control Register B Ch 1
04 hex	ASCI Status Register Ch 0
05 hex	ASCI Status Register Ch 1
06 hex	ASCI Transmit Data Register Ch 0
07 hex	ASCI Transmit Data Register Ch 1
08 hex	ASCI Receive Data Register Ch 0
09 hex	ASCI Receive Data Register Ch 1
0C hex	Timer Data Register Ch 0 low byte
0D hex	Timer Data Register Ch 0 High byte
0E hex	Reload Register Ch 0 Low byte
0F hex	Reload Register Ch 1 High byte
10 hex	Timer Control Register

0A hex CSI/O Control Register
0B hex CSI/O Transmit/Receive Data Register

14 hex Timer Data Register Ch 1 low byte
15 hex Timer Data Register Ch 1 high byte
16 hex Reload Register Ch 1 low byte
17 hex Reload Register Ch 1 high byte

18 hex Free Running Counter

20 hex DMA Source Address Register Ch 0 low byte
21 hex DMA Source Address Register Ch 0 high byte
22 hex DMA Source Address Register Ch 0 bank byte
23 hex DMA Destination Address Register Ch 0 low byte
24 hex DMA Destination Address Register Ch 0 high byte
25 hex DMA Destination Address Register Ch 0 bank byte
26 hex DMA Byte Count Register Ch 0 low byte
27 hex DMA Byte Count Register Ch 0 high byte
28 hex DMA Memory Address Register Ch 1 low byte
29 hex DMA Memory Address Register Ch 1 high byte
2A hex DMA Memory Address Register Ch 1 bank byte
2B hex DMA I/O Address Register Ch 1 low byte
2C hex DMA I/O Address Register Ch 1 high byte
2E hex DMA Byte Count Register Ch 1 low byte
2F hex DMA Byte Count Register Ch 1 high byte
30 hex DMA Status Register
31 hex DMA Mode Register
32 hex DMA/WAIT Control Register

33 hex IL Register (Interrupt Vector Low)
34 hex INT/TRAP Control Register
36 hex Refresh control Register

38 hex MMU Common Base Register
39 hex MMU Bank Base Register
3A hex MMU Common/Bank Area Register

3E hex Operation Mode Control Register
3F hex I/O Control Register

EPAC 3000 PORTS

PPI #1 PORT A Address 80 hex: must be an output port

Bit 0. Analog mux bit 0, and SEEPROM serial clock.
Bit 1. Analog mux bit 1, and SEEPROM write data.
Bit 2. Analog mux Bit 2.
Bit 3. Analog mux bit 3.
Bit 4. SEEPROM chip select. (enable)
Bit 5. Network TXEN lead.
Bit 6. RS-232 Handshake output.
Bit 7. TTL output to pin 4 of HDR3.

PPI #1 PORT B Address 81 hex: programmable as input or output
Bits 0 through 7 are all direct TTL leads to header connector HDR2.

PPI #1 PORT C Address 82 hex: programmable as input or output
Bits 0 through 7 are all direct TTL leads to header connector HDR2.

PPI #0 PORT A: Address 100 hex: must be an output port
Bits 0 through 7. All outputs to buffered digital outputs.

PPI #0 PORT B: Address 101 hex: Must be an input port
Bits 0 through 7. All inputs from buffered digital inputs.

PPI #0 PORT C: Address 102 hex: Bits 4-7 must be inputs and bits 0-3 are programmable as input or output.

Bit 0. TTL I/O bit 16 available on HDR2
Bit 1. TTL I/O bit 17 available on HDR2
Bit 2. TTL I/O bit 18 available on HDR2
Bit 3. TTL I/O bit 19 available on HDR2
Bit 4. CTS line (pin 8 of COM1)
Bit 5. A/D conversion complete polling bit (conversion complete = 0)
Bit 6. Serial EEPROM data receive bit.
Bit 7. TTL input from pin 5 of HDR3.

8 BIT A/D CONV.: Address 180 hex: Writing to this port starts the conversion, reading this port returns the conversion value and brings the INTR line high.

OPTIONAL PORTS

12 BIT A/D PORTS (see data sheets for detailed description)

DATA LO BYTE:	Address 180 hex
DATA HI BYTE:	Address 181 hex
CONTROL LO BYTE:	Address 182 hex
CONTROL HI BYTE:	Address 183 hex

8 BIT D/A PORTS

CHANNEL 0	Address C0 hex
CHANNEL 1	Address C1 hex
CHANNEL 2	Address C2 hex
CHANNEL 3	Address C3 hex

APPENDIX D

THIS APPENDIX IS NOT AVAILABLE IN PDF FORMAT

APPENDIX E

THIS APPENDIX IS NOT AVAILABLE IN PDF FORMAT

APPENDIX F

EPAC 3000 ASSEMBLY LANGUAGE DRIVERS

```
; This sub-routine will pulse
; the Watchdog timer
; No parameters
;
WTCHDG  PUSH  PSW
        PUSH  BC
        LD    BC,102h     ;PORT C
        IN    A,(C)
        AND   0BFH
        OUT   (C),A
        OR    60H
        OUT   (C),A
        POP   BC
        POP   PSW
        RET
;
;                               INITIALIZATIONS
;
CLD     DI
        LD    A,10H       ; ONE I/0 WAIT ZERO MEMORY WAIT
        OUT0  WAITS,39h

        LD    A,82H       ; INITIALIZE PPI'S
        LD    BC,103h     ; IOCREG
        OUT   (C),A
        LD    A,9BH
        LD    BC,143h     ; IOCREG1
        OUT   (C),A

        XOR   A
        OUT   36h,A       ; REFCON - TURN REFRESH OFF

        LD    BC,182h     ; ADCCON
        LD    A,1         ; CALIBRATE A/D
        OUT   (C),A
        LD    A,4
        OUT   (C),A

; SET COM PORTS TO 9600 BAUD, NO PARITY, 1 STOP BIT
        LD    A,74H
        OUT   00,A        ; OUT0 (M),G - SERCOMA
        OUT   01,A        ; SRCOMA1
        LD    A,02H       ;
        OUT   02,A        ; SERCOMB
        OUT   03,A        ; SRCOMB1

        LD    A,0F8H      ; MMU INITIALIZATION
        OUT   3Ah,A       ; CBAR
        LD    A,08H
```

```
        OUT   39h,A       ; BBR
        OUT   38h,A       ; CBR
        RET

;
;                                EEPROM DRIVERS
;

; Select EEPROM
; used by other sub-routines
; No parameters
;
CSON    PUSH  BC
        PUSH  PSW
        LD    BC,102h     ;PORT C
        IN    A,(C)
        OR    10H
        OUT   (C),A
        POP   PSW
        POP   BC
        RET
;
; Make EEPROM Clock High
; used by other sub-routines
; No parameters
;
CLKHI   PUSH  BC
        PUSH  PSW
        LD    BC,102h     ;PORT C
        IN    A,(C)
        OR    01H
        OUT   (C),A
        POP   PSW
        POP   BC
        RET
;
; Make EEPROM Clock Low
; used by other sub-routines
; No parameters
;
CLKLO   PUSH  BC
        PUSH  PSW
        LD    BC,102h     ;PORT C
        IN    A,(C)
        AND   0FEH
        OUT   (C),A
        POP   PSW
        POP   BC
        RET
```

```
;
; Write A0 to EEPROM
; used by other sub-routines
; No parameters
;
DAT1    PUSH  BC
        PUSH  PSW
        LD    BC,102h     ;PORT C
        IN    A,(C)
        OR    02H
        OUT   (C),A
        POP   PSW
        POP   BC
        RET
;
; Write A1 to EEPROM
; used by other sub-routines
; No parameters
;
DAT0    PUSH  BC
        PUSH  PSW
        LD    BC,102h     ;PORT C
        IN    A,(C)
        ANI   0FDH
        OUT   (C),A
        POP   PSW
        POP   BC
        RET
;
; Deselect EEPROM
; used by other sub-routines
; No parameters
;
CSOFF   PUSH  BC
        PUSH  PSW
        LD    BC,102h     ;PORT C
        IN    A,(C)
        AND   0EFH
        OUT   (C),A
        POP   PSW
        POP   BC
        RET
;
; Provide 1 clock cycle to EEPROM
; used by other sub-routines
; No parameters
;
CLKIT   CALL  CLKHI
        CALL  CLKLO
        RET
```

```
;
; Provide 3 clock cycles to EEPROM
; used by other sub-routines
; No parameters
;
CK3     PUSH  BC
        PUSH  PSW
        LD    BC,102h     ;PORT C
        IN    A,(C)
        OR    01H
        OUT   (C),A
        AND   0FEH
        OUT   (C),A
        OR    01H
        OUT   (C),A
        AND   0FEH
        OUT   (C),A
        OR    01H
        OUT   (C),A
        AND   0FEH
        OUT   (C),A
        POP   PSW
        POP   BC
        RET
;
; Read 1 bit of EEPROM
; used by other sub-routines
; No parameters
;
DINAT   PUSH  BC
        LD    BC,140h     ; PORT1A
        IN    A,(C)
        AND   80H
        RLCA
        POP   BC
        RET
```

```
;
; Write 1 word (16 bits at preselected address) to EEPROM
; Parameters H/L contains word to be written
; used by other sub-routines
;
SERPSH  LD    E,8H
        LD    A,H
SERPSH0 RLCA
        JPNC  SERPSH1
        CALL  DAT1
        JP    SERPSH2
SERPSH1 CALL  DAT0
SERPSH2 CALL  CLKIT
        DEC   E
        JPNZ  SERPSH3
        LD    A,L
SERPSH3 DEC   D
        JPNZ  SERPSH0
        CALL  DAT0
        RET
;
; Read 1 word (16 bits at preselected address) to EEPROM
; Parameters leave 16 bit EEPROM value in H/L reg pair
; used by other sub-routines
;
SERPOP  LD    D,14
        LD    E,7H
        LD    L,0H
SERPOP0 CALL  CLKIT
        CALL  DINAT
        OR    L
        RLCA
        LD    L,A
        DEC   E
        JPNZ  SERPOP1
        CALL  CLKIT
        CALL  DINAT
        OR    L
        LD    H,A
        LD    L,0
SERPOP1 DEC   D
        JPNZ  SERPOP0
        CALL  CLKIT
        CALL  DINAT
        OR    L
        LD    L,A
        CALL  CLKIT
        RET
```

```
;
; Write Enable EEPROM
; used by other sub-routines
; No parameters
;
WREN    LD    HL,4C00H
        LD    D,0BH
        CALL  CSON
        CALL  SERPSH
        CALL  CSOFF
        CALL  CK3
        RET
;
; Write Disable EEPROM
; used by other sub-routines
; No parameters
;
WRDIS   LD    HL,4000H
        LD    D,0BH
        CALL  CSON
        CALL  SERPSH
        CALL  CSOFF
        CALL  CK3
        RET
;
; Write EEPROM
; Parameter Input: H/L contains Address
; Parameter Input: B/C contains Data
;
WREE    DI
        CALL  CSON
        LD    D,0EH       ; 4 DUMMY, 4 HEADER, AND 6 ADDRESS
        LD    A,L
        RLCA              ; SHIFT ADDRESS TO MSBIT
        RLCA
        LD    L,A
        LD    H,05H       ; HEADER
        CALL  SERPSH
        LD    H,B         ; DATA
        LD    L,C
        LD    D,10H       ; 16 DATA
        CALL  SERPSH
        CALL  CSOFF
        CALL  CK3
        CALL  CSON
WREE0   CALL  CLKIT
        CALL  DINAT
        OR    A
        JPZ   WREE0
        CALL  CSOFF
        CALL  CK3
```

```
        EI
        RET;


; Read EEPROM
; Parameter  Input: H/L contains Address
; Parameter Output: H/L contains Data after Execution
;
RDEE    DI
        CALL  CSON
        LD    D,0EH       ; 4 DUMMY, 4 HEADER, AND 6 ADDRESS
        LD    A,L
        RLCA              ; SHIFT ADDRESS TO MSBIT
        RLCA
        LD    L,A
        LD    H,06H       ; HEADER
        CALL  SERPSH
        CALL  SERPOP
        CALL  CSOFF
        CALL  CK3
        EI
        RET
;
;                          SERIAL ASYNC COMMUNICATON
;
;
; Wait for Data on (ASYNC 0) (COM 1)
; Parameters Output: A Register contains Key
;
QPKEY   EI
        CALL  WTCHDG
PKEY    IN0   A,04        ; SERSTAT
        AND   80H
        DI
        JPZ   QPKEY
PKEY2   IN0   A,08        ; SERDTAR
        AND   7F          ; Parameter A reg contains Data
        RET
;
; Output Character through Com 1 ( ASYNC 0 )
; Parameters L register contains Character
;
PEMIT   EI
        IN0   A,04        ; SERSTAT
        AND   02H
        DI
        JPZ   PEMIT
        OUT0  06,L        ; SERDTAT
        RET
```

```
;
; Output Character through Com 0 ( ASYNC 1 )
; Parameters L register contains Character
;
C0OUT   EI
        IN    A,05h       ; SRSTAT1
        AND   02H
        DI
        JPZ   C0OUT
        OUT   07h,L       ; SRDTAT1
        RET
;
; Intput Character through Com 0 ( ASYNC 1 )
; Parameters Output:    L register contains Character and H ;
      register contains 0 ( Char Available ) ;                          or   L
register contains 0 and H register ;                        contains 1 ( Char
Not Available )
;
C0IN    LD    HL,0
        DI
        IN    A,05h       ; SRSTAT1
        AND   80H
        JPNZ  C0IN1
        EI
        INC   H
        RET
C0IN1   IN    A,09        ; SRDTAR1
        EI
        LD    L,A
        RET
;
;                            DIGITAL INPUT/OUTPUT
;
;
; Output byte through PPI0 PortA
; Parameters L register contains byte
;
PTAOUT  PUSH  BC
        LD    BC,100h     ; PORT A
        OUT   (C),L
        POP   BC
        RET
;
; Input byte containing the contents of PPI0 PortA
; Parameter Ouput: L register contains byte
;
PTAIN   PUSH  BC
        LD    BC,100h     ; PORT A
        IN    L,(C)
        LD    H,0
        POP   BC
```

```
        RET


;
; Input byte through PPI0 PortB
; Parameter Ouput: L register contains byte
;
PTBIN   PUSH  BC
        LD    BC,101h     ;PORT B
        IN    A,(C)
        CPL
        LD    H,0
        LD    L,A
        POP   BC
        RET
;
; Input 7 bit value from Dipswitch
; Parameters A register contains Value
;
QDIP    PUSH  BC
        LD    BC,140h     ; PORT1A
        IN    A,(C)
        AND   7FH
        POP   BC
        RET
;
:                              ANALOG INPUT/OUTPUT
;
;
; Output 12 bit Value to D/A channel 0 or 1
; Parameter Input: E register contains channel number and H/L ;
      register pair contains Value.
;
DAC0    LD    A,E
        OR    A
        JPNZ  DAC1
        LD    A,L
        AND   0FH
        OUT   0C0h,A      ; DACALOW
        LD    A,L
        RLCA
        RLCA
        RLCA
        RLCA
        AND   0FH
        OUT   0C5h,A      ; DACAMID
        LD    A,H
        AND   0FH
        OUT   0C2h,A      ; DACAHI
        OUT   0C3h,A      ; DACACON
        RET
```

```
DAC1    LD    A,L
        AND   0FH
        OUT   0C4h,A      ; DACBLOW
        LD    A,L
        RLCA
        RLCA
        RLCA
        RLCA
        AND   0FH
        OUT   0C5h,A      ; DACBMID
        LD    A,H
        AND   0FH
        OUT   0C6h,A      ; DACBHI
        OUT   0C7h,A      ; DACBCON
        RET
;
; Input 12 bit Signed Value from A/D channels 0 through 15
; Parameter  Input:      A register contains channel number
; Parameter Output:      H/L register pair contains signed value of
      that channel
;
ADCIN   AND   0FH
        PUSH  BC
        LD    D,A
        LD    BC,102h  ;PORT C
        IN    A,(C)
        LD    H,A
        AND   0FH
        CP    D
        JPZ   ADLP1
        LD    A,H
        AND   0F0H
        OR    D
        OUT   (C),A
        LD    A,10
ADLP0   DEC   A
        JPNZ  ADLP0
ADLP1   XOR   A
        LD    BC,180h     ; ADCLOW
        OUT   (C),A
        LD    BC,182h     ; ADCCON
ADLP2   IN    A,(C)
        AND   2
        JPNZ  ADLP2
        LD    BC,181h     ; ADCHI
        IN    H,(C)
        LD    BC,180h     ; ADCLOW
        IN    L,(C)
        POP   BC
        RET
```