MICROPAC HC11

HARDWARE REFERENCE MANUAL

for Revision 2 boards

Manual Revision 3

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DISCLAIMER

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FCC COMPLIANCE

EMAC's MICROPAC series of computers and accessories are classified as sub-assemblies per FCC CST bulletin, No. 62, May 1984. The bulletin states that sub-assemblies are not themselves subject to the FCC rules. Only the end product is directly subject to the rules.

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FEATURES:

The MICROPAC HC11 board (referred to hereafter as the HC11) uses the Motorola MC68HC11F1 microprocessor chip as the core MPU. Most of the capabilities of the board are built into the microprocessor itself. These are as follows:

Expanded 16-Bit Timer System with Four Stage Programmable Prescaler, 3 input captures(IC), 4 output compares (OC) and a pin which can be configured as a 4th IC or 5th OC.

Enhanced Nonreturn-to-Zero (NRZ) Serial Communications Interface (SCI)

Eight-Channel 8-Bit Analog-to-Digital Convertor

Clocked Serial Peripheral Interface

8-Bit Pulse Accumulator Circuit

Real-Time Interrupt Circuit

Computer Operating Properly (COP) Watchdog System

512 Bytes of EEPROM With Block Protect Mechanism

1024 Bytes of Static RAM

Power Saving STOP and WAIT Modes

The other on-board standard features are:

12 TTL level, bit programmable I/O lines and 8 additional high current output drivers.
RS-232 serial port which can optionally be configured as RS-422.
LCD interface for OPTREX(c) or compatible character LCD displays.

Optional features are:

An additional RS-232 serial port
4 channel, 8 bit digital to analog convertor
Interface for 4 by 5 keypads
Battery backed Real Time Clock/Calendar
32k to 128k battery backed RAM.

DIMENSIONS

The overall dimensions are 3 3/8 inches by 5 1/4 inches, and overall maximum component clearance (board thickness) of 1/2 inch.

POWER REQUIREMENTS

A single, unregulated DC supply input, fed through screw terminal ST1 is all that is required to operate the HC11. All RS-232 bipolar supplies are built in. This input is bypassed for power supply noise I/O by C7 and protected for reverse polarity by sacrificial crowbar diode D1.
The supply voltage should be at least 7 volts DC, including negative ripple peaks, and should be no more than 15 volts DC. The HC11 input voltage is less critical than the other SBC's, as the upper voltage limit set by the heat dissipation of the 5 volt regulator, and the voltage rating of the input power supply bypass capacitor. Input transient voltages as high as 35 volts maximum will not harm the board if given for a short period of time only, on the order of 1 second or less.

The current consumption depends somewhat upon the digital output status and RS-232 connections, but will normally be below 150 mA. The board without without the serial port upgrade and D/A option will typically draw under 55mA. Typically, the D/A draws under 6mA and

the serial port upgrade under 75mA.

MPU RESET

The 68HC11 MPU chip has a rather unusual RESET input pin. Unlike more conventional MPU's, which have a simple "power-on reset" provided by a charging capacitor, which also are "input only" in nature; the 68HC11 RESET pin is bi-directional. A system hardware reset may be issued FROM the MPU, as well as received by it.

This requires special circuitry to permit the pin to accept both power-on and pushbutton resets, as well as to permit the MPU to generate a reset output, without hardware contention.

Power-on and pushbutton resets are provided by conventional circuitry. Pushbutton reset is supplied by simply connecting a pushbutton contact accross screw terminal ST1, terminal 3 and 2.

MEMORY MAP

There are 4 modes of operation for the 68HC11. Selection of the operating mode is made at MPU pins MODA and MODB. Jumpers are Normally, these jumpers are never touched by the user, except when special operating modes are required.

The default configuration with no jumpers installed is Expanded Nonmultiplexed mode since both MODA and MODB inputs are tied high through pullup resistors. In this mode, code can be executed in any memory area (in the internal RAM or EEPROM, or in the external RAM or ROM).

The 68HC11 microprocessor allows remapping of the internal RAM, internal EEPROM, I/O chip selects and internal device registers. Because there are so many combinations possible, for simplicity we will use the configuration included on the distribution disk demo program. This memory map is as follows:

$0000-$7FFF	EXTERNAL RAM (SOCKET U7)
$8000-$805F	INTERNAL REGISTERS
$8060-$87FF	ON-BOARD CHIP SELECTS
$8800-$8DFF	EXTERNAL CHIP SELECT (ON EXPANSION CONNECTOR)
$8E00-$8FFF	INTERNAL EEPROM
$9000-$93FF	INTERNAL RAM
$9400-$FFFF	EXTERNAL ROM (SOCKET U6)

ROM

The HC11 has a program ROM socket that may accept either 16K or 32K devices depending on the position of JP3. The ROM space in memory is from address 8000 hex to FFFF hex but may be overlapped by the internal memory and registers since they have higher priority.

EEPROM

The HC11 has 512 bytes of EEPROM which can be block protected from accidental writing or erasure. Since the EEPROM is relocatable on any 4K boundary (xE00 to xFFF, where "x" is any valid hex digit) it could be moved to $FE00, allowing a small application program to reside in the EEPROM and eliminating the need for an external ROM. See the demo program for example drivers and see the MC68HC11F1 Technical Data Manual for more details.

RAM

The SRAM socket (U7) accepts 8K or 32K/128K byte devices depending on the setting of JP4. The memory space for SRAM is from

$0000 to $7FFF. When a 128K device is in the socket, one of the four 32K banks within the device may be selected by writing to PORT G bits 0 and 1. Note that the bank select lines are pulled down to ground via two resistors, so bank 0 is always selected until such time as the port lines are deliberately set by software to another bank.

PORT G BIT 1	BIT 0	BANK
0	0	0
0	1	1
1	0	2
1	1	3

This socket also accepts 32K or 128K battery-backed RAMs (part # E010-09, E010-12) or a real time clock/battery-backed RAM (part # E010-03).

I/O PORTS

The I/O map listed below is for the configuration included in the demo program. The I/O map is as follows:

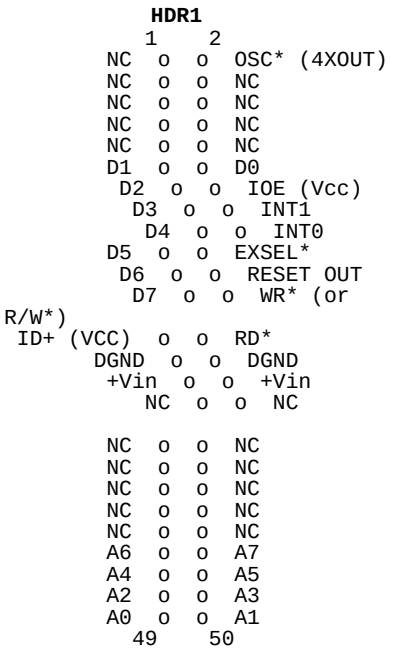
$8000-$805F	Internal control and status registers (see the MC68HC11F1 Technical Data Manual for more details
$8060-$87FF	I/O CHIP SELECT 1 (CSIO1 is for on-board devices)
$8060	LCD COMMMAND REGISTER (LCDCMD)
$8061	LCD DATA REGISTER (LCDDAT)
	(SCN2651 PORTS. See SCN2651 Data Sheets for more details)
$8064	WR TO TRANSMIT, RD TO RECEIVE (SERDR)
$8065	RD STATUS, WR TO SYN1/2/DLE REGS (SERCNST)
$8066	RD/WR MODE REGS 1/2 (SERMODE)
$8067	RD/WR COMMAND REGISTER (SERCMD)
$8068	KEYPAD PORT (KEYPRT)
$8800-$8DFF	External Chip select (EXSEL* on HDR1)
$B000	DATA LATCH (for PX12-PX19 on the digital I/O HDR)
$B004-$B007	D/A output channels 0-4

Note:

For the Data Latch and the D/A output channels, the address must be one which accesses the external ROM (i.e. a ROM address that is not overlapped by the 68HC11's internal registers, RAM or EEPROM). These ports are write only.

I/O EXPANSION BUS HEADER

The bus expansion header's data, address, and control signal configuration is compatible with all EMAC SBC's, thus permitting the HC11 to interconnect with most EMAC bus peripherals, such as the EPROM PROGRAMMER board and the Programmable 32 Line Parallel I/O board (this assumes the configuration included in the demo program is used). It can also be used to connect to customized application expansion boards. Its layout is as follows:



(A0-A7) These are the lower 8 bits of the address bus.

(D0-D7) These are the data Bus.

(Osc*) This pin carries an 8 MHz clock signal from the 68HC11 MPU. The MPU signal name is 4XCLK. Essentially, the 8 MHz system oscillator, controlled by crystal Y1, is output at this MPU pin. Internally to the 68HC11, the crystal frequency is divided by four, and gated with the oscillator signal to produce the ECLOCK (Enable Clock) signal.

On the HC11, the 4XCLK passes through two inverters used to buffer the 4XCLK signal. These inverters were used simply because they were "spares" from the circuit design. Although only one inverter would serve to buffer the signal, the 4XCLK signal would be inverted relative to the timing of other MPU signals, as far as the bus expansion timing is concerned. The second inverter flips the polarity back to normal.

It should be cautioned, however, there are now two gate delays present. This is no problem for the EPAC bus cards. However, this timing detail is important in custom interface cards that are timing critical.

Normally, this clock signal would be used only as a handy clock to feed to divider chains for baud generation, timer functions, etc.

(EXSEL*) In the demo program setup, this is the external chip select activated by reads or writes to $8800-$8DFF and is active low. It is active during the full device address valid time (compatible with the INTEL style bus timing).

This pin is connected to the CSIO2/PG4 pin of the 68HC11, which means it can be programmed to be a TTL input or output.

To make the expansion bus Motorola compatible, set JP8 in the "MO" position. In this configuration the WR* line can be used as a Motorola compatible RD/WR* line. CSIO2 should be set up to be qualified and valid with the Eclock. Note that CSIO2 can be programmed to be active high or active low. See the MC68HC11F1 Technical Data Manual for more details

(WR*) This pin is wired to JP8. When used with INTEL bus style peripherals, JP8 should be set to the "IN" position, and this pin will have the separate, active low WR* bus signal present on it. When Motorola bus style peripheral chips are used, JP8 should be set to the "MO" position, then this pin will perform as the R/W* line.

(RD*) This pin is used with INTEL bus style peripherals, it is the separate active low RD* signal. When Motorola peripheral chips are used in a bus expansion card, this signal line is not needed.

(INT1) This pin is an interrupt input which in the EPAC bus expansion specification, is called INT1. This pin is controlled by JP10, so a jumper in position "E" connects INT1 to the inverter that feeds the 68HC11's XIRQ interrupt. This interrupt is pseudo-nonmaskable, meaning it is not maskable once it is enabled (by clearing the X bit in the CCR register). However it is masked during reset and after receiving an XIRQ interrupt.

When variables or registers are used and modified by different interrupt handlers, it is important to disable interrupts around the code that reads/modifies/writes the variables. This prevents another handler from interrupting and modifying the same variable, causing the data to be corrupted. For this reason care should be taken to insure that the XIRQ handler doesn't modify RAM variables or registers that are used in the foreground or used by other interrupt handlers since XIRQ can't be disabled.

(INT0) This pin is an interrupt input, which in the EPAC bus expansion specification is called INT0. This goes to JP7 and is connected to the 68HC11's IRQ interrupt pin by putting a jumper in position B (see "JUMPER DESCRIPTION" for warnings regarding JP7). Note that the INT1 signal is inverted before it gets to the IRQ line. Since IRQ can be programmed to be falling edge sensitive (demo program's default) or low level sensitive, this means INT1 can be rising edge, or high level sensitive.

(RESET) Power on reset, low voltage reset, and MPU initiated RESET all appear at this pin, in active high mode. All peripheral devices used must accept this signal as the reset state when this line is high, and in the operational condition when low.

(IOE) This stands for I/O enable. On the HC11, this pin is simply tied to Vcc. On some other board designs, the I/O enable pin is a

programmable function pin, which passes into the peripheral card's decoder. This function is not employed on the peripheral cards that are used with the HC11, so it is simply tied high, so if an expansion card requires this enable to be active, it will see an enable level at this pin.

(ID) On the HC11, this pin is simply tied to Vcc. On some other board designs, the ID enable pin is used to identify when power is applied to the host SBC. This function is not employed on the peripheral cards currently used with the HC11.

(DGND) These pins are the digital power ground pins of the EPAC expansion bus specification. They are simply paralleled lines for carrying ground return between the host SBC and peripheral boards.

(DPOW) These pins are the Direct power leads. They carry unregulated DC power fed from the host's power supply screw termination, to the peripheral card(s). All current EPAC peripherals have a separate 5 volt regulator on them, which regulates this raw power input voltage down to 5 volts, for distribution among the chips on each peripheral card.

ANALOG INPUTS

The HC11 has 8 analog inputs. They are strictly unipolar, 0 to 5 volts, 8 bit resolution. No other ranges are possible, as these features are part of the MPU chip itself.

The analog inputs are accessible via the analog input connector header, which has the MICROPAC standard connection format. The connector is organized as follows:

+VIN power, Vcc and ground are available here to supply power to signal conditioning cards that may be connected here.

Analog Input HDR4

```
                1   2
analog channel 0  . .  ANL GND
analog channel 1  . .  ANL GND
analog channel 2  . .  ANL GND
analog channel 3  . .  ANL GND
analog channel 4  . .  ANL GND
analog channel 5  . .  ANL GND
analog channel 6  . .  ANL GND
analog channel 7  . .  ANL GND
     ground  . .  ground
       +VIN  . .  VCC
           19   20
```

Since the 0-5 volt range is built into the MPU itself and no other full scale voltage ranges are possible without external signal processing on support cards, forcing the analog inputs beyond these voltage limits will cause the MPU to latch-up, or even damage it. External circuitry should be designed to protect the inputs from high energy transients, and to provide the HC11 with signals within the 0-5 volt range only.

Additionally, power supply sequencing should be designed to apply input voltages only when the HC11 is powered up, or to at least send very low input currents to it when the MPU is in the powered down state. These are standard CMOS anti-lachtup procedures, nothing unique to the HC11 design.

See the MC68HC11F1 Technical Data Manual for more details.

ANALOG OUTPUT

The HC11 has provision for an optional four channel, eight bit resolution, 0 to 5 volt analog output port. The output voltage and resolution are selected to match the analog inputs, so these ratings are also fixed at 0-5 volts, and are not alterable. The connector is organized as follows:

D/A HDR2

```
   1   2
+Vin . . GND (ground)
CH 0 . . GND
CH 1 . . GND
CH 2 . . GND
CH 3 . . GND
PORT A0 . . GND
  11   12
```

Writing to $B004-$B007 will write to channels 0-3 respectively (see notes under "I/O PORTS" for restrictions).

+Vin is the unregulated DC that is applied to ST1. Port A0 is a port line which can be programmed as a digital input or output (also available on HDR3).

DIGITAL I/O HEADER

The HC11 board has a digital I/O port, whose basic function is similar to the Digital I/O ports found the other SBC's in the EPAC and Micropac family. These Digital I/O port lines are accessible at header connector HDR3.
The header connection footprint for HDR3 is compatible with OPTO-22(tm) I/O rack assemblies and is defined as follows (even numbered pins are ground):

Port lines PX0-PX11 and PX20 may be programmed as inputs or outputs or their special functions may be enabled. See the MC68HC11F1 Technical Data Manual for programming details. The PX20 pin may be used for general purpose I/O, or may be delegated by JP9 (see "JUMPER DESCRIPTION") to LCD backlight control, or to polling interrupts.

Port lines PX12-PX19 are output only. They come from an octal latch and a buffer driver allowing them to drive high voltage or high current loads, or LEDs, but they are not TTL level compatible.

Each line of the buffered output driver is an open collector darlington transistor that switches that line to ground when the corresponding port bit is set. Each line may sink up to 500 mA, but the total package current may not exceed 1.5 Amps. There is space available for LEDs and current limiting resistors to be populated and driven by these eight output lines.

HDR3 pins 5, 3, and 1 are not used, or wired to anything at this time in the HC11 design.

HDR3

```
50 49
 . . Vcc
 . . PX0 PORTA 0/IC3 (IC=INPUT CAPTURE)
 . . PX1 PORTA 1/IC2
 . . PX2 PORTA 2/IC1
 . . PX3 PORTA 3/IC4/OC5/OC1 (OC=OUTPUT COMPARE)
 . . PX4 PORTA 4/OC4/OC1
 . . PX5 PORTA 5/OC3/OC1
 . . PX6 PORTA 6/OC2/OC1
 . . PX7 PORTA 7/OC1/PAI (PULSE ACCUMULATOR IN)
 . . PX8 PORTD 2/MISO (SPIs MASTER-IN SLAVE-OUT LINE)
 . . PX9 PORTD 3/MOSI (SPIs SLAVE-OUT MASTER-IN LINE)
 . . PX10 PORTD 4/SCK (SPIs SERIAL CLOCK LINE)
 . . PX11 PORTD 5/SS* (SPIs SLAVE SELECT. HI=MASTER, LO=SLAVE)
 . . PX12 DATA LATCH 0
 . . PX13 DATA LATCH 1
 . . PX14 DATA LATCH 2
 . . PX15 DATA LATCH 3
 . . PX16 DATA LATCH 4
 . . PX17 DATA LATCH 5
 . . PX18 DATA LATCH 6
 . . PX19 DATA LATCH 7
 . . PX20 PORTG 6/CSGEN (GENERAL CHIP SELECT)
 . . NC
 . . NC
 . . NC
2   1
```

LCD DISPLAY PORT

A 16 station ribbon cable header with pin assignments compatible with OPTREX character type LCD displays is provided on the HC11. (Consultation with EMAC should be made prior to selection of any non-standard LCD display.) This connector is defined as follows:

LED Backlit LCD displays may also be used with the HC11. Putting a jumper in JP9 position E allows you to drive the backlight continuously. If you put a jumper in position D, with position E vacant, you may turn it on by configuring PORTG 6 (PX20) to be an output and setting the output high.

Most LED backlit LCD displays used have built-in current limiting for the LEDs. Resistor R6, a 1 ohm 1/8 watt resistor, is present merely as a formality. If non-standard displays are used, that do not have LED current limiting built into the panel, this resistor must be replaced with the correct value. Further, a higher power resistor may need to be used.

```
Vcc . . GROUND
 RS . . Vee (CONTRAST)
  E . . R/W*
 D1 . . D0
 D3 . . D2
 D5 . . D4
 D7 . . D6
 BA . . BK (LED backlight
cathode)
  15   16
```

HDR 6

```
  1   2
```

Optrex compatible displays have a "contrast" control. LCD display contrast refers to the clarity of a displayed character relative to the viewing angle. A voltage fed to the contrast pin adjusts the "tilt" of the LCD crystals when they are polarized (turned on). The HC11 has a fixed resistor R7 feeding the contrast input to the LCD panel. This value has been found satisfactory for most practical applications. Therefore, an adjustable contrast control is not provided.

KEYPAD PORT

The optional keypad port has a connector directly compatible with 3X4 and 4X4 keypads made by C&K Switches, however, many formats may be adapted to it. It can accept up to a 4X5 matrix. The keypad port merely scans five column lines, and reads four row input lines. Any crossover reports a key pressed, and the IRQ* input is triggered if there is a jumper in position C of JP7 (see "JUMPER DESCRIPTION" for warnings regarding JP7). The interrupt handler should mask off the upper 3 bits after reading the keypad port. Figure B shows the value that will be returned at the crossover of an X and Y axis. See the demo program for an example of the keypad related routines.

Note that if the keypad interrupt and COM1 receive and/or INT0, are enabled to trigger IRQ, any other interrupts received will be missed as long as a key is being pressed even though only one interrupt will occur. If the keypad is used, it should be the only interrupt on IRQ.

Fig. A
HDR5

```
   . Y5
1  . X4
   . X3
   . X2
   . X1
   . Y4
   . Y3
   . Y2
   . Y1
9  . GROUND
```

Fig. B

	X1	**X2**	**X3**	**X4**
Y1	00	01	02	03
Y2	04	05	06	07
Y3	08	09	0A	0B
Y4	0C	0D	0E	0F
Y5	10	11	12	13

SERIAL COMMUNICATION

The HC11 has a standard RS-232 serial communication port. The serial port hardware is built into the MPU itself, and RS-232 to TTL serial interface is provided by a MAX-232 interface/power supply chip. If the standard serial port is configured for RS-422/485 operation, handshaking is not available. The RS-422/485 option may be used either in full duplex, or in the EMAC networking mode (half duplex).

The optional second serial port if populated, uses a SCN2651 UART, and an additional MAX-232 chip for interface (it cannot be configured as RS-422/485).

HANDSHAKE LINES

Both serial ports have identical handshake capability, with one handshake out, and one handshake in, both at RS-232 signal levels.
For the standard serial port (CN1), the handshake out line is controlled by writing PORTG bit 3(writing a 0 activates, and 1 deactivates). The status of the handshake in line is found by examining PORTG bit 2 (Reading a 0=active and 1=inactive). In the demo program, PORTG bit 3 is configured as an output and PORTG bit 2 is configured as an input.

For the optional serial port (CN2), the handshake out is controlled by the DTR* line and the handshake in is controlled by DSR*. Writing a 0 to bit 1 of the SCN2651 command register will cause the handshake line to deactivate and writing a 1 will activate the line. Reading a 0 from bit 7 of the SCN2651 status register indicates the line is inactive and reading a 1 indicates it is active.

CN1 (RS-232)

```
   1   2
 nc . . nc
 Tx . . handshake input (PG2)
 Rx . . handshake output (PG3)
 nc . . nc
GND . . nc
   9  10
```

CN1 (RS-422/485)

```
    1   2
  nc . . nc
 TXB . . RXB
 TXA . . RXA
  nc . . nc
 GND . . nc
    9  10
```

CN2 (OPTIONAL)

```
   1   2
 nc . . nc
 Tx . . handshake input (DSR)
 Rx . . handshake output (DTR)
 nc . . nc
GND . . nc
   9  10
```

The standard serial port has a special jumper selection that enhances half-duplex communication (It is normally full duplex). This half duplex loopback option is normally used only in special applications.

Both the main serial port (CN1), and the optional serial port (CN2) may be connected to the outside world via a ten position ribbon cable header for each port. CN1 and CN2 have identical pinouts. The ribbon cable connections are strategically assigned so that insulation displacement DB-9 female housings may be crimped onto the other end of the ribbon cable, and the standard EMAC pinout for signal, ground, and handshake lines will appear at the DB-9 connector.

The built-in serial port has standard baud rates from 150 to 9600 baud. The optional serial port has the following 16 baud rates available: 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600 and 19200. Note that baud rates 134.5, 2000 and 19,200 have errors of +0.016%, +0.235% and +3.125% respectively. See the SCN2651 data sheets for more features and programming information.

JUMPER DESCRIPTION

JP1 and JP2.

Jumpers JP1 and JP2 are used in conjunction with the special direct TTL interface for a proprietary board. Jumper JP1 switches a gate input that loop back serial data transmitted back to the serial data input. Jumper JP2 is used in conjunction with the handshake output to block the actual serial data input during this special mode. The jumpers are normally configured with the loopback and force block modes disabled.

JP1 and JP2 are normally soldered in place, as normal applications do not require them. The full duplex mode is selected by this factory installed configuration. Only when the custom proprietary board (or similar custom application) is installed on a HC11 will the jumpers be configured to the special half-duplex mode.

JP3.

Jumper JP3 configures the EPROM socket U6 to accept either 16K or 32K devices. It is located inside the barriers of the socket housing, and is hidden when a device is installed in the socket.

JP4.

Jumper JP4 configures the SRAM socket U7 to accept either 8Kbyte, 32K or 128K devices. It is located inside the barriers of the socket housing, and is hidden when a device is installed in the socket.

When installing an 8K SRAM, switch the jumper to the "8" position first, then install the RAM. Likewise, if installing a 32K or a 128K device, switch the jumper to the "32/128" position.

JP5 and JP6.

Jumper options JP5 and JP6 are used to select special operating modes of the core MPU. The MPU reads the state of the MODA and MODB control pins upon power on or reset. These pin configuration codes affect the operation of the 68HC11 MPU at the most basic level. They are normally only used for diagnostic or internal EEPROM configuration, and almost never employed by the normal operation of the HC11 board.

In rare cases, it may be necessary to invoke these special MPU core modes, so jumpers JP5 and JP6 exist to permit access to the logic level applied to these MPU control pins. Normally, these inputs are tied to logic high by 4.7 Kohm resistors. By inserting a jumper at JP5, control line MODB will be grounded and by inserting a jumper at JP6, control line MODA will be grounded.

JP7.

This allows connection of 1 to 3 interrupt sources (or none) to the IRQ interrupt. Putting jumpers in positions A,B, and C will enable interrupts from COM1 receive, INT0, and the KEYPAD interface, respectively. Remember that if you put jumpers in more than one position and your program requires these interrupts to occur asynchronously, there is a possibility that they may occur simultaneously and therefore not be detected! Multiple interrupt sources on IRQ should be used with care.

JP8.

When using the HC11 with INTEL bus style peripherals, JP8 should be set to the "IN" position, and the expansion buss' WR* will be compatible with them. To make the expansion bus Motorola compatible, set JP8 in the "MO" position. In this configuration the WR* line can be used as a Motorola compatible RD/WR* line. Since CSIO2 is set up to be INTEL compatible in the demo program, CSIO2 should be changed so that it is qualified and valid with the Eclock. Note that CSIO2 can be programmed to be active high or active low. See the MC68HC11F1 Technical Data Manual for more details

JP9.

Putting a jumper in position A or B or C of JP9 (only one of these 3 positions at a time), allows you to poll the selected interrupt source by using PX20 (port G 6) in input mode. Positions A,B, and C correspond to the COM1 receive, INT0, and KEYPAD interface interrupt sources, respectively.

Positions D and E determine the drive source for the LCD backlight. You may put a jumper in only one of the two positions at a time. If PX20 is not being used for the polling function, you may put a jumper in position D to drive the LCD backlight with PX20 in the output mode. Putting a jumper in position E will turn on the backlighting continuously, leaving PX20 free to be used for polling or general purpose I/O.

JP10.

This is included to enable the single-step function of the BUFFALO monitor. Putting a jumper in position "SS" enables the single stepper by connecting XIRQ to OC5/PA3 (through an inverter). A jumper in position "E" connects the INT1 pin of HDR1 to the inverter that feeds XIRQ*.

CHANGES BETWEEN BOARD REVISIONS

Rev. 1 Changes in General

Pullups have been added to CSIO1 and CSIO2 to keep them from selecting devices and causing bus contention in the period of time between reset and the moment they are initialized as chip selects. Other features implemented are as follows:

1) serial port handshake lines have been changed.
2) redirection of interrupts via jumper.
3) interrupt polling capability.
3) hardware support of BUFFALO single stepper.

Compatibility with Rev. 0

The following section tells how to retain compatibility with revision 0 boards.

CN1 and CN2

The handshake lines pins (4 and 6) should be exchanged to make them the same as REV. 0.

XIRQ

XIRQ now can only accept 1 input at a time, so COM1 Rx and INT0 cannot be connect to it at the same time. To connect COM1 to XIRQ, connect JP7 pin 2 (position A jumper removed) to the center pin of JP10 (JP10 jumper removed). To connect INT0 to XIRQ, connect JP7 pin 4 (position B jumper removed) to the center pin of JP10 (JP10 jumper removed).

IRQ

To restore the original IRQ interrupt capability, there should be a jumper in position C (only) of JP7 and no jumper in JP10. Then connect the pin of JP10 labeled "E" to pin 3 of JP7.

Following are details of the changes on revision 1.

LCD PORT

The LCD backlight drive selector has been moved to JP9 (described later).

KEYPAD PORT

Rev. 1 gives access to another row selector, Y5, by including an access hole just before pin 1 of the connector (the connector is the same as before). When using this extra row, the values 10h, 11h, 12h, and 13h will be returned when X1, X2, X3, or X4 are intersected, respectively. Also, if using Y5 the value read from the port should mask off the upper 3 bits instead of the upper 4.

I/O EXPANSION BUS HEADER

HDR1 pins labeled INT0 and INT1 have been changed in REV. 1 so that they are no longer directly connected to the XIRQ and IRQ lines, respectively. This may be done by wire wrapping

DIGITAL I/O HEADER

PX20 is can also be used to poll interrupts. See the description of JP 9.

JP7

Following is a description of JP7 of rev. 0 and rev. 1.

REV. 0 JP7.

Jumper option JP7 provides selection of LCD backlight control. If put in the "on" position the backlight is turned on. If put in the "PX20" position the MPU's CSGEN/PG6 line controls the backlight (PX20 is also available on digital I/O header HDR3). See the section "DIGITAL I/O HEADER" for more information.

REV. 1 JP7.

This allows connection of 1 to 3 interrupt sources (or none) to the IRQ interrupt. Putting jumpers in positions A,B, and C will enable interrupts from COM1 receive, INT0, and the KEYPAD interface, respectively. Remember that if you put jumpers in more than one position and your program requires these interrupts to occur asynchronously, there is a possibility that they may occur simultaneously and therefore not be detected! Multiple interrupt sources on IRQ should be used with care.

JP9. (REV.1 ONLY)

Putting a jumper in position A or B or C of JP9 (only one of these 3 positions at a time), allows you to poll the selected interrupt source by using PX20 (port G 6) in input mode. Positions A,B, and C correspond to the COM1 receive, INT0, and KEYPAD interface interrupt sources, respectively.

Positions D and E determine the drive source for the LCD backlight. You may put a jumper in only one of the two positions at a time. If PX20 is not being used for the polling function, you may put a jumper in position D to drive the LCD backlight with PX20 in the output mode. Putting a jumper in position E will turn on the backlighting continuously, leaving PX20 free to be used for polling or general purpose I/O.

JP10. (REV.1 ONLY)

This is included to enable the single-step function of the BUFFALO monitor. Putting a jumper in position "SS" enables the single stepper by connecting XIRQ to OC5/PA3 (through an inverter). A jumper in position "E" connects the INT1 pin of HDR1 to the invertor that feeds XIRQ*.

APPENDIX A

Data Sheets

APPENDIX B

Schematics