MICROPAC 180

HARDWARE REFERENCE MANUAL

for Revision 3 boards

Manual Revision 1.5

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DISCLAIMER

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FCC COMPLIANCE

EMAC's MICROPAC series of computers and accessories are classified as sub-assemblies per FCC CST bulletin, No. 62, May 1984. The bulletin states that sub-assemblies are not themselves subject to the FCC rules. Only the end product is directly subject to the rules.

TABLE OF CONTENTS

THE MICROPAC 180 TECHNICAL DESCRIPTION

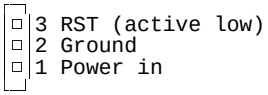
DIMENSIONS

The MICROPAC 180 board measures approximately 3.675" by 5.362" , with four mounting holes, spaced 3.3" and 5.00" apart. The board consumes a little less than 0.75" vertical spacing. The RS-232 DB-9 connector hangs about 0.25" past the edge of the board on one side.

POWER SUPPLY

The MICROPAC 180 may be powered by 8 to 15V DC when 2 jumpers are in JP8 (this is the standard configuration). In this configuration the board may be used in automotive environments if transients such as alternator load dump, and reversed battery are isolated from the MICROPAC 180. If used permanently in such an environment, extra protection circuitry and extended temperature range optioning is recommended to enhance reliability. To power the board from an external 5V regulated supply, remove the 2 jumpers from JP8 and jumper the middle 2 pins leaving the outer 2 pins open.

Power/reset
Screw Terminal
ST1



MEMORY MAP DESCRIPTION

The MICROPAC 180 has two memory sockets on it and each socket is mapped for 512K byte devices with the ability to accept lower cost, smaller memory chips. The MICROPAC 180 requires no memory or I/O wait states other than those built directly into the microprocessor itself.

CMOS devices should be used for all memory components to preserve the low power consumption and low voltage overhead ratings of the MICROPAC 180. With static RAMs (SRAMs), there is a greater choice in the supply current grades with LP (low power, which is standard), and LLP (low, low power) versions available. The current drain specifications of the MICROPAC 180 are rated using the LP grade of static rams, types 432000 LP-XX, 431000 LP-XX or 43128 LP-XX devices, so current drain may be decreased further by using LLP devices.

EPROM/Flash memory

Memory socket U6 accepts EPROMs and PEROMs (flash memory). The memory in this socket is mapped at memory addresses 00000 hex through 7FFFF hex (512K bytes). If the smaller EPROM option is used (128K or 64K), the memory map remains the same, but the data will wrap around throughout the entire 512K addressing range. Devices with access times of 250 nS or lower (faster) have been found to function reliably with the MICROPAC 180.

The following tables show the jumper configurations for JP3, JP4 and JP5 for the different sizes of EPROM and PEEROM.

EPROMS

PART #	SIZE	JP3	JP4	JP5
AT27C512R	64K	B	B	B
AT27C010/L 27C1001A	128K	B	B	OUT
AT27C020	256K	B	B	OUT
AT27C040 27C2001	512K	A	B	B

PEROMS

PART #	SIZE	JP3	JP4	JP5
AT29C512	64K	B	B	A
AT29C010	128K	B	B	A

AT29C020	256K	A	B	A
AT29C040	512K	A	A	A

A 28 pin memory chip (such as the 27C512) should be placed with its notch alligned with that of the socket but leaving socket pins 1, 2, 31 and 32 unoccupied, and the rest filled (this is called the ground justified position).

RAM

Memory socket U5 is mapped from 80000 hex to FFFFF hex for 512K SRAM memory devices. Devices with access times of 250 nS or lower (faster) should be used.

As in the case of the EPROM socket, smaller memory devices, such as 128K or 32K may also be used here. The smaller devices are placed in the ground justified position (described earlier) of their sockets, and the memory data accessed will also wrap around if the smaller devices are used in place of the full sized 512K RAMs.

RAM MEMORY SIZE	**DEVICE NUMBERS**	**JP2 POSITION**
512K	432000	"512"
128K	431000 M5M51008P HM628128	"32/128"
32K	84256C 43256 CXK58257AP	"32/128"

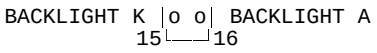
If a battery backed RAM option (Smart-socket), or a real time clock option (Smart-clock) is added, the RAM device should be removed and the option plugged in its place (ground justified with the notch oriented correctly). After the RAM is plugged into the Smart-socket or Smart-clock, it will be non-volatile. These options have power monitors and lithium batteries built into them, which supply standby power to the RAM device when the board is powered down. Only low power RAMs should be plugged into a Smart-socket or Smart-clock.

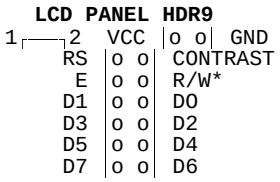
SERIAL EEPROM

This non-volatile memory is not part of the memory map and is intended to be used to hold configuration information and other data that doesn't change often, since the device is rated for only 10,000 write cycles. The memory is organized as 64X16 bits and all access is done serially through control port D. See assembly language drivers for programming examples.

LCD INTERFACE

The LCD interface allows the MICROPAC to control OPTREX and compatible LCD panels. The source for power for LED backlight is directed by JP7. If JP7 is in position "B", the backlighting is always on. If in position "A" it is controlled by port C bit 7. A high on this port line turns it on, and a low turns it off. The contrast level may be controlled by a fixed resistor on the MICROPAC or by a remote potentiometer. See the distribution disk's assembly language drivers for programming examples.





DIGITAL I/O

The MICROPAC 180 has a 24 line parallel digital I/O port with 16 programmable lines and 8 high current driver outputs. The Digital I/O header, HDR2 is a 50 pin male header, best suited for connection to a ribbon cable. The pinout is compatible with OPTO-22 I/O rack standards.

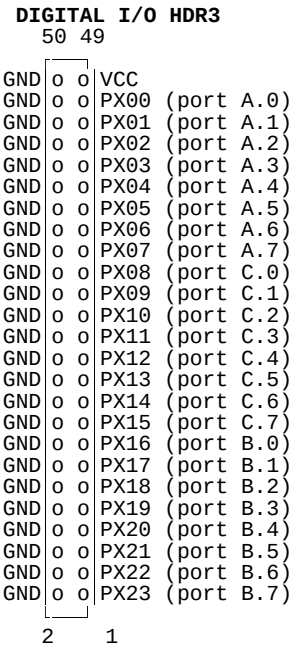
The parallel port chip is an 82C55, with ports A and C routed directly to connector HDR2 and port B driving a ULN2803 high current driver. Note that the output of the high current driver is the inverse of the port B output. All ports may be initialized as input or output ports by writing to the control register, but port B is only useful when programmed as an output port.

The digital I/O port is located in the I/O map, with the following addresses :

Port A	400 Hex	Read/Write
Port B	401 Hex	Read/Write
Port C	402 Hex	Read/Write
Control	403 Hex	Write only

For information on programming the 82C55 PPI chip see the appendix.

DIGITAL I/O HDR3



SERIAL COMMUNICATIONS PORTS

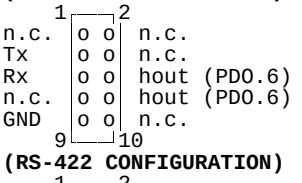
In the standard configuration, the two serial ports that are part of the HD64180/Z180 Asynchronous Serial Communication Interface (ASCI) are connected to the outside world through an RS-232 interface. The RS-232 negative supply voltage is generated by a MAX232 chip on board so no external negative supply is needed.

The COM0 and COM1 ports are both implemented in the HD64180/Z180 microprocessor. These asynchronous serial ports provide full duplex serial communication at software selectable baud rates of 300 to 38400. To set the baud rate, the correct prescale value (divide by 10 or 30) and the correct divide ratio must be selected. These values are chosen depending on the baud rate desired and the processor's clock frequency. The Asynchronous Serial Communications Interface (ASCI) Control Register B is used to set the baud rate. In addition to setting the baud rate, the number of bits, the type of parity, and the number of stop bits must be selected. These parameters are set by ASCI Control Register A. See apppendix for details.

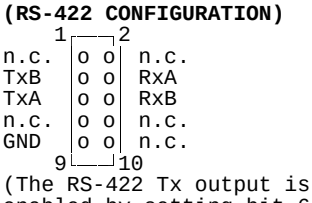
Both COM1 and COM0 have the provision to be used in an interrupt mode or a polled mode. To use the ASCI in the interrupt mode, first enable the interrupts using the ASCI Status Register and "EI" instruction and provide the software interrupt handlers at the software selectable vector. In the polled mode of operation for reception, check bit 7 (RDRF) of the ASCI Status Register. If this bit is high then there is a byte available for reading. This byte can be read from the ASCI Receive Data Register. For transmission, check bit 1 (TDRE) of the ASCI Status Register. If this bit is high then the transmit buffer is empty and a byte may be written to the ASCI Transmit Data Register.

If the RS422/485 option is installed instead of the RS232 on COM0, it can be used as a full duplex RS422/485 port. The port can be configured as a half duplex, RS-485 networking port by tying the output and input pins together. Up to 32 similar ports may share the same communication lines. To prevent contention, especially when used as a half duplex port, care must be taken to assure that only one port transmits at a time. The system automatically powers up in the receive mode. The RS-485 transmitter is enabled by setting bit 6 of Port D or disabled by resetting bit 6. The RS422/485 option is necessary when using EPAC

HDR2 (COM0)
(RS-232 CONFIGURATION)

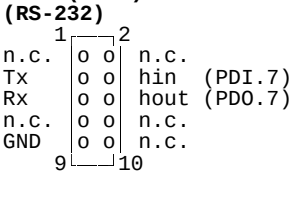


(RS-422 CONFIGURATION)

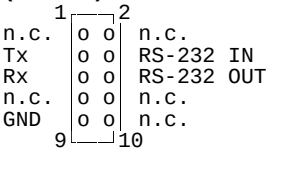


(The RS-422 Tx output is enabled by setting bit 6 of port D, and disabled by resetting this bit).

HDR3 (COM1)
(RS-232)



HDR4 (COM2)
(RS-232)



networking software.

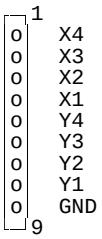
The HD64180/Z180 ASCI ports also provide the ability for a nine bit network. This innovative function when enabled, will interrupt the processor if the ninth bit of a data byte is set. Using this feature in conjunction with the multi-drop RS485 option and software drivers provide all the components of a simple yet powerful nine bit network.

COM2 is implemented on the optional coprocessor (this processor and its interface are discussed later). The handshake lines are not software controllable (the RS-232 OUTPUT pin merely follows the level applied to the RS-232 INPUT line). The coprocessor buffers characters received and characters to be transmitted and can interrupt the main processor based on the number of characters in the buffers. See the assembly language drivers for details on this interface.

KEYPAD INTERFACE

This interface is implemented on the optional coprocessor (discussed later). It is a 4 by 4 matrix decoder which detects a connection at the intersection of an X and Y pin. An interrupt can be generated when a key is pressed indicating that the coprocessor has a key ready to be read. See the assembly language drivers for programming details for this interface.

Keypad input HDR8



ANALOG TO DIGITAL CONVERTOR

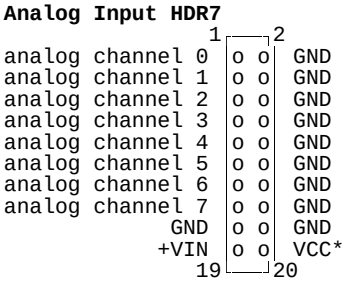
The MICROPAC 180 has an 8 channel analog to digital converter unit. Resolution of the A/D converter is standard 10 bits, or an optional 12 bit converter may be installed. The input to the analog system is unipolar with a voltage range of 0 to 5 volts.

The A/D utilizes a CMOS low power A/D chip, with a built in multiplexor. Control data is written via a serial data link to the A/D, specifying the channel number and other bit information, and the conversion result is retrieved by this link. As no microprocessor system address or data bus lines go directly to the A/D, internal noise is very low, and the conversion results are very clean and stable. See the assembly language drivers for programming details.

The analog inputs are accessible via header connector HDR7. This is a 20 pin male header, suitable for connection to a ribbon cable. Present at this header is power feed for external analog signal conditioning circuits, power ground and shield for each analog input, the 8 analog inputs themselves,

and a Vcc through a 10K pullup.

Analog Input HDR7

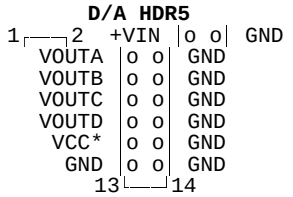


*Vcc is through a 10k pullup resistor.

DIGITAL TO ANALOG CONVERTOR

There are 4 D/A channels with 12 bit resolution, providing an output voltage range of 0 to 5 volts. When the MICROPAC 180 is reset, the 4 outputs go to 0 volts. Control data is written via a serial data link to the D/A, specifying the channel number and the 12 bit value to be output. See the assembly language drivers for programming details.

D/A HDR5



*Vcc is through a 10k pullup resistor.

WATCHDOG TIMER

The MICROPAC 180 has a circuit that resets the HD64180 microprocessor on power up, or it can accept an external reset via screw terminal ST1, or from a built in timer, called a watchdog timer. The watchdog timer is a 1 second R-C oscillator that resets the board approximately once a second, unless periodically re-triggered at shorter intervals. It is re-triggered by toggling RTS0 low then high (this is controlled by bit 4 of register CNTLA0.

Its purpose is to guard against software hang-ups induced by random electrical noise external to the MICROPAC 180. EMAC operating systems employ drivers that handle this function automatically, but user application programs can be easily written to do so as well. This safeguard is provided to enhance system reliability, but if necessary, the watchdog timer function can be disabled by jumper JP1.

TIMERS

The MICROPAC 180 comes equipped with two 16 bit timers which are resident in the HD64180/Z180 microprocessor. By loading a user programmable termination count, time intervals from microseconds to tenths of seconds are available. When the termination count is reached, an interrupt can then be issued to the MPU. The timer can also be set up to reload itself or to stop counting upon reaching the termination count. In either case, an interrupt can be issued. The timer interrupts are internally connected and controlled. The timer status can also be checked in a polled mode by reading the Timer Control Register.

These timers (TIMER0/PRT0, TIMER1/PRT1) are 16 bit down counters that count the timer input pulses and issues a HD64180/Z180 timer interrupt when the terminal pulse is reached. The user can reprogram the length of the count before the termination pulse is reached if so desired. The user can also determine the timer interval by programming the counter register from values 2H to FFFFH. The source of

timer input pulses is the system clock divided by 20 (307.2KHz for a clock frequency of 6.144 MHz and 460.8KHz for a clock frequency of 9.216MHz).

These timers are ideal as an external program interval timers. If you wish to perform a software operation at a specific time interval, then the timer/counter can be programmed to that interval. Upon the resulting timer interrupt your program can execute the desired software.

INTERRUPTS

The HD64180 microprocessor has four hardware interrupt input pins. They are: INT0*, INT1*, INT2*, and NMI* with interrupt inputs INT0 through INT2 being maskable. The microprocessor also has several internal interrupts for the serial communication ports, programmable reload timers, and DMA channels.

Expansion connector HDR1 provides access to the external hardware interrupts INT0 and INT1. Both inputs are pulled to ground by 3.9K resistors before being inverted by schmitt trigger invertors and input to the CPU's INT0* and INT1*. The INT1 input has a shared function; it also connects into the "wake up circuit" of the MICROPAC 180, and an input here will awaken a sleeping MICROPAC, as well as generate an interrupt input. Interrupt INT2* is directly connected to the INTB* output of the DS1286. The NMI* interrupt is accessible through screw terminal ST1.

The interrupts are arranged in a fixed priority. They will be described in order, from highest priority to lowest.

1. TRAP

The TRAP interrupt is an internally defined interrupt. It occurs when an undefined op-code is fetched. Software can use this interrupt for purposes of error detection or software debugging. This interrupt is non-maskable.

2. NMI

The NMI* interrupt is a non-maskable hardware interrupt and is activated when the pin input edge is low. The input must remain low for the MPU to acknowledge this interrupt. The NMI interrupt input is accessible via jumper JP6.

3. INT0*
4. INT1*

INT0 and INT1 may be masked by software, using the internal mask register in the MPU. The INT0* pin is active low and must be held low until acknowledged, then released. INT0 has 3 response modes: mode 0, mode 1 and mode 2. The mode defaults to 0 but may also be selected by the IM 0, IM 1 and IM 2 instructions respectively. Mode 1 will do a restart at address 0038h. Mode 0 and 2 require external hardware to operate (see appendix). INT1 requests an interrupt when held low and it must be held low until acknowledged.

Since the INT0 and INT1 pin inputs to the MPU are active low, inverters are placed ahead of them to provide hardware compatibility with existing EMAC SBCs. These interrupt lines both go to the Bus Expansion Connector header HDR1, for use by EMAC expansion peripherals or user created add on boards.

5. INT2*

INT2 requests an interrupt when held low and it must be held low until acknowledged. This interrupt is connected to the optional coprocessor which allows it to request attention of the main processor.

6. PRT channel 0
7. PRT channel 1
8. DMA channel 0
9. DMA channel 1
10. Clocked Serial I/O port
11. Asynchronous SCI channel 0
12. Asynchronous SCI channel 1

These remaining interrupts are all internal to the MPU. The MPU contains two timers, two asynchronous serial communication ports, two DMA channels, and one synchronous serial port. All these devices, when enabled, produce a unique interrupt vector response into the vector table, which must contain the associated interrupt handler address. All hardware interface is taken care of internally. All these interrupts may be enabled/disabled through software via a mask bit or by the EI/DI instructions.

Their interrupt vectors come from the IL register in the MPU, accessible via software (I/O address 33H). The IL vector joins up with the I register to point to the required interrupt handler code. Given the values programmed in I and IL, the table below can be used to determine the address of a vector for a particular interrupt.

	I								IL							
INT1	x	x	x	x	x	x	x	x	L	L	L	0	0	0	0	0
INT2	x	x	x	x	x	x	x	x	L	L	L	0	0	0	1	0
PRT channel 0	x	x	x	x	x	x	x	x	L	L	L	0	0	1	0	0
PRT channel 1	x	x	x	x	x	x	x	x	L	L	L	0	0	1	1	0
DMA channel 0	x	x	x	x	x	x	x	x	L	L	L	0	1	0	0	0
DMA channel 1	x	x	x	x	x	x	x	x	L	L	L	0	1	0	1	0
Clk Serial I/O	x	x	x	x	x	x	x	x	L	L	L	0	1	1	0	0
ASCI channel 0	x	x	x	x	x	x	x	x	L	L	L	0	1	1	1	0
ASCI channel 1	x	x	x	x	x	x	x	x	L	L	L	1	0	0	0	0

DMA

The HD64180 microprocessor chip has two DMA controller inputs and outputs, and the MICROPAC 180 provides access to these control signals via the bus expansion header HDR1, described below.

BUS EXPANSION

The MICROPAC 180 board has a bus expansion connector header, HDR1, which is suitable as a ribbon cable connector, to allow connection of expansion boards to the MICROPAC 180. Expansion cards allow the end user to custom tailor the MICROPAC 180 used in a system to have functions the MICROPAC 180 may not already have. Some functions are available as standard EMAC peripherals, or the end user may create his own.

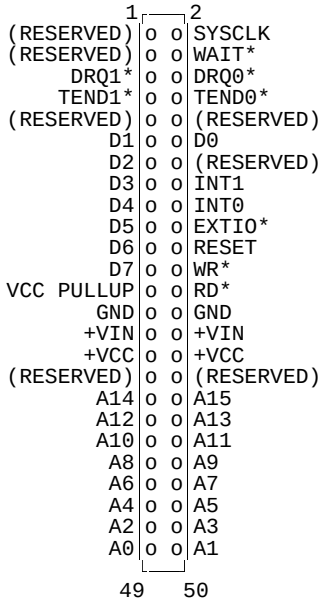
This connector allows connection to EMAC peripherals, as well as peripherals of your own design. Included are:

D0-D7	8 bit data bus
A0-A15	address bus lines
EXTIO*	external I/O select line which is asserted low when accessing I/O addresses 700H to 7FFH.
WR*	active low write select line
RD*	active low read select line
RESET	active high reset output from the DS1232 watchdog.
INT0, INT1	these are interrupt inputs that are inverted to drive INT0* and INT1* on the Z180. See section on interrupts.
GND, +VIN	these provide ground and the voltage supplied to pin 1 of ST1.
VCC	+5V source.
VCC PULLUP	this is a 10k pullup to Vcc.
SYSCLK	this is half the frequency of the CPU crystal.
WAIT*	active low input will introduce wait states in memory or I/O cycles
DRQ0*,TEND0*	handshake lines for DMA channel 0.
DRQ1*,TEND1*	handshake lines for DMA channel 1.

The reserved pins are not

connected on this revision of the MICROPAC 180 but may in future revisions, so to maintain compatibility they should be left unconnected in peripherals of your own design.

I/O EXPANSION CONNECTOR HDR1



CONTROL PORT D

Control Port D is used to control various on-board functions of the MICROPAC 180. Upon power up or RESET, they all are reset to 0 (LOW). Since many operations require setting/reseting bits without disturbing the others, the programmer should access the port with a subroutine which writes to the port, and write a copy of the bit pattern into a memory variable. When the D port is to be read, the driver will then retrieve the copy from memory, as the port itself cannot be read back. This copy may then be logically manipulated, and written to the port and its copy as required.

When reading Port D the bits are defined as follows:

Bit.Function.

0 Not used.
1 When this bit is low, the board has a 12.288 crystal installed. If high, a 24.576 crystal is installed.
2-5 Not used.
6 Clocked serial data receive input. This is used to read the data output by the clocked serial devices.
7 Handshake input. This bit will read a 0 or 1 for a + or - RS-232 input level, respectively.

When writing to Port D the bits are defined as follows :

Bit.Function.

0 Clocked serial device select 0 (S0). See Clock serial device select bits description below.
1 Clocked serial device select 1 (S1). See Clock serial device select bits description below.
2 Coprocessor active low handshake output.
3 Serial clock bit. This bit is used as a serial clock for communicating with the clocked serial I/O devices.

4 Clocked serial transmit bit. This bit is used to send serial data to the clocked serial I/O devices. It is used in conjunction with the serial clock bit to command and configure the devices.

5 Coprocessor active high reset output.

6 This bit enables the transmit side RS-422 driver when RS-422 option is installed in COM0. The receive side is always active. By default the transmitter is disabled. If this bit is set high (1), the transmitter is enabled. This bit has no effect when COM0 is optioned as RS-232.

7 COM1 handshake output. This bit is used as a handshaking bit on the COM 1 serial port. As defaulted, this bit is low, and the RS-232 line named RTS is high, or at +7 volts. Setting this port line high will switch the RTS line output to -7 volts.

Clock serial device select bits description.

S1	S0	Function.
0	0	Digital to Analog convertor LD* input.
0	1	Serial EEPROM select.
1	1	Analog to Digital convertor select.
1	1	Digital to Analog convertor select.

COPROCESSOR

The optional coprocessor adds the following features to the MICROPAC 180: an additional serial port with buffered inputs and outputs, a 4 by 4 keypad decoder and a 16 bit counter. All communication is through the Z180's Clocked Serial I/O interface (CSIO) with the INT2* interrupt used as an attention signal to the Z180. Due to the complexity of the interface it is described in the assembly language drivers software.

When special custom features are needed, many of these can be implemented on the coprocessor. EMAC can custom program the the coprocessor's firmware for almost unlimited applications (please call for an estimate on the cost for your application). Some hardware features available for a custom programmed coprocessor are: two 16 bit counter/timers, a serial port which can be used in synchronous or asynchronous mode, up to 12 I/O lines, and an analog comparator.

ON-BOARD I/O ADDRESSES

Following are the addresses of the on-board I/O devices.

0400H TO 04FFH 82C55 PPI, of which all I/O lines free to use as desired except for port B which should be used as an output only. Refer to the 82C55 data sheets for programming information.

0400	port A
0401	port B
0402	port C
0403	PPI control

0500H to 05FFH Control Port D.

0600H to 06FFH LCD panel control header. See OPTREX manual for programming data.

0500	LCD data address
0501	LCD control address

0700H to 07FFH These 256 I/O addresses are reserved for peripheral expansion cards. As consistent with previous designs, these addresses activate a special I/O expansion select line on the Expansion bus connector, that maps the I/O group for off-card use.

MPU INTERNAL I/O

ADDRESS	FUNCTION
00 hex	ASCI Control Register A Ch 0
01 hex	ASCI Control Register A Ch 1
02 hex	ASCI Control Register B Ch 0
03 hex	ASCI Control Register B Ch 1
04 hex	ASCI Status Register Ch 0
05 hex	ASCI Status Register Ch 1
06 hex	ASCI Transmit Data Register Ch 0
07 hex	ASCI Transmit Data Register Ch 1
08 hex	ASCI Receive Data Register Ch 0
09 hex	ASCI Receive Data Register Ch 1

0C hex Timer Data Register Ch 0 low byte
0D hex Timer Data Register Ch 0 High byte
0E hex Reload Register Ch 0 Low byte
0F hex Reload Register Ch 1 High byte
10 hex Timer Control Register

0A hex CSI/O Control Register
0B hex CSI/O Transmit/Receive Data Register

14 hex Timer Data Register Ch 1 low byte
15 hex Timer Data Register Ch 1 high byte
16 hex Reload Register Ch 1 low byte
17 hex Reload Register Ch 1 high byte

18 hex Free Running Counter

20 hex DMA Source Address Register Ch 0 low byte
21 hex DMA Source Address Register Ch 0 high byte
22 hex DMA Source Address Register Ch 0 bank byte
23 hex DMA Destination Address Register Ch 0 low byte
24 hex DMA Destination Address Register Ch 0 high byte
25 hex DMA Destination Address Register Ch 0 bank byte
26 hex DMA Byte Count Register Ch 0 low byte
27 hex DMA Byte Count Register Ch 0 high byte

28 hex DMA Memory Address Register Ch 1 low byte
29 hex DMA Memory Address Register Ch 1 high byte
2A hex DMA Memory Address Register Ch 1 bank byte
2B hex DMA I/O Address Register Ch 1 low byte
2C hex DMA I/O Address Register Ch 1 high byte
2E hex DMA Byte Count Register Ch 1 low byte
2F hex DMA Byte Count Register Ch 1 high byte
30 hex DMA Status Register
31 hex DMA Mode Register
32 hex DMA/WAIT Control Register

33 hex IL Register (Interrupt Vector Low)
34 hex INT/TRAP Control Register

36 hex Refresh control Register

38 hex MMU Common Base Register
39 hex MMU Bank Base Register
3A hex MMU Common/Bank Area Register

3E hex Operation Mode Control Register
3F hex I/O Control Register

Micropac 180 Rev. 2
On-board I/O Addresses

0400h to 04FFh	82C55 PPI, of which all I/O lines free to use as desired. Refer to 82C55 data sheets. 0400h port A 0401h port B 0402h port C 0403h PPI control
0500h to 05FF h	Port D (write only)
0600h to 06FF h	LCD panel control header. See Assembly Language Drivers and/or HD44780 LCD controller manual for programming data. 0600h LCD control address 0601h LCD data address
0700h to 07FFh	These 256 I/O addresses are reserved for peripheral expansion cards. As consistent with previous designs, these addresses activate a special I/O expansion select line on the Expansion Bus connector, that maps the I/O group for off-board use.

Micropac 180 Rev. 2
Jumper Description

JP1	Watchdog enable/disable.
JP2	RAM memory size jumper.
JP3,4,5	EPROM/Flash memory size jumper.
JP 6	Non maskable interrupt (NMI) access (the pin farthest from the board edge is NMI and the other is ground).
JP 7	LCD backlight control.
JP 8	On-board regulator bypass jumper.

APPENDIX A

Schematics

APPENDIX B

Data sheets